# AMD Xilinx - XC6VSX475T-1FF1156I Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 37200 |
| Number of Logic Elements/Cells | 476160 |
| Total RAM Bits | 39223296 |
| Number of I/O | 600 |
| Number of Gates | - |
| Voltage - Supply | 0.95V ~ 1.05V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 1156-BBGA, FCBGA |
| Supplier Device Package | 1156-FCBGA (35x35) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc6vsx475t-1ff1156i |

*Table 4:* **Typical Quiescent Supply Current *(Cont'd)***

| Symbol | Description | Device | Speed and Temperature Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | -3 (C) | -2 (C, E, & I) | -1 (C & I) | -1 (I & M)[2] | -1L (C) | -1L (I)[1] | |
| $I_{CCOQ}$ | Quiescent $V_{CCO}$ supply current | XC6VLX75T | 1 | 1 | 1 | N/A | 1 | 1 | mA |
| | | XC6VLX130T | 1 | 1 | 1 | N/A | 1 | 1 | mA |
| | | XC6VLX195T | 1 | 1 | 1 | N/A | 1 | 1 | mA |
| | | XC6VLX240T | 2 | 2 | 2 | N/A | 2 | 2 | mA |
| | | XC6VLX365T | 2 | 2 | 2 | N/A | 2 | 2 | mA |
| | | XC6VLX550T(3) | N/A | 3 | 3 | N/A | 3 | 3 | mA |
| | | XC6VLX760(3) | N/A | 3 | 3 | N/A | 3 | 3 | mA |
| | | XC6VSX315T | 2 | 2 | 2 | N/A | 2 | 2 | mA |
| | | XC6VSX475T(3) | N/A | 2 | 2 | N/A | 2 | 2 | mA |
| | | XC6VHX250T | 1 | 1 | 1 | N/A | N/A | N/A | mA |
| | | XC6VHX255T | 1 | 1 | 1 | N/A | N/A | N/A | mA |
| | | XC6VHX380T(4) | 2 | 2 | 2 | N/A | N/A | N/A | mA |
| | | XC6VHX565T(5) | N/A | 2 | 2 | N/A | N/A | N/A | mA |
| | | XQ6VLX130T | N/A | 1 | N/A | 1 | N/A | 1 | mA |
| | | XQ6VLX240T | N/A | 2 | N/A | 2 | N/A | 2 | mA |
| | | XQ6VLX550T(7) | N/A | N/A | N/A | 3 | N/A | 3 | mA |
| | | XQ6VSX315T | N/A | 2 | N/A | 2 | N/A | 2 | mA |
| | | XQ6VSX475T(7) | N/A | N/A | N/A | 2 | N/A | 2 | mA |

*Table 4:* **Typical Quiescent Supply Current *(Cont'd)***

| Symbol | Description | Device | Speed and Temperature Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | -3 (C) | -2 (C, E, & I) | -1 (C & I) | -1 (I & M)[2] | -1L (C) | -1L (I)[1] | |
| $I_{CCAUXQ}$ | Quiescent $V_{CCAUX}$ supply current | XC6VLX75T | 45 | 45 | 45 | N/A | 45 | 45 | mA |
| | | XC6VLX130T | 75 | 75 | 75 | N/A | 75 | 75 | mA |
| | | XC6VLX195T | 113 | 113 | 113 | N/A | 113 | 113 | mA |
| | | XC6VLX240T | 135 | 135 | 135 | N/A | 135 | 135 | mA |
| | | XC6VLX365T | 191 | 191 | 191 | N/A | 191 | 191 | mA |
| | | XC6VLX550T(3) | N/A | 286 | 286 | N/A | 286 | 286 | mA |
| | | XC6VLX760(3) | N/A | 387 | 387 | N/A | 387 | 387 | mA |
| | | XC6VSX315T | 186 | 186 | 186 | N/A | 186 | 186 | mA |
| | | XC6VSX475T(3) | N/A | 279 | 279 | N/A | 279 | 279 | mA |
| | | XC6VHX250T | 152 | 152 | 152 | N/A | N/A | N/A | mA |
| | | XC6VHX255T | 152 | 152 | 152 | N/A | N/A | N/A | mA |
| | | XC6VHX380T(4) | 227 | 227 | 227 | N/A | N/A | N/A | mA |
| | | XC6VHX565T(5) | N/A | 315 | 315 | N/A | N/A | N/A | mA |
| | | XQ6VLX130T(6) | N/A | 75 | N/A | 75 | N/A | 75 | mA |
| | | XQ6VLX240T(6) | N/A | 135 | N/A | 135 | N/A | 135 | mA |
| | | XQ6VLX550T(7) | N/A | N/A | N/A | 286 | N/A | 286 | mA |
| | | XQ6VSX315T(6) | N/A | 186 | N/A | 186 | N/A | 186 | mA |
| | | XQ6VSX475T(7) | N/A | N/A | N/A | 279 | N/A | 279 | mA |

**Notes:**

1. Typical values are specified at nominal voltage, 85°C junction temperatures ($T_j$). -1 and -2 industrial (I) grade devices have the same typical values as commercial (C) grade devices at 85°C, but higher values at 100°C. Use the XPE tool to calculate 100°C values. -1L industrial temperature range devices have the values specified in this column.
2. Use the XPE tool to calculate 125°C values for -1M temperature range devices.
3. The -2E extended temperature range ($T_j$ = 0°C to +100°C) is only available in these devices. The -2I temperature range ($T_j$ = –40°C to +100°C) is available for all other devices except the XC6VHX565T.
4. The XC6VHX380T is available with both -2E and -2I temperature ranges.
5. The XC6VHX565T is only available in the following temperature ranges: -1C, -1I, -2C, and -2E.
6. The XQ6VLX130T, XQ6VLX240T, and XQ6VSX315T are available in -2I, -1I, -1M, and -1LI temperature ranges.
7. The XQ6VLX550T and the XQ6VSX475T are only available in -1I and -1LI temperature ranges.
8. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
9. If DCI or differential signaling is used, more accurate quiescent current estimates can be obtained by using the XPE or XPower Analyzer (XPA) tools.

*Table 6:* **Power Supply Ramp Time**

| Symbol | Description | Ramp Time | Units |
|---|---|---|---|
| $V_{CCINT}$ | Internal supply voltage relative to GND | 0.20 to 50.0 | ms |
| $V_{CCO}$ | Output drivers supply voltage relative to GND | 0.20 to 50.0 | ms |
| $V_{CCAUX}$ | Auxiliary supply voltage relative to GND | 0.20 to 50.0 | ms |

## SelectIO™ DC Input and Output Levels

Values for $V_{IL}$ and $V_{IH}$ are recommended input voltages. Values for $I_{OL}$ and $I_{OH}$ are guaranteed over the recommended operating conditions at the $V_{OL}$ and $V_{OH}$ test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum $V_{CCO}$ with the respective $V_{OL}$ and $V_{OH}$ voltage levels shown. Other standards are sample tested.

*Table 7:* **SelectIO DC Input and Output Levels**

| I/O Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ | $V_{OH}$ | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|
| | V, Min | V, Max | V, Min | V, Max | V, Max | V, Min | mA | mA |
| LVCMOS25,<br>LVDCI25 | –0.3 | 0.7 | 1.7 | $V_{CCO}$ + 0.3 | 0.4 | $V_{CCO}$ – 0.4 | Note(3) | Note(3) |
| LVCMOS18,<br>LVDCI18 | –0.3 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.3 | 0.45 | $V_{CCO}$ – 0.45 | Note(4) | Note(4) |
| LVCMOS15,<br>LVDCI15 | –0.3 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.3 | 25% $V_{CCO}$ | 75% $V_{CCO}$ | Note(4) | Note(4) |
| LVCMOS12 | –0.3 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.3 | 25% $V_{CCO}$ | 75% $V_{CCO}$ | Note(5) | Note(5) |
| HSTL I_12 | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | $V_{CCO}$ + 0.3 | 25% $V_{CCO}$ | 75% $V_{CCO}$ | 6.3 | 6.3 |
| HSTL I(2) | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | $V_{CCO}$ + 0.3 | 0.4 | $V_{CCO}$ – 0.4 | 8 | –8 |
| HSTL II(2) | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | $V_{CCO}$ + 0.3 | 0.4 | $V_{CCO}$ – 0.4 | 16 | –16 |
| HSTL III(2) | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | $V_{CCO}$ + 0.3 | 0.4 | $V_{CCO}$ – 0.4 | 24 | –8 |
| DIFF HSTL I(2) | –0.3 | 50% $V_{CCO}$ – 0.1 | 50% $V_{CCO}$ + 0.1 | $V_{CCO}$ + 0.3 | – | – | – | – |
| DIFF HSTL II(2) | –0.3 | 50% $V_{CCO}$ – 0.1 | 50% $V_{CCO}$ + 0.1 | $V_{CCO}$ + 0.3 | – | – | – | – |
| SSTL2 I | –0.3 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | $V_{CCO}$ + 0.3 | $V_{TT}$ – 0.61 | $V_{TT}$ + 0.61 | 8.1 | –8.1 |
| SSTL2 II | –0.3 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | $V_{CCO}$ + 0.3 | $V_{TT}$ – 0.81 | $V_{TT}$ + 0.81 | 16.2 | –16.2 |
| DIFF SSTL2 I | –0.3 | 50% $V_{CCO}$ – 0.15 | 50% $V_{CCO}$ + 0.15 | $V_{CCO}$ + 0.3 | – | – | – | – |
| DIFF SSTL2 II | –0.3 | 50% $V_{CCO}$ – 0.15 | 50% $V_{CCO}$ + 0.15 | $V_{CCO}$ + 0.3 | – | – | – | – |
| SSTL18 I | –0.3 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCO}$ + 0.3 | $V_{TT}$ – 0.47 | $V_{TT}$ + 0.47 | 6.7 | –6.7 |
| SSTL18 II | –0.3 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCO}$ + 0.3 | $V_{TT}$ – 0.60 | $V_{TT}$ + 0.60 | 13.4 | –13.4 |
| DIFF SSTL18 I | –0.3 | 50% $V_{CCO}$ – 0.125 | 50% $V_{CCO}$ + 0.125 | $V_{CCO}$ + 0.3 | – | – | – | – |
| DIFF SSTL18 II | –0.3 | 50% $V_{CCO}$ – 0.125 | 50% $V_{CCO}$ + 0.125 | $V_{CCO}$ + 0.3 | – | – | – | – |
| SSTL15 | –0.3 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | $V_{CCO}$ + 0.3 | $V_{TT}$ – 0.175 | $V_{TT}$ + 0.175 | 14.3 | 14.3 |

**Notes:**

1. Tested according to relevant specifications.
2. Applies to both 1.5V and 1.8V HSTL.
3. Using drive strengths of 2, 4, 6, 8, 12, 16, or 24 mA.
4. Using drive strengths of 2, 4, 6, 8, 12, or 16 mA.
5. Supported drive strengths of 2, 4, 6, or 8 mA.
6. For detailed interface specific DC voltage levels, see UG361:*Virtex-6 FPGA SelectIO Resources User Guide*.

## HT DC Specifications (HT_25)

*Table 8:* **HT DC Specifications**

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCO}$ | Supply Voltage | | 2.38 | 2.5 | 2.63 | V |
| $V_{OD}$ | Differential Output Voltage for XC devices | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 480 | 600 | 885 | mV |
| | Differential Output Voltage for XQ devices | | 480 | 600 | 930 | mV |
| $\Delta V_{OD}$ | Change in $V_{OD}$ Magnitude | | –15 | – | 15 | mV |
| $V_{OCM}$ | Output Common Mode Voltage | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 440 | 600 | 760 | mV |
| $\Delta V_{OCM}$ | Change in $V_{OCM}$ Magnitude | | –15 | – | 15 | mV |
| $V_{ID}$ | Input Differential Voltage | | 200 | 600 | 1000 | mV |
| $\Delta V_{ID}$ | Change in $V_{ID}$ Magnitude | | –15 | – | 15 | mV |
| $V_{ICM}$ | Input Common Mode Voltage | | 440 | 600 | 780 | mV |
| $\Delta V_{ICM}$ | Change in $V_{ICM}$ Magnitude | | –15 | – | 15 | mV |

## LVDS DC Specifications (LVDS_25)

*Table 9:* **LVDS DC Specifications**

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCO}$ | Supply Voltage | | 2.38 | 2.5 | 2.63 | V |
| $V_{OH}$ | Output High Voltage for Q and $\overline{Q}$ | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | – | – | 1.675 | V |
| $V_{OL}$ | Output Low Voltage for Q and $\overline{Q}$ | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 0.825 | – | – | V |
| $V_{ODIFF}$ | Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 247 | 350 | 600 | mV |
| $V_{OCM}$ | Output Common-Mode Voltage for XC devices | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 1.075 | 1.250 | 1.425 | V |
| | Output Common-Mode Voltage for XQ devices | | 1.000 | 1.250 | 1.425 | V |
| $V_{IDIFF}$ | Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High | | 100 | 350 | 600 | mV |
| $V_{ICM}$ | Input Common-Mode Voltage | | 0.3 | 1.2 | 2.2 | V |

## Extended LVDS DC Specifications (LVDSEXT_25)

*Table 10:* **Extended LVDS DC Specifications**

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCO}$ | Supply Voltage | | 2.38 | 2.5 | 2.63 | V |
| $V_{OH}$ | Output High Voltage for Q and $\overline{Q}$ | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | – | – | 1.785 | V |
| $V_{OL}$ | Output Low Voltage for Q and $\overline{Q}$ | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 0.715 | – | – | V |
| $V_{ODIFF}$ | Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High for XC devices | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 350 | – | 840 | mV |
| | Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High for XQ devices | | 350 | – | 850 | mV |
| $V_{OCM}$ | Output Common-Mode Voltage for XC devices | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 1.075 | 1.250 | 1.425 | V |
| | Output Common-Mode Voltage for XQ devices | | 1.000 | 1.250 | 1.425 | V |
| $V_{IDIFF}$ | Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High | Common-mode input voltage = 1.25V | 100 | – | 1000 | mV |
| $V_{ICM}$ | Input Common-Mode Voltage | Differential input voltage = ±350 mV | 0.3 | 1.2 | 2.2 | V |

*Table 16:* **GTX Transceiver Quiescent Supply Current (per Lane)** (1)(2)(3)

| Symbol | Description | Typ(4) | Max | Units |
|---|---|---|---|---|
| $I_{MGTAVTTQ}$ | Quiescent MGTAVTT supply current for one GTX transceiver | 0.9 | Note 2 | mA |
| $I_{MGTAVCCQ}$ | Quiescent MGTAVCC supply current for one GTX transceiver | 3.5 | | mA |

**Notes:**

1. Device powered and unconfigured.
2. Currents for conditions other than values specified in this table can be obtained by using the XPE or XPA tools.
3. GTX transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTX transceivers.
4. Typical values are specified at nominal voltage, 25°C.

## GTX Transceiver DC Input and Output Levels

Table 17 summarizes the DC output specifications of the GTX transceivers in Virtex-6 FPGAs. Consult UG366: *Virtex-6 FPGA GTX Transceivers User Guide* for further details.

*Table 17:* **GTX Transceiver DC Specifications**

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $DV_{PPIN}$ | Differential peak-to-peak input voltage | External AC coupled ≤ 4.25 Gb/s | 125 | – | 2000 | mV |
| | | External AC coupled > 4.25 Gb/s | 175 | – | 2000 | mV |
| $V_{IN}$ | Absolute input voltage | DC coupled<br>MGTAVTT = 1.2V | –400 | – | MGTAVTT | mV |
| $V_{CMIN}$ | Common mode input voltage | DC coupled<br>MGTAVTT = 1.2V | – | 2/3 MGTAVTT | – | mV |
| $DV_{PPOUT}$ | Differential peak-to-peak output voltage (1) | Transmitter output swing is set to maximum setting | – | – | 1000 | mV |
| $V_{CMOUTDC}$ | DC common mode output voltage. | Equation based | MGTAVTT – $DV_{PPOUT}$/4 | | | mV |
| $R_{IN}$ | Differential input resistance | | 80 | 100 | 130 | Ω |
| $R_{OUT}$ | Differential output resistance | | 80 | 100 | 120 | Ω |
| $T_{OSKEW}$ | Transmitter output pair (TXP and TXN) intra-pair skew | | – | 2 | 8 | ps |
| $C_{EXT}$ | Recommended external AC coupling capacitor(2) | | – | 100 | – | nF |

**Notes:**

1. The output swing and preemphasis levels are programmable using the attributes discussed in UG366: *Virtex-6 FPGA GTX Transceivers User Guide* and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

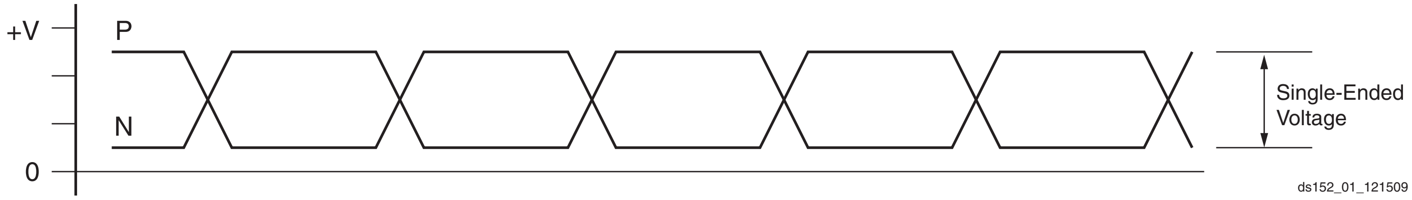

*Figure 1:* **Single-Ended Peak-to-Peak Voltage**

*Table 21:* **GTX Transceiver Reference Clock Switching Characteristics**

| Symbol | Description | Conditions | All Speed Grades | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $F_{GCLK}$ | Reference clock frequency range | | 62.5 | – | 650 | MHz |
| $T_{RCLK}$ | Reference clock rise time | 20% – 80% | – | 200 | – | ps |
| $T_{FCLK}$ | Reference clock fall time | 80% – 20% | – | 200 | – | ps |
| $T_{DCREF}$ | Reference clock duty cycle | Transceiver PLL only | 45 | 50 | 55 | % |
| $T_{LOCK}$ | Clock recovery frequency acquisition time | Initial PLL lock | – | – | 1 | ms |
| $T_{PHASE}$ | Clock recovery phase acquisition time | Lock to data after PLL has locked to the reference clock | – | – | 200 | µs |

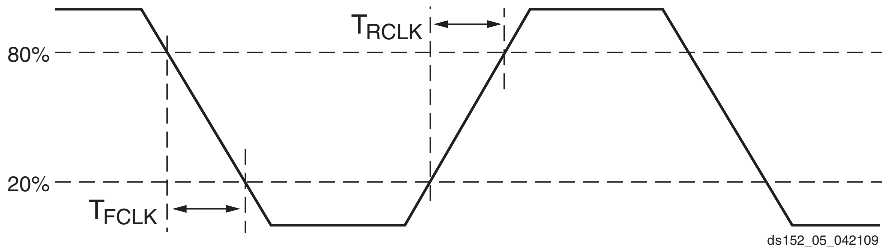

*Figure 3:* **Reference Clock Timing Parameters**

*Table 22:* **GTX Transceiver User Clock Switching Characteristics**(1)

| Symbol | Description | Conditions | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1 | -1L | |
| $F_{TXOUT}$ | TXOUTCLK maximum frequency | Internal 20-bit data path | 330 | 330 | 250 | 250 | MHz |
| | | Internal 16-bit data path | 412.5 | 412.5 | 312.5 | 250 | MHz |
| $F_{RXREC}$ | RXRECCLK maximum frequency | Internal 20-bit data path | 330 | 330 | 250 | 250 | MHz |
| | | Internal 16-bit data path | 412.5 | 412.5 | 312.5 | 250 | MHz |
| $T_{RX}$ | RXUSRCLK maximum frequency | | 412.5(2) | 412.5(2) | 312.5 | 250 | MHz |
| $T_{RX2}$ | RXUSRCLK2 maximum frequency | 1 byte interface | 376 | 376 | 312.5 | 250 | MHz |
| | | 2 byte interface | 406.25 | 406.25 | 312.5 | 250 | MHz |
| | | 4 byte interface | 206.25 | 206.25 | 156.25 | 125 | MHz |
| $T_{TX}$ | TXUSRCLK maximum frequency | | 412.5(3) | 412.5(3) | 312.5 | 250 | MHz |
| $T_{TX2}$ | TXUSRCLK2 maximum frequency | 1 byte interface | 376 | 376 | 312.5 | 250 | MHz |
| | | 2 byte interface | 406.25 | 406.25 | 312.5 | 250 | MHz |
| | | 4 byte interface | 206.25 | 206.25 | 156.25 | 125 | MHz |

**Notes:**

1. Clocking must be implemented as described in UG366:*Virtex-6 FPGA GTX Transceivers User Guide*.
2. 406.25 MHz when the RX elastic buffer is bypassed.
3. 406.25 MHz when the TX buffer is bypassed.

*Table 24:* **GTX Transceiver Receiver Switching Characteristics**

| Symbol | Description | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{GTXRX}$ | Serial data rate | RX oversampler not enabled | 0.600 | – | $F_{GTXMAX}$ | Gb/s |
| | | RX oversampler enabled | 0.480 | – | 0.600 | Gb/s |
| $T_{RXELECIDLE}$ | Time for RXELECIDLE to respond to loss or restoration of data | | – | 75 | – | ns |
| $RX_{OOBVDPP}$ | OOB detect threshold peak-to-peak | | 60 | – | 150 | mV |
| $RX_{SST}$ | Receiver spread-spectrum tracking(1) | Modulated @ 33 KHz | –5000 | – | 0 | ppm |
| $RX_{RL}$ | Run length (CID) | Internal AC capacitor bypassed | – | – | 512 | UI |
| $RX_{PPMTOL}$ | Data/REFCLK PPM offset tolerance | CDR 2nd-order loop disabled | –200 | – | 200 | ppm |
| | | CDR 2nd-order loop enabled | –2000 | – | 2000 | ppm |
| **SJ Jitter Tolerance(2)** | | | | | | |
| $JT\_SJ_{6.5}$ | Sinusoidal Jitter(3) | 6.5 Gb/s | 0.44 | – | – | UI |
| $JT\_SJ_{5.0}$ | Sinusoidal Jitter(3) | 5.0 Gb/s | 0.44 | – | – | UI |
| $JT\_SJ_{4.25}$ | Sinusoidal Jitter(3) | 4.25 Gb/s | 0.44 | – | – | UI |
| $JT\_SJ_{3.75}$ | Sinusoidal Jitter(3) | 3.75 Gb/s | 0.44 | – | – | UI |
| $JT\_SJ_{3.125}$ | Sinusoidal Jitter(3) | 3.125 Gb/s | 0.45 | – | – | UI |
| $JT\_SJ_{3.125L}$ | Sinusoidal Jitter(3) | 3.125 Gb/s(4) | 0.45 | – | – | UI |
| $JT\_SJ_{2.5}$ | Sinusoidal Jitter(3) | 2.5 Gb/s(5) | 0.5 | – | – | UI |
| $JT\_SJ_{1.25}$ | Sinusoidal Jitter(3) | 1.25 Gb/s(6) | 0.5 | – | – | UI |
| $JT\_SJ_{600}$ | Sinusoidal Jitter(3) | 600 Mb/s | 0.4 | – | – | UI |
| $JT\_SJ_{480}$ | Sinusoidal Jitter(3) | 480 Mb/s | 0.4 | – | – | UI |
| **SJ Jitter Tolerance with Stressed Eye(2)** | | | | | | |
| $JT\_TJSE_{3.125}$ | Total Jitter with Stressed Eye(7) | 3.125 Gb/s | 0.70 | – | – | UI |
| | | 5.0 Gb/s | 0.70 | – | – | UI |
| $JT\_SJSE_{3.125}$ | Sinusoidal Jitter with Stressed Eye(7) | 3.125 Gb/s | 0.1 | – | – | UI |
| | | 5.0 Gb/s | 0.1 | – | – | UI |

**Notes:**

1. Using PLL_RXDIVSEL_OUT = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of 1e$^{-12}$.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. PLL frequency at 1.5625 GHz and OUTDIV = 1.
5. PLL frequency at 2.5 GHz and OUTDIV = 2.
6. PLL frequency at 2.5 GHz and OUTDIV = 4.
7. Composite jitter with RX equalizer enabled. DFE disabled.

## GTH Transceiver Switching Characteristics

Consult UG371: *Virtex-6 FPGA GTH Transceivers User Guide* for further information.

*Table 32:* **GTH Transceiver Maximum Data Rate and PLL Frequency Range**

| Symbol | Description | Conditions | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1 | |
| $F_{GTHMAX}$ | Maximum GTH transceiver data rate | PLL Output Divider = 1 | 11.182 | 11.182 | 10.32 | Gb/s |
| | | PLL Output Divider = 4 | 2.795 | 2.795 | 2.58 | Gb/s |
| $F_{GTHMIN}$ | Minimum GTH transceiver data rate(1) | PLL Output Divider = 1 | 9.92 | 9.92 | 9.92 | Gb/s |
| | | PLL Output Divider = 4 | 2.48 | 2.48 | 2.48 | Gb/s |
| $F_{GPLLMAX}$ | Maximum GTH PLL frequency | | 5.591 | 5.591 | 5.16 | GHz |
| $F_{GPLLMIN}$ | Minimum GTH PLL frequency | | 4.96 | 4.96 | 4.96 | GHz |

**Notes:**

1. Lower data rates can be achieved using FPGA logic based oversampling designs.

*Table 33:* **GTH Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2 | -1 | |
| $F_{GTHDRPCLK}$ | GTHDRPCLK maximum frequency | 70 | 70 | 60 | MHz |

*Table 34:* **GTH Transceiver Reference Clock Switching Characteristics**

| Symbol | Description | Conditions | All Speed Grades | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $F_{GCLK}$ | Reference clock frequency range | -1 speed grade | 150 | – | 645 | MHz |
| | | -2 and -3 speed grades | 150 | – | 700 | MHz |
| $T_{RCLK}$ | Reference clock rise time | 20% – 80% | – | 200 | – | ps |
| $T_{FCLK}$ | Reference clock fall time | 80% – 20% | – | 200 | – | ps |
| $T_{DCREF}$ | Reference clock duty cycle | CLK | 45 | 50 | 55 | % |
| $T_{LOCK}$ | Clock recovery frequency acquisition time | Initial PLL lock | – | – | 2 | ms |
| $T_{PHASE}$ | Clock recovery phase acquisition time | Lock to data after PLL has locked to the reference clock | – | – | 20 | µs |

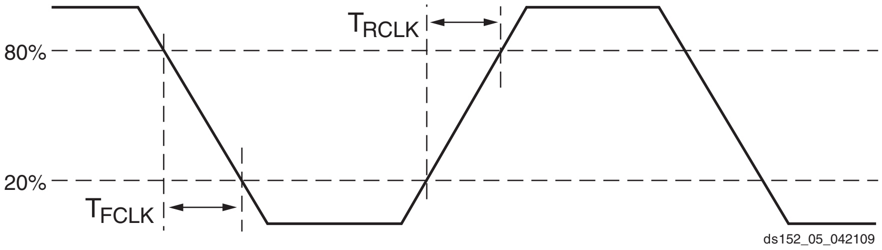

*Figure 5:* **Reference Clock Timing Parameters**

## Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:
http://www.xilinx.com/technology/protocols/pciexpress.htm

*Table 39:* **Maximum Performance for PCI Express Designs**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 | -1L | |
| $F_{PIPECLK}$ | Pipe clock maximum frequency | 250 | 250 | 250 | 250 | MHz |
| $F_{USERCLK}$ | User clock maximum frequency | 500 | 500 | 250 | 250 | MHz |
| $F_{DRPCLK}$ | DRP clock maximum frequency | 250 | 250 | 250 | 250 | MHz |

## System Monitor Analog-to-Digital Converter Specification

*Table 40:* **Analog-to-Digital Specifications**

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $AV_{DD}$ = 2.5V ± 5%, $V_{REFP}$ = 1.25V, $V_{REFN}$ = 0V, ADCCLK = 5.2 MHz, $T_j$ = –55°C to 125°C M-Grade, Typical values at $T_j$=+35°C | | | | | | |
| **DC Accuracy:** All external input channels. Both unipolar and bipolar modes. | | | | | | |
| Resolution | | | 10 | – | – | Bits |
| Integral Nonlinearity | INL | | – | – | ±1 | LSBs |
| Differential Nonlinearity | DNL | No missing codes ($T_{MIN}$ to $T_{MAX}$)<br>Guaranteed Monotonic | – | – | ±0.9 | LSBs |
| Unipolar Offset Error (1) | | Uncalibrated | – | ±2 | ±30 | LSBs |
| Bipolar Offset Error (1) | | Uncalibrated measured in bipolar mode | – | ±2 | ±30 | LSBs |
| Gain Error | | Uncalibrated - External Reference | – | ±0.2 | ±2 | % |
| | | Uncalibrated - Internal Reference | – | ±2 | – | % |
| Bipolar Gain Error (1) | | Uncalibrated - External Reference | – | ±0.2 | ±2 | % |
| | | Uncalibrated - Internal Reference | – | ±2 | – | % |
| Total Unadjusted Error (Uncalibrated) | TUE | Deviation from ideal transfer function. External 1.25V reference | – | ±10 | – | LSBs |
| | | Deviation from ideal transfer function. Internal reference | – | ±20 | – | LSBs |
| Total Unadjusted Error (Calibrated) | TUE | Deviation from ideal transfer function. External 1.25V reference | – | ±1 | ±2 | LSBs |
| Calibrated Gain Temperature Coefficient | | Variation of FS code with temperature | – | ±0.01 | – | LSB/°C |
| DC Common-Mode Reject | $CMRR_{DC}$ | $V_N = V_{CM}$ = 0.5V ± 0.5V,<br>$V_P - V_N$ = 100mV | – | 70 | – | dB |
| **Conversion Rate**(2) | | | | | | |
| Conversion Time - Continuous | $t_{CONV}$ | Number of CLK cycles | 26 | – | 32 | |
| Conversion Time - Event | $t_{CONV}$ | Number of CLK cycles | – | – | 21 | |
| T/H Acquisition Time | $t_{ACQ}$ | Number of CLK cycles | 4 | – | – | |
| DRP Clock Frequency | DCLK | DRP clock frequency | 8 | – | 80 | MHz |
| ADC Clock Frequency | ADCCLK | Derived from DCLK | 1 | – | 5.2 | MHz |
| CLK Duty cycle | | | 40 | – | 60 | % |

*Table 44:* **IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | | $T_{IOOP}$ | | | | $T_{IOTP}$ | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | -3 | -2 | -1 | -1L | -3 | -2 | -1 | -1L | -3 | -2 | -1 | -1L | |
| DIFF_SSTL18_I | 0.85 | 0.94 | 1.09 | 1.08 | 1.47 | 1.58 | 1.75 | 1.73 | 1.47 | 1.58 | 1.75 | 1.73 | ns |
| DIFF_SSTL18_I_DCI | 0.85 | 0.94 | 1.09 | 1.08 | 1.40 | 1.51 | 1.67 | 1.65 | 1.40 | 1.51 | 1.67 | 1.65 | ns |
| DIFF_SSTL18_II | 0.85 | 0.94 | 1.09 | 1.08 | 1.39 | 1.50 | 1.67 | 1.66 | 1.39 | 1.50 | 1.67 | 1.66 | ns |
| DIFF_SSTL18_II_DCI | 0.85 | 0.94 | 1.09 | 1.08 | 1.36 | 1.47 | 1.63 | 1.62 | 1.36 | 1.47 | 1.63 | 1.62 | ns |
| DIFF_SSTL18_II_T_DCI | 0.85 | 0.94 | 1.09 | 1.08 | 1.40 | 1.51 | 1.67 | 1.65 | 1.40 | 1.51 | 1.67 | 1.65 | ns |
| DIFF_SSTL15 | 0.81 | 0.91 | 1.06 | 1.06 | 1.42 | 1.54 | 1.71 | 1.69 | 1.42 | 1.54 | 1.71 | 1.69 | ns |
| DIFF_SSTL15_DCI | 0.81 | 0.91 | 1.06 | 1.06 | 1.41 | 1.52 | 1.68 | 1.66 | 1.41 | 1.52 | 1.68 | 1.66 | ns |
| DIFF_SSTL15_T_DCI | 0.81 | 0.91 | 1.06 | 1.06 | 1.41 | 1.52 | 1.68 | 1.66 | 1.41 | 1.52 | 1.68 | 1.66 | ns |

*Table 45:* **IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices**

| I/O Standard | $T_{IOPI}$ | | | $T_{IOOP}$ | | | $T_{IOTP}$ | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | Speed Grade | | | Speed Grade | | | |
| | -2 | -1 | -1L | -2 | -1 | -1L | -2 | -1 | -1L | |
| LVDS_25 | 0.94 | 1.09 | 1.08 | 1.54 | 2.16 | 1.62 | 1.54 | 2.16 | 1.62 | ns |
| LVDSEXT_25 | 0.94 | 1.09 | 1.08 | 1.65 | 2.20 | 1.73 | 1.65 | 2.20 | 1.73 | ns |
| HT_25 | 0.94 | 1.09 | 1.08 | 1.62 | 2.20 | 1.69 | 1.62 | 2.20 | 1.69 | ns |
| BLVDS_25 | 0.94 | 1.09 | 1.08 | 1.50 | 3.18 | 1.65 | 1.50 | 3.18 | 1.65 | ns |
| RSDS_25 (point to point) | 0.94 | 1.09 | 1.08 | 1.54 | 2.22 | 1.62 | 1.54 | 2.22 | 1.62 | ns |
| HSTL_I | 0.91 | 1.06 | 1.06 | 1.56 | 2.44 | 1.71 | 1.56 | 2.44 | 1.71 | ns |
| HSTL_II | 0.91 | 1.06 | 1.06 | 1.56 | 2.21 | 1.72 | 1.56 | 2.21 | 1.72 | ns |
| HSTL_III | 0.91 | 1.06 | 1.06 | 1.54 | 2.50 | 1.69 | 1.54 | 2.50 | 1.69 | ns |
| HSTL_I_18 | 0.91 | 1.06 | 1.06 | 1.58 | 2.43 | 1.72 | 1.58 | 2.43 | 1.72 | ns |
| HSTL_II_18 | 0.91 | 1.06 | 1.06 | 1.62 | 2.30 | 1.78 | 1.62 | 2.30 | 1.78 | ns |
| HSTL_III_18 | 0.91 | 1.06 | 1.06 | 1.54 | 2.49 | 1.69 | 1.54 | 2.49 | 1.69 | ns |
| SSTL2_I | 0.91 | 1.06 | 1.06 | 1.60 | 2.50 | 1.74 | 1.60 | 2.50 | 1.74 | ns |
| SSTL2_II | 0.91 | 1.06 | 1.06 | 1.54 | 2.49 | 1.71 | 1.54 | 2.49 | 1.71 | ns |
| SSTL15 | 0.91 | 1.06 | 1.06 | 1.54 | 2.07 | 1.69 | 1.54 | 2.07 | 1.69 | ns |
| LVCMOS25, Slow, 2 mA | 0.57 | 0.66 | 0.70 | 5.46 | 6.01 | 5.63 | 5.46 | 6.01 | 5.63 | ns |
| LVCMOS25, Slow, 4 mA | 0.57 | 0.66 | 0.70 | 3.49 | 3.79 | 3.65 | 3.49 | 3.79 | 3.65 | ns |
| LVCMOS25, Slow, 6 mA | 0.57 | 0.66 | 0.70 | 2.81 | 3.08 | 2.95 | 2.81 | 3.08 | 2.95 | ns |
| LVCMOS25, Slow, 8 mA | 0.57 | 0.66 | 0.70 | 2.41 | 2.72 | 2.59 | 2.41 | 2.72 | 2.59 | ns |
| LVCMOS25, Slow, 12 mA | 0.57 | 0.66 | 0.70 | 1.95 | 2.23 | 2.10 | 1.95 | 2.23 | 2.10 | ns |
| LVCMOS25, Slow, 16 mA | 0.57 | 0.66 | 0.70 | 2.05 | 2.29 | 2.21 | 2.05 | 2.29 | 2.21 | ns |
| LVCMOS25, Slow, 24 mA | 0.57 | 0.66 | 0.70 | 1.82 | 2.24 | 1.98 | 1.82 | 2.24 | 1.98 | ns |
| LVCMOS25, Fast, 2 mA | 0.57 | 0.66 | 0.70 | 5.49 | 6.04 | 5.62 | 5.49 | 6.04 | 5.62 | ns |
| LVCMOS25, Fast, 4 mA | 0.57 | 0.66 | 0.70 | 3.50 | 3.82 | 3.65 | 3.50 | 3.82 | 3.65 | ns |
| LVCMOS25, Fast, 6 mA | 0.57 | 0.66 | 0.70 | 2.73 | 2.99 | 2.88 | 2.73 | 2.99 | 2.88 | ns |
| LVCMOS25, Fast, 8 mA | 0.57 | 0.66 | 0.70 | 2.33 | 2.65 | 2.53 | 2.33 | 2.65 | 2.53 | ns |
| LVCMOS25, Fast, 12 mA | 0.57 | 0.66 | 0.70 | 1.88 | 2.08 | 2.03 | 1.88 | 2.08 | 2.03 | ns |

*Table 45:* **IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices** ***(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | $T_{IOOP}$ | | | $T_{IOTP}$ | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | Speed Grade | | | Speed Grade | | | |
| | -2 | -1 | -1L | -2 | -1 | -1L | -2 | -1 | -1L | |
| LVDCI_DV2_18 | 0.61 | 0.72 | 0.73 | 1.81 | 2.36 | 1.98 | 1.81 | 2.36 | 1.98 | ns |
| LVDCI_DV2_15 | 0.73 | 0.85 | 0.85 | 1.77 | 2.30 | 1.98 | 1.77 | 2.30 | 1.98 | ns |
| LVPECL_25 | 0.94 | 1.09 | 1.08 | 1.49 | 2.68 | 1.64 | 1.49 | 2.68 | 1.64 | ns |
| HSTL_I_12 | 0.91 | 1.06 | 1.06 | 1.60 | 2.48 | 1.74 | 1.60 | 2.48 | 1.74 | ns |
| HSTL_I_DCI | 0.91 | 1.06 | 1.06 | 1.50 | 2.43 | 1.64 | 1.50 | 2.43 | 1.64 | ns |
| HSTL_II_DCI | 0.91 | 1.06 | 1.06 | 1.49 | 2.39 | 1.66 | 1.49 | 2.39 | 1.66 | ns |
| HSTL_II_T_DCI | 0.91 | 1.06 | 1.06 | 1.50 | 2.43 | 1.64 | 1.50 | 2.43 | 1.64 | ns |
| HSTL_III_DCI | 0.91 | 1.06 | 1.06 | 1.45 | 2.48 | 1.61 | 1.45 | 2.48 | 1.61 | ns |
| HSTL_I_DCI_18 | 0.91 | 1.06 | 1.06 | 1.53 | 2.44 | 1.66 | 1.53 | 2.44 | 1.66 | ns |
| HSTL_II_DCI_18 | 0.91 | 1.06 | 1.06 | 1.46 | 2.41 | 1.59 | 1.46 | 2.41 | 1.59 | ns |
| HSTL_II _T_DCI_18 | 0.91 | 1.06 | 1.06 | 1.53 | 2.43 | 1.66 | 1.53 | 2.43 | 1.66 | ns |
| HSTL_III_DCI_18 | 0.91 | 1.06 | 1.06 | 1.54 | 2.50 | 1.67 | 1.54 | 2.50 | 1.67 | ns |
| DIFF_HSTL_I_18 | 0.94 | 1.09 | 1.08 | 1.58 | 2.30 | 1.72 | 1.58 | 2.30 | 1.72 | ns |
| DIFF_HSTL_I_DCI_18 | 0.94 | 1.09 | 1.08 | 1.53 | 2.21 | 1.66 | 1.53 | 2.21 | 1.66 | ns |
| DIFF_HSTL_I | 0.94 | 1.09 | 1.08 | 1.56 | 2.28 | 1.71 | 1.56 | 2.28 | 1.71 | ns |
| DIFF_HSTL_I_DCI | 0.94 | 1.09 | 1.08 | 1.50 | 2.28 | 1.64 | 1.50 | 2.28 | 1.64 | ns |
| DIFF_HSTL_II_18 | 0.94 | 1.09 | 1.08 | 1.62 | 2.33 | 1.78 | 1.62 | 2.33 | 1.78 | ns |
| DIFF_HSTL_II_DCI_18 | 0.94 | 1.09 | 1.08 | 1.46 | 2.18 | 1.59 | 1.46 | 2.18 | 1.59 | ns |
| DIFF_HSTL_II _T_DCI_18 | 0.94 | 1.09 | 1.08 | 1.53 | 2.22 | 1.66 | 1.53 | 2.22 | 1.66 | ns |
| DIFF_HSTL_II | 0.94 | 1.09 | 1.08 | 1.56 | 2.29 | 1.72 | 1.56 | 2.29 | 1.72 | ns |
| DIFF_HSTL_II_DCI | 0.94 | 1.09 | 1.08 | 1.49 | 2.26 | 1.66 | 1.49 | 2.26 | 1.66 | ns |
| SSTL2_I_DCI | 0.91 | 1.06 | 1.06 | 1.53 | 2.51 | 1.68 | 1.53 | 2.51 | 1.68 | ns |
| SSTL2_II_DCI | 0.91 | 1.06 | 1.06 | 1.50 | 2.50 | 1.69 | 1.50 | 2.50 | 1.69 | ns |
| SSTL2_II_T_DCI | 0.91 | 1.06 | 1.06 | 1.53 | 2.52 | 1.68 | 1.53 | 2.52 | 1.68 | ns |
| SSTL18_I | 0.91 | 1.06 | 1.06 | 1.58 | 2.48 | 1.73 | 1.58 | 2.48 | 1.73 | ns |
| SSTL18_II | 0.91 | 1.06 | 1.06 | 1.50 | 2.46 | 1.66 | 1.50 | 2.46 | 1.66 | ns |
| SSTL18_I_DCI | 0.91 | 1.06 | 1.06 | 1.51 | 2.49 | 1.65 | 1.51 | 2.49 | 1.65 | ns |
| SSTL18_II_DCI | 0.91 | 1.06 | 1.06 | 1.47 | 2.41 | 1.62 | 1.47 | 2.41 | 1.62 | ns |
| SSTL18_II_T_DCI | 0.91 | 1.06 | 1.06 | 1.51 | 2.49 | 1.65 | 1.51 | 2.49 | 1.65 | ns |
| SSTL15_T_DCI | 0.91 | 1.06 | 1.06 | 1.52 | 2.48 | 1.66 | 1.52 | 2.48 | 1.66 | ns |
| SSTL15_DCI | 0.91 | 1.06 | 1.06 | 1.52 | 2.48 | 1.66 | 1.52 | 2.48 | 1.66 | ns |
| DIFF_SSTL2_I | 0.94 | 1.09 | 1.08 | 1.60 | 2.34 | 1.74 | 1.60 | 2.34 | 1.74 | ns |
| DIFF_SSTL2_I_DCI | 0.94 | 1.09 | 1.08 | 1.53 | 2.25 | 1.68 | 1.53 | 2.25 | 1.68 | ns |
| DIFF_SSTL2_II | 0.94 | 1.09 | 1.08 | 1.54 | 2.29 | 1.71 | 1.54 | 2.29 | 1.71 | ns |
| DIFF_SSTL2_II_DCI | 0.94 | 1.09 | 1.08 | 1.50 | 2.23 | 1.69 | 1.50 | 2.23 | 1.69 | ns |
| DIFF_SSTL2_II_T_DCI | 0.94 | 1.09 | 1.08 | 1.53 | 2.26 | 1.68 | 1.53 | 2.26 | 1.68 | ns |
| DIFF_SSTL18_I | 0.94 | 1.09 | 1.08 | 1.58 | 2.22 | 1.73 | 1.58 | 2.22 | 1.73 | ns |
| DIFF_SSTL18_I_DCI | 0.94 | 1.09 | 1.08 | 1.51 | 2.30 | 1.65 | 1.51 | 2.30 | 1.65 | ns |

## Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 6 and Figure 7.

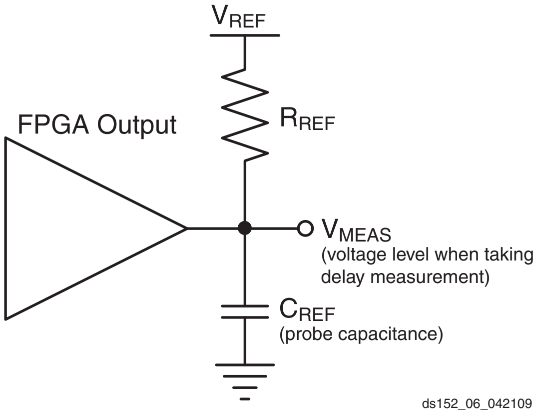

*Figure 6:* **Single Ended Test Setup**

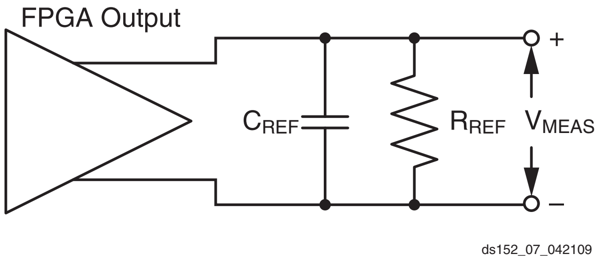

*Figure 7:* **Differential Test Setup**

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. Parameters $V_{REF}$, $R_{REF}$, $C_{REF}$, and $V_{MEAS}$ fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from Table 48.
2. Record the time to $V_{MEAS}$.
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to $V_{MEAS}$.
5. Compare the results of steps 2 and 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

*Table 48:* **Output Delay Measurement Methodology**

| Description | I/O Standard Attribute | $R_{REF}$ ($\Omega$) | $C_{REF}$(1) (pF) | $V_{MEAS}$ (V) | $V_{REF}$ (V) |
|---|---|---|---|---|---|
| LVCMOS, 2.5V | LVCMOS25 | 1M | 0 | 1.25 | 0 |
| LVCMOS, 1.8V | LVCMOS18 | 1M | 0 | 0.9 | 0 |
| LVCMOS, 1.5V | LVCMOS15 | 1M | 0 | 0.75 | 0 |
| LVCMOS, 1.2V | LVCMOS12 | 1M | 0 | 0.75 | 0 |
| HSTL (High-Speed Transceiver Logic), Class I | HSTL_I | 50 | 0 | $V_{REF}$ | 0.75 |
| HSTL, Class II | HSTL_II | 25 | 0 | $V_{REF}$ | 0.75 |
| HSTL, Class III | HSTL_III | 50 | 0 | 0.9 | 1.5 |
| HSTL, Class I, 1.8V | HSTL_I_18 | 50 | 0 | $V_{REF}$ | 0.9 |
| HSTL, Class II, 1.8V | HSTL_II_18 | 25 | 0 | $V_{REF}$ | 0.9 |
| HSTL, Class III, 1.8V | HSTL_III_18 | 50 | 0 | 1.1 | 1.8 |
| SSTL (Stub Series Terminated Logic), Class I, 1.8V | SSTL18_I | 50 | 0 | $V_{REF}$ | 0.9 |
| SSTL, Class II, 1.8V | SSTL18_II | 25 | 0 | $V_{REF}$ | 0.9 |
| SSTL, Class I, 2.5V | SSTL2_I | 50 | 0 | $V_{REF}$ | 1.25 |
| SSTL, Class II, 2.5V | SSTL2_II | 25 | 0 | $V_{REF}$ | 1.25 |
| LVDS (Low-Voltage Differential Signaling), 2.5V | LVDS_25 | 100 | 0 | 0(2) | 1.2 |
| LVDSEXT (LVDS Extended Mode), 2.5V | LVDS_25 | 100 | 0 | 0(2) | 1.2 |
| BLVDS (Bus LVDS), 2.5V | BLVDS_25 | 100 | 0 | 0(2) | 0 |

*Table 50:* **OLOGIC Switching Characteristics**

| Symbol | Description | Speed Grade | | | | | Units |
|---|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 (XC) | -1 (XQ) | -1L | |
| **Setup/Hold** | | | | | | | |
| $T_{ODCK}/T_{OCKD}$ | D1/D2 pins Setup/Hold with respect to CLK | 0.45/<br>–0.08 | 0.50/<br>–0.08 | 0.54/<br>–0.08 | 0.54/<br>–0.08 | 0.69/<br>–0.11 | ns |
| $T_{OOCECK}/T_{OCKOCE}$ | OCE pin Setup/Hold with respect to CLK | 0.17/<br>–0.03 | 0.20/<br>–0.03 | 0.22/<br>–0.03 | 0.27/<br>–0.05 | 0.27/<br>–0.04 | ns |
| $T_{OSRCK}/T_{OCKSR}$ | SR pin Setup/Hold with respect to CLK | 0.59/<br>–0.24 | 0.62/<br>–0.24 | 0.54/<br>–0.08 | 0.54/<br>–0.08 | 0.79/<br>–0.35 | ns |
| $T_{OTCK}/T_{OCKT}$ | T1/T2 pins Setup/Hold with respect to CLK | 0.44/<br>–0.07 | 0.51/<br>–0.07 | 0.56/<br>–0.07 | 0.60/<br>–0.10 | 0.68/<br>–0.13 | ns |
| $T_{OTCECK}/T_{OCKTCE}$ | TCE pin Setup/Hold with respect to CLK | 0.15/<br>–0.04 | 0.19/<br>–0.04 | 0.21/<br>–0.04 | 0.27/<br>–0.05 | 0.29/<br>–0.05 | ns |
| **Combinatorial** | | | | | | | |
| $T_{DOQ}$ | D1 to OQ out or T1 to TQ out | 0.78 | 0.87 | 1.01 | 1.01 | 1.15 | ns |
| **Sequential Delays** | | | | | | | |
| $T_{OCKQ}$ | CLK to OQ/TQ out | 0.54 | 0.61 | 0.71 | 0.71 | 0.80 | ns |
| $T_{RQ}$ | SR pin to OQ/TQ out | 0.80 | 0.90 | 1.05 | 1.05 | 1.19 | ns |
| $T_{GSRQ}$ | Global Set/Reset to Q outputs | 7.60 | 7.60 | 10.51 | 10.51 | 10.51 | ns |
| **Set/Reset** | | | | | | | |
| $T_{RPW}$ | Minimum Pulse Width, SR inputs | 0.78 | 0.95 | 1.20 | 1.20 | 1.30 | ns, Min |

## Input Serializer/Deserializer Switching Characteristics

*Table 51:* **ISERDES Switching Characteristics**

| Symbol | Description | Speed Grade | | | | | Units |
|---|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 (XC) | -1 (XQ) | -1L | |
| **Setup/Hold for Control Lines** | | | | | | | |
| $T_{ISCCK\_BITSLIP}$/ $T_{ISCKC\_BITSLIP}$ | BITSLIP pin Setup/Hold with respect to CLKDIV | 0.07/ 0.15 | 0.08/ 0.16 | 0.09/ 0.17 | 0.09/ 0.17 | 0.14/ 0.17 | ns |
| $T_{ISCCK\_CE}$ / $T_{ISCKC\_CE}$(2) | CE pin Setup/Hold with respect to CLK (for CE1) | 0.20/ 0.03 | 0.25/ 0.04 | 0.27/ 0.04 | 0.27/ 0.04 | 0.31/ 0.05 | ns |
| $T_{ISCCK\_CE2}$ / $T_{ISCKC\_CE2}$(2) | CE pin Setup/Hold with respect to CLKDIV (for CE2) | 0.01/ 0.27 | 0.01 0.29 | 0.01/ 0.31 | 0.01/ 0.31 | –0.05/ 0.35 | ns |
| **Setup/Hold for Data Lines** | | | | | | | |
| $T_{ISDCK\_D}$ /$T_{ISCKD\_D}$ | D pin Setup/Hold with respect to CLK | 0.07/ 0.08 | 0.08/ 0.09 | 0.09/ 0.11 | 0.09/ 0.11 | 0.11/ 0.19 | ns |
| $T_{ISDCK\_DDLY}$ /$T_{ISCKD\_DDLY}$ | DDLY pin Setup/Hold with respect to CLK (using IODELAY)(1) | 0.10/ 0.05 | 0.12/ 0.06 | 0.14/ 0.07 | 0.14/ 0.07 | 0.16/ 0.15 | ns |
| $T_{ISDCK\_D\_DDR}$ /$T_{ISCKD\_D\_DDR}$ | D pin Setup/Hold with respect to CLK at DDR mode | 0.07/ 0.08 | 0.08/ 0.09 | 0.09/ 0.11 | 0.09/ 0.11 | 0.11/ 0.19 | ns |
| $T_{ISDCK\_DDLY\_DDR}$<br>$T_{ISCKD\_DDLY\_DDR}$ | D pin Setup/Hold with respect to CLK at DDR mode (using IODELAY)(1) | 0.10/ 0.05 | 0.12/ 0.06 | 0.14/ 0.07 | 0.14/ 0.07 | 0.16/ 0.15 | ns |
| **Sequential Delays** | | | | | | | |
| $T_{ISCKO\_Q}$ | CLKDIV to out at Q pin | 0.57 | 0.66 | 0.75 | 0.80 | 0.88 | ns |
| **Propagation Delays** | | | | | | | |
| $T_{ISDO\_DO}$ | D input to DO output pin | 0.19 | 0.22 | 0.25 | 0.25 | 0.28 | ns |

**Notes:**

1. Recorded at 0 tap value.
2. $T_{ISCCK\_CE2}$ and $T_{ISCKC\_CE2}$ are reported as $T_{ISCCK\_CE}$/$T_{ISCKC\_CE}$ in TRACE report.

*Table 57:* **Block RAM and FIFO Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 | -1L | |
| $T_{RCCK\_WE}/T_{RCKC\_WE}$ | Write Enable (WE) input (Block RAM only) | 0.44/<br>0.19 | 0.47/<br>0.25 | 0.52/<br>0.35 | 0.67/<br>0.24 | ns, Min |
| $T_{RCCK\_WREN}/T_{RCKC\_WREN}$ | WREN FIFO inputs | 0.47/<br>0.26 | 0.50/<br>0.27 | 0.55/<br>0.30 | 0.68/<br>0.31 | ns, Min |
| $T_{RCCK\_RDEN}/T_{RCKC\_RDEN}$ | RDEN FIFO inputs | 0.46/<br>0.26 | 0.50/<br>0.27 | 0.55/<br>0.30 | 0.67/<br>0.31 | ns, Min |
| **Reset Delays** | | | | | | |
| $T_{RCO\_FLAGS}$ | Reset RST to FIFO Flags/Pointers(10) | 0.90 | 0.98 | 1.10 | 1.23 | ns, Max |
| $T_{RCCK\_RSTREG}/T_{RCKC\_RSTREG}$ | FIFO reset timing(11) | 0.22/<br>0.23 | 0.24/<br>0.24 | 0.28/<br>0.26 | 0.31/<br>0.27 | ns, Min |
| **Maximum Frequency** | | | | | | |
| $F_{MAX}$ | Block RAM in TDP and SDP modes (Write First and No Change modes) | 600 | 540 | 450 | 340 | MHz |
| | Block RAM (Read First mode) | 525 | 475 | 400 | 275 | MHz |
| | Block RAM (SDP mode)(12) | 525 | 475 | 400 | 275 | MHz |
| $F_{MAX\_CASCADE}$ | Block RAM Cascade (Write First and No Change modes) | 550 | 490 | 400 | 300 | MHz |
| | Block RAM Cascade (Read First mode) | 475 | 425 | 350 | 235 | MHz |
| $F_{MAX\_FIFO}$ | FIFO in all modes | 600 | 540 | 450 | 340 | MHz |
| $F_{MAX\_ECC}$ | Block RAM and FIFO in ECC configuration | 450 | 400 | 325 | 250 | MHz |

**Notes:**

1. TRACE will report all of these parameters as $T_{RCKO\_DO}$.
2. $T_{RCKO\_DOR}$ includes $T_{RCKO\_DOW}$, $T_{RCKO\_DOPR}$, and $T_{RCKO\_DOPW}$ as well as the B port equivalent timing parameters.
3. These parameters also apply to synchronous FIFO with DO_REG = 0.
4. $T_{RCKO\_DO}$ includes $T_{RCKO\_DOP}$ as well as the B port equivalent timing parameters.
5. These parameters also apply to multirate (asynchronous) and synchronous FIFO with DO_REG = 1.
6. $T_{RCKO\_FLAGS}$ includes the following parameters: $T_{RCKO\_AEMPTY}$, $T_{RCKO\_AFULL}$, $T_{RCKO\_EMPTY}$, $T_{RCKO\_FULL}$, $T_{RCKO\_RDERR}$, $T_{RCKO\_WRERR}$.
7. $T_{RCKO\_POINTERS}$ includes both $T_{RCKO\_RDCOUNT}$ and $T_{RCKO\_WRCOUNT}$.
8. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
9. $T_{RCKO\_DI}$ includes both A and B inputs as well as the parity inputs of A and B.
10. $T_{RCO\_FLAGS}$ includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
11. The FIFO reset must be asserted for at least three positive clock edges.
12. When using ISE software v12.4 or later, if the RDADDR_COLLISION_HWCONFIG attribute is set to PERFORMANCE or the block RAM is in single-port operation, then the faster $F_{MAX}$ for WRITE_FIRST/NO_CHANGE modes apply.

## DSP48E1 Switching Characteristics

*Table 58:* **DSP48E1 Switching Characteristics**

| Symbol | Description | Speed Grade | | | | | Units |
|---|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 (XC) | -1 (XQ) | -1L | |
| **Setup and Hold Times of Data/Control Pins to the Input Register Clock** | | | | | | | |
| $T_{\text{DSPDCK\_\{A, ACIN; B, BCIN\}\_\{AREG; BREG\}}}$/ $T_{\text{DSPCKD\_\{A, ACIN; B, BCIN\}\_\{AREG; BREG\}}}$ | {A, ACIN, B, BCIN} input to {A, B} register CLK | 0.25/ 0.27 | 0.29/ 0.30 | 0.35/ 0.34 | 0.36/ 0.34 | 0.46/ 0.39 | ns |
| $T_{\text{DSPDCK\_C\_CREG}}$/$T_{\text{DSPCKD\_C\_CREG}}$ | C input to C register CLK | 0.16/ 0.20 | 0.19/ 0.22 | 0.22/ 0.24 | 0.25/ 0.24 | 0.33/ 0.30 | ns |
| $T_{\text{DSPDCK\_D\_DREG}}$/$T_{\text{DSPCKD\_D\_DREG}}$ | D input to D register CLK | 0.07/ 0.31 | 0.10/ 0.34 | 0.15/ 0.39 | 0.16/ 0.39 | 0.24/ 0.45 | ns |
| **Setup and Hold Times of Data Pins to the Pipeline Register Clock** | | | | | | | |
| $T_{\text{DSPDCK\_\{A, ACIN, B, BCIN\}\_MREG\_MULT}}$/ $T_{\text{DSPCKD\_\{A, ACIN, B, BCIN\}\_MREG\_MULT}}$ | {A, ACIN, B, BCIN} input to M register CLK | 2.36/ 0.04 | 2.70/ 0.04 | 3.21/ 0.04 | 3.21/ 0.04 | 3.66/ 0.02 | ns |
| $T_{\text{DSPDCK\_\{A, D\}\_ADREG}}$/ $T_{\text{DSPCKD\_\{A, D\}\_ADREG}}$ | {A, D} input to AD register CLK | 1.24/ 0.10 | 1.42/ 0.12 | 1.69/ 0.13 | 1.69/ 0.13 | 1.91/ 0.16 | ns |
| **Setup and Hold Times of Data/Control Pins to the Output Register Clock** | | | | | | | |
| $T_{\text{DSPDCK\_\{A, ACIN, B, BCIN\}\_PREG\_MULT}}$/ $T_{\text{DSPCKD\_\{A, ACIN, B, BCIN\}\_PREG\_MULT}}$ | {A, ACIN, B, BCIN} input to P register CLK using multiplier | 3.83/ –0.13 | 4.37/ –0.13 | 5.20/ –0.13 | 5.20/ –0.13 | 5.94/ –0.24 | ns |
| $T_{\text{DSPDCK\_D\_PREG\_MULT}}$/ $T_{\text{DSPCKD\_D\_PREG\_MULT}}$ | D input to P register CLK | 3.62/ –0.47 | 4.13/ –0.47 | 4.90/ –0.47 | 4.90/ –0.47 | 5.61/ –0.77 | ns |
| $T_{\text{DSPDCK\_\{A, ACIN, B, BCIN\}\_PREG}}$/ $T_{\text{DSPCKD\_\{A, ACIN, B, BCIN\}\_PREG}}$ | {A, ACIN, B, BCIN} input to P register CLK not using multiplier | 1.59/ –0.13 | 1.81/ –0.13 | 2.15/ –0.13 | 2.15/ –0.13 | 2.44/ –0.24 | ns |
| $T_{\text{DSPDCK\_C\_PREG}}$/ $T_{\text{DSPCKD\_C\_PREG}}$ | C input to P register CLK | 1.42/ –0.10 | 1.61/ –0.10 | 1.91/ –0.10 | 1.91/ –0.10 | 2.16/ –0.19 | ns |
| $T_{\text{DSPDCK\_\{PCIN, CARRYCASCIN, MULTSIGNIN\}\_PREG}}$/ $T_{\text{DSPCKD\_\{PCIN, CARRYCASCIN, MULTSIGNIN\}\_PREG}}$ | {PCIN, CARRYCASCIN, MULTSIGNIN} input to P register CLK | 1.23/ –0.02 | 1.41/ –0.02 | 1.67/ –0.02 | 1.67/ –0.02 | 1.91/ –0.07 | ns |
| **Setup and Hold Times of the CE Pins** | | | | | | | |
| $T_{\text{DSPDCK\_\{CEA; CEB\}\_\{AREG; BREG\}}}$/ $T_{\text{DSPCKD\_\{CEA; CEB\}\_\{AREG; BREG\}}}$ | {CEA; CEB} input to {A; B} register CLK | 0.14/ 0.19 | 0.17/ 0.22 | 0.22/ 0.25 | 0.22/ 0.25 | 0.30/ 0.28 | ns |
| $T_{\text{DSPDCK\_CEC\_CREG}}$/ $T_{\text{DSPCKD\_CEC\_CREG}}$ | CEC input to C register CLK | 0.15/ 0.18 | 0.18/ 0.20 | 0.24/ 0.23 | 0.24/ 0.23 | 0.31/ 0.26 | ns |
| $T_{\text{DSPDCK\_CED\_DREG}}$/ $T_{\text{DSPCKD\_CED\_DREG}}$ | CED input to D register CLK | 0.20/ 0.12 | 0.24/ 0.13 | 0.31/ 0.14 | 0.31/ 0.14 | 0.43/ 0.16 | ns |
| $T_{\text{DSPDCK\_CEM\_MREG}}$/ $T_{\text{DSPCKD\_CEM\_MREG}}$ | CEM input to M register CLK | 0.16/ 0.19 | 0.20/ 0.21 | 0.26/ 0.25 | 0.26/ 0.25 | 0.32/ 0.28 | ns |
| $T_{\text{DSPDCK\_CEP\_PREG}}$/ $T_{\text{DSPCKD\_CEP\_PREG}}$ | CEP input to P register CLK | 0.32/ 0.02 | 0.38/ 0.02 | 0.46/ 0.03 | 0.46/ 0.03 | 0.54/ 0.04 | ns |
| **Setup and Hold Times of the RST Pins** | | | | | | | |
| $T_{\text{DSPDCK\_\{RSTA; RSTB\}\_\{AREG; BREG\}}}$/ $T_{\text{DSPCKD\_\{RSTA; RSTB\}\_\{AREG; BREG\}}}$ | {RSTA, RSTB} input to {A, B} register CLK | 0.27/ 0.17 | 0.31/ 0.19 | 0.38/ 0.22 | 0.38/ 0.22 | 0.41/ 0.25 | ns |
| $T_{\text{DSPDCK\_RSTC\_CREG}}$/ $T_{\text{DSPCKD\_RSTC\_CREG}}$ | RSTC input to C register CLK | 0.18/ 0.08 | 0.20/ 0.08 | 0.23/ 0.09 | 0.23/ 0.09 | 0.27/ 0.11 | ns |
| $T_{\text{DSPDCK\_RSTD\_DREG}}$/ $T_{\text{DSPCKD\_RSTD\_DREG}}$ | RSTD input to D register CLK | 0.28/ 0.15 | 0.32/ 0.16 | 0.38/ 0.19 | 0.38/ 0.19 | 0.45/ 0.21 | ns |
| $T_{\text{DSPDCK\_RSTM\_MREG}}$/ $T_{\text{DSPCKD\_RSTM\_MREG}}$ | RSTM input to M register CLK | 0.20/ 0.24 | 0.23/ 0.26 | 0.26/ 0.30 | 0.26/ 0.30 | 0.29/ 0.34 | ns |

*Table 58:* **DSP48E1 Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | | | Units |
|---|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 (XC) | -1 (XQ) | -1L | |
| **Maximum Frequency** | | | | | | | |
| $F_{MAX}$ | With all registers used | 600 | 540 | 450 | 450 | 410 | MHz |
| $F_{MAX\_PATDET}$ | With pattern detector | 551 | 483 | 408 | 408 | 356 | MHz |
| $F_{MAX\_MULT\_NOMREG}$ | Two register multiply without MREG | 356 | 311 | 262 | 262 | 224 | MHz |
| $F_{MAX\_MULT\_NOMREG\_PATDET}$ | Two register multiply without MREG with pattern detect | 327 | 286 | 241 | 241 | 211 | MHz |
| $F_{MAX\_PREADD\_MULT\_NOADREG}$ | Without ADREG | 398 | 347 | 292 | 292 | 254 | MHz |
| $F_{MAX\_PREADD\_MULT\_NOADREG\_PATDET}$ | Without ADREG with pattern detect | 398 | 347 | 292 | 292 | 254 | MHz |
| $F_{MAX\_NOPIPELINEREG}$ | Without pipeline registers (MREG, ADREG) | 266 | 233 | 196 | 196 | 171 | MHz |
| $F_{MAX\_NOPIPELINEREG\_PATDET}$ | Without pipeline registers (MREG, ADREG) with pattern detect | 250 | 219 | 184 | 184 | 160 | MHz |

## Configuration Switching Characteristics

*Table 59:* **Configuration Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 | -1L | |
| **Power-up Timing Characteristics** | | | | | | |
| $T_{PL}$(1) | Program Latency | 5 | 5 | 5 | 5 | ms, Max |
| $T_{POR}$(1) | Power-on-Reset | 15/55 | 15/55 | 15/55 | 15/60 | ms, Min/Max |
| $T_{ICCK}$ | CCLK (output) delay | 400 | 400 | 400 | 400 | ns, Min |
| $T_{PROGRAM}$ | Program Pulse Width | 250 | 250 | 250 | 250 | ns, Min |
| **Master/Slave Serial Mode Programming Switching** | | | | | | |
| $T_{DCCK}/T_{CCKD}$ | DIN Setup/Hold, slave mode | 4.0/0.0 | 4.0/0.0 | 4.0/0.0 | 4.5/0.0 | ns, Min |
| $T_{DSCCK}/T_{SCCKD}$ | DIN Setup/Hold, master mode | 4.0/0.0 | 4.0/0.0 | 4.0/0.0 | 5.0/0.0 | ns, Min |
| $T_{CCO}$ | DOUT at 2.5V | 6 | 6 | 6 | 7 | ns, Max |
| | DOUT at 1.8V | 6 | 6 | 6 | 7 | ns, Max |
| $F_{MCCK}$ | Maximum CCLK frequency, serial modes | 105 | 105 | 105 | 70 | MHz, Max |
| $F_{MCCKTOL}$ | Frequency Tolerance, master mode with respect to nominal CCLK. | 55 | 55 | 55 | 60 | % |
| $F_{MSCCK}$ | Slave mode external CCLK | 100 | 100 | 100 | 100 | MHz |
| **SelectMAP Mode Programming Switching** | | | | | | |
| $T_{SMDCCK}/T_{SMCCKD}$ | SelectMAP Data Setup/Hold | 4.0/0.0 | 4.0/0.0 | 4.0/0.0 | 5.5/0.0 | ns, Min |
| $T_{SMCSCCK}/T_{SMCCKCS}$ | CSI_B Setup/Hold | 4.0/0.0 | 4.0/0.0 | 4.0/0.0 | 5.5/0.0 | ns, Min |
| $T_{SMCCKW}/T_{SMWCCK}$ | RDWR_B Setup/Hold | 10.0/0.0 | 10.0/0.0 | 10.0/0.0 | 16.0/0.0 | ns, Min |
| $T_{SMCKCSO}$ | CSO_B clock to out<br>(330 Ω pull-up resistor required) | 6 | 6 | 6 | 7 | ns, Max |
| $T_{SMCO}$ | CCLK to DATA out in readback at 2.5V | 6 | 6 | 6 | 7 | ns, Max |
| | CCLK to DATA out in readback at 1.8V | 6 | 6 | 6 | 7 | ns, Max |

*Table 59:* **Configuration Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 | -1L | |
| $T_{MMCMDCK\_DI}$/ $T_{MMCMCKD\_DI}$ | DI Setup/Hold | 1.25/ 0.00 | 1.40/ 0.00 | 1.63/ 0.00 | 1.64/ 0.00 | ns |
| $T_{MMCMDCK\_DEN}$/ $T_{MMCMCKD\_DEN}$ | DEN Setup/Hold time | 1.25/ 0.00 | 1.40/ 0.00 | 1.63/ 0.00 | 1.64/ 0.00 | ns |
| $T_{MMCMDCK\_DWE}$/ $T_{MMCMCKD\_DWE}$ | DWE Setup/Hold time | 1.25/ 0.00 | 1.40/ 0.00 | 1.63/ 0.00 | 1.64/ 0.00 | ns |
| $T_{MMCMCKO\_DO}$ | CLK to out of DO(3) | 2.60 | 3.02 | 3.64 | 3.68 | ns |
| $T_{MMCMCKO\_DRDY}$ | CLK to out of DRDY | 0.32 | 0.34 | 0.38 | 0.38 | ns |

**Notes:**

1. To support longer delays in configuration, use the design solutions described in UG360: *Virtex-6 FPGA Configuration User Guide*.
2. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.
3. DO will hold until next DRP operation.

## Clock Buffers and Networks

*Table 60:* **Global Clock Switching Characteristics (Including BUFGCTRL)**

| Symbol | Description | Devices | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1 | -1L | |
| $T_{BCCCK\_CE}$/$T_{BCCKC\_CE}$(1) | CE pins Setup/Hold | All | 0.11/ 0.00 | 0.13/ 0.00 | 0.16/ 0.00 | 0.13/ 0.00 | ns |
| $T_{BCCCK\_S}$/$T_{BCCKC\_S}$(1) | S pins Setup/Hold | All | 0.11/ 0.00 | 0.13/ 0.00 | 0.16/ 0.00 | 0.13/ 0.00 | ns |
| $T_{BCCKO\_O}$(2) | BUFGCTRL delay from I0/I1 to O | All | 0.07 | 0.08 | 0.10 | 0.10 | ns |
| **Maximum Frequency** | | | | | | | |
| $F_{MAX}$ | Global clock tree (BUFG) | All except LX760 | 800 | 750 | 700 | 667 | MHz |
| | | LX760 | N/A | 700 | 700 | 667 | MHz |

**Notes:**

1. $T_{BCCCK\_CE}$ and $T_{BCCKC\_CE}$ must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX_VIRTEX4 primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. $T_{BGCKO\_O}$ (BUFG delay from I0 to O) values are the same as $T_{BCCKO\_O}$ values.

*Table 61:* **Input/Output Clock Switching Characteristics (BUFIO)**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 | -1L | |
| $T_{BIOCKO\_O}$ | Clock to out delay from I to O | 0.14 | 0.16 | 0.18 | 0.21 | ns |
| **Maximum Frequency** | | | | | | |
| $F_{MAX}$ | I/O clock tree (BUFIO) | 800 | 800 | 710 | 710 | MHz |

*Table 62:* **Regional Clock Switching Characteristics (BUFR)**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 | -1L | |
| $T_{BRCKO\_O}$ | Clock to out delay from I to O | 0.56 | 0.62 | 0.73 | 0.82 | ns |
| $T_{BRCKO\_O\_BYP}$ | Clock to out delay from I to O with Divide Bypass attribute set | 0.28 | 0.31 | 0.36 | 0.41 | ns |

## Clock Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-6 FPGA clock transmitter and receiver data-valid windows.

*Table 71:* **Duty Cycle Distortion and Clock-Tree Skew**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1 | -1L | |
| $T_{DCD\_CLK}$ | Global Clock Tree Duty Cycle Distortion(1) | All | 0.12 | 0.12 | 0.12 | 0.12 | ns |
| $T_{CKSKEW}$ | Global Clock Tree Skew(2) | XC6VLX75T | 0.15 | 0.16 | 0.18 | 0.17 | ns |
| | | XC6VLX130T | 0.25 | 0.26 | 0.29 | 0.28 | ns |
| | | XC6VLX195T | 0.26 | 0.27 | 0.31 | 0.30 | ns |
| | | XC6VLX240T | 0.26 | 0.27 | 0.31 | 0.30 | ns |
| | | XC6VLX365T | 0.28 | 0.29 | 0.31 | 0.31 | ns |
| | | XC6VLX550T | N/A | 0.50 | 0.54 | 0.54 | ns |
| | | XC6VLX760 | N/A | 0.51 | 0.56 | 0.56 | ns |
| | | XC6VSX315T | 0.27 | 0.28 | 0.32 | 0.30 | ns |
| | | XC6VSX475T | N/A | 0.39 | 0.44 | 0.42 | ns |
| | | XC6VHX250T | 0.25 | 0.26 | 0.29 | N/A | ns |
| | | XC6VHX255T | 0.35 | 0.37 | 0.41 | N/A | ns |
| | | XC6VHX380T | 0.45 | 0.47 | 0.52 | N/A | ns |
| | | XC6VHX565T | N/A | 0.46 | 0.51 | N/A | ns |
| | | XQ6VLX130T | N/A | 0.26 | 0.29 | 0.28 | ns |
| | | XQ6VLX240T | N/A | 0.27 | 0.31 | 0.30 | ns |
| | | XQ6VLX550T | N/A | N/A | 0.54 | 0.54 | ns |
| | | XQ6VSX315T | N/A | 0.28 | 0.32 | 0.30 | ns |
| | | XQ6VSX475T | N/A | N/A | 0.44 | 0.42 | ns |
| $T_{DCD\_BUFIO}$ | I/O clock tree duty cycle distortion | All | 0.08 | 0.08 | 0.08 | 0.08 | ns |
| $T_{BUFIOSKEW}$ | I/O clock tree skew across one clock region | All | 0.03 | 0.03 | 0.03 | 0.02 | ns |
| $T_{BUFIOSKEW2}$ | I/O clock tree skew across three clock regions | All | 0.10 | 0.12 | 0.23 | 0.12 | ns |
| $T_{DCD\_BUFR}$ | Regional clock tree duty cycle distortion | All | 0.15 | 0.15 | 0.15 | 0.15 | ns |

**Notes:**

1. These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
2. The $T_{CKSKEW}$ value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

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