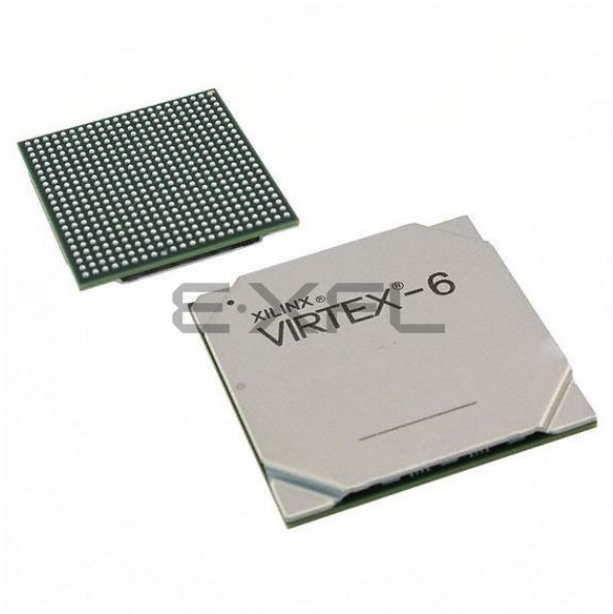
AMD Xilinx - XC6VSX475T-1FFG1759C Datasheet



Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	37200
Number of Logic Elements/Cells	476160
Total RAM Bits	39223296
Number of I/O	840
Number of Gates	-
Voltage - Supply	0.95V ~ 1.05V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1759-BBGA, FCBGA
Supplier Device Package	1759-FCBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6vsx475t-1ffg1759c

LVPECL DC Specifications (LVPECL_25)

These values are valid when driving a 100Ω differential load only, i.e., a 100Ω resistor between the two receiver pins. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. Table 11 summarizes the DC output specifications of LVPECL. For more information on using LVPECL, see UG361: *Virtex-6 FPGA SelectIO Resources User Guide*.

Table 11: **LVPECL DC Specifications**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{OH}	Output High Voltage	V_{CC} – 1.025	1.545	V_{CC} – 0.88	V
V_{OL}	Output Low Voltage	V_{CC} – 1.81	0.795	V_{CC} – 1.62	V
V_{ICM}	Input Common-Mode Voltage	0.6	–	2.2	V
V_{IDIFF}	Differential Input Voltage(1)(2)	0.100	–	1.5	V

Notes:

1. Recommended input maximum voltage not to exceed V_{CCAUX} + 0.2V.
2. Recommended input minimum voltage not to go below –0.5V.

eFUSE Read Endurance

Table 12 lists the maximum number of read cycle operations expected. For more information, see UG360: *Virtex-6 FPGA Configuration User Guide*.

Table 12: **eFUSE Read Endurance**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
DNA_CYCLES	Number of DNA_PORT READ operations or JTAG ISC_DNA read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles
AES_CYCLES	Number of JTAG FUSE_KEY or FUSE_CNTL read command operations. Unaffected by SHIFT operations.	30,000,000				Read Cycles

GTX Transceiver Specifications

GTX Transceiver DC Characteristics

Table 13: **Absolute Maximum Ratings for GTX Transceivers(1)**

Symbol	Description	Min	Max	Units
MGTAVCC	Analog supply voltage for the GTX transmitter and receiver circuits relative to GND	–0.5	1.1	V
MGTAVTT	Analog supply voltage for the GTX transmitter and receiver termination circuits relative to GND	–0.5	1.32	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	–0.5	1.32	V
V_{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	–0.5	1.32	V
$V_{MGTREFCLK}$	Reference clock absolute input voltage	–0.5	1.32	V

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 14: **Recommended Operating Conditions for GTX Transceivers(1)(2)**

Symbol	Description	Speed Grade	PLL Frequency	Min	Typ	Max	Units
MGTAVCC	Analog supply voltage for the GTX transmitter and receiver circuits relative to GND	-3, -2(3)	> 2.7 GHz	1.0	1.03	1.06	V
		-3, -2(3)	≤ 2.7 GHz	0.95	1.0	1.06	V
		-1	≤ 2.7 GHz	0.95	1.0	1.06	V
		-1L	≤ 2.7 GHz	0.95	1.0	1.05	V
MGTAVTT	Analog supply voltage for the GTX transmitter and receiver termination circuits relative to GND	All	–	1.14	1.2	1.26	V
MGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	All	–	1.14	1.2	1.26	V

Notes:

1. Each voltage listed requires the filter circuit described in UG366: *Virtex-6 FPGA GTX Transceivers User Guide*.
2. Voltages are specified for the temperature range of T_j = –40°C to +100°C for all XC devices and T_j = –55°C to +125°C for the XQ devices
3. If a GTX Quad contains transceivers operating with a mixture of PLL frequencies above and below 2.7 GHz, the MGTAVCC voltage supply must be in the range of 1.0V to 1.06V.

Table 15: **GTX Transceiver Supply Current (per Lane) (1)(2)**

Symbol	Description	Typ	Max	Units
$I_{MGTAVTT}$	MGTAVTT supply current for one GTX transceiver	55.9	Note 2	mA
$I_{MGTAVCC}$	MGTAVCC supply current for one GTX transceiver	56.1		mA
$MGTR_{REF}$	Precision reference resistor for internal calibration termination	100.0 ± 1% tolerance		Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C, with a 3.125 Gb/s line rate.
2. Values for currents of other transceiver configurations and conditions can be obtained by using the XPower Estimator (XPE) or XPower Analyzer (XPA) tools.

Table 23: **GTX Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTXTX}	Serial data rate range		0.480	–	F_{GTXMAX}	Gb/s
T_{RTX}	TX Rise time	20%–80%	–	120	–	ps
T_{FTX}	TX Fall time	80%–20%	–	120	–	ps
T_{LLSKEW}	TX lane-to-lane skew(1)		–	–	350	ps
$V_{TXOOBVDPP}$	Electrical idle amplitude		–	–	15	mV
$T_{TXOOBTRANSITION}$	Electrical idle transition time		–	–	75	ns
$TJ_{6.5}$	Total Jitter(2)(3)	6.5 Gb/s	–	–	0.33	UI
$DJ_{6.5}$	Deterministic Jitter(2)(3)		–	–	0.17	UI
$TJ_{5.0}$	Total Jitter(2)(3)	5.0 Gb/s	–	–	0.33	UI
$DJ_{5.0}$	Deterministic Jitter(2)(3)		–	–	0.15	UI
$TJ_{4.25}$	Total Jitter(2)(3)	4.25 Gb/s	–	–	0.33	UI
$DJ_{4.25}$	Deterministic Jitter(2)(3)		–	–	0.14	UI
$TJ_{3.75}$	Total Jitter(2)(3)	3.75 Gb/s	–	–	0.34	UI
$DJ_{3.75}$	Deterministic Jitter(2)(3)		–	–	0.16	UI
$TJ_{3.125}$	Total Jitter(2)(3)	3.125 Gb/s	–	–	0.2	UI
$DJ_{3.125}$	Deterministic Jitter(2)(3)		–	–	0.1	UI
$TJ_{3.125L}$	Total Jitter(2)(3)	3.125 Gb/s(4)	–	–	0.35	UI
$DJ_{3.125L}$	Deterministic Jitter(2)(3)		–	–	0.16	UI
$TJ_{2.5}$	Total Jitter(2)(3)	2.5 Gb/s(5)	–	–	0.20	UI
$DJ_{2.5}$	Deterministic Jitter(2)(3)		–	–	0.08	UI
$TJ_{1.25}$	Total Jitter(2)(3)	1.25 Gb/s(6)	–	–	0.15	UI
$DJ_{1.25}$	Deterministic Jitter(2)(3)		–	–	0.06	UI
TJ_{600}	Total Jitter(2)(3)	600 Mb/s	–	–	0.1	UI
DJ_{600}	Deterministic Jitter(2)(3)		–	–	0.03	UI
TJ_{480}	Total Jitter(2)(3)	480 Mb/s	–	–	0.1	UI
DJ_{480}	Deterministic Jitter(2)(3)		–	–	0.03	UI

Notes:

1. Using same REFCLK input with TXENPMAPHASEALIGN enabled for up to 12 consecutive transmitters (three fully populated GTX Quads).
2. Using PLL_DIVSEL_FB = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. All jitter values are based on a bit-error ratio of $1e^{-12}$.
4. PLL frequency at 1.5625 GHz and OUTDIV = 1.
5. PLL frequency at 2.5 GHz and OUTDIV = 2.
6. PLL frequency at 2.5 GHz and OUTDIV = 4.

Table 24: **GTX Transceiver Receiver Switching Characteristics**

Symbol	Description		Min	Typ	Max	Units
F_{GTXRX}	Serial data rate	RX oversampler not enabled	0.600	–	F_{GTXMAX}	Gb/s
		RX oversampler enabled	0.480	–	0.600	Gb/s
$T_{RXELECIDLE}$	Time for RXELECIDLE to respond to loss or restoration of data		–	75	–	ns
$RX_{OOBVDPP}$	OOB detect threshold peak-to-peak		60	–	150	mV
RX_{SST}	Receiver spread-spectrum tracking(1)	Modulated @ 33 KHz	–5000	–	0	ppm
RX_{RL}	Run length (CID)	Internal AC capacitor bypassed	–	–	512	UI
RX_{PPMTOL}	Data/REFCLK PPM offset tolerance	CDR 2nd-order loop disabled	–200	–	200	ppm
		CDR 2nd-order loop enabled	–2000	–	2000	ppm
SJ Jitter Tolerance(2)						
$JT\_SJ_{6.5}$	Sinusoidal Jitter(3)	6.5 Gb/s	0.44	–	–	UI
$JT\_SJ_{5.0}$	Sinusoidal Jitter(3)	5.0 Gb/s	0.44	–	–	UI
$JT\_SJ_{4.25}$	Sinusoidal Jitter(3)	4.25 Gb/s	0.44	–	–	UI
$JT\_SJ_{3.75}$	Sinusoidal Jitter(3)	3.75 Gb/s	0.44	–	–	UI
$JT\_SJ_{3.125}$	Sinusoidal Jitter(3)	3.125 Gb/s	0.45	–	–	UI
$JT\_SJ_{3.125L}$	Sinusoidal Jitter(3)	3.125 Gb/s(4)	0.45	–	–	UI
$JT\_SJ_{2.5}$	Sinusoidal Jitter(3)	2.5 Gb/s(5)	0.5	–	–	UI
$JT\_SJ_{1.25}$	Sinusoidal Jitter(3)	1.25 Gb/s(6)	0.5	–	–	UI
JT_SJ_{600}	Sinusoidal Jitter(3)	600 Mb/s	0.4	–	–	UI
JT_SJ_{480}	Sinusoidal Jitter(3)	480 Mb/s	0.4	–	–	UI
SJ Jitter Tolerance with Stressed Eye(2)						
$JT\_TJSE_{3.125}$	Total Jitter with Stressed Eye(7)	3.125 Gb/s	0.70	–	–	UI
		5.0 Gb/s	0.70	–	–	UI
$JT\_SJSE_{3.125}$	Sinusoidal Jitter with Stressed Eye(7)	3.125 Gb/s	0.1	–	–	UI
		5.0 Gb/s	0.1	–	–	UI

Notes:

1. Using PLL_RXDIVSEL_OUT = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of $1e^{-12}$.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. PLL frequency at 1.5625 GHz and OUTDIV = 1.
5. PLL frequency at 2.5 GHz and OUTDIV = 2.
6. PLL frequency at 2.5 GHz and OUTDIV = 4.
7. Composite jitter with RX equalizer enabled. DFE disabled.

Figure 4 shows the timing parameters in Table 27.

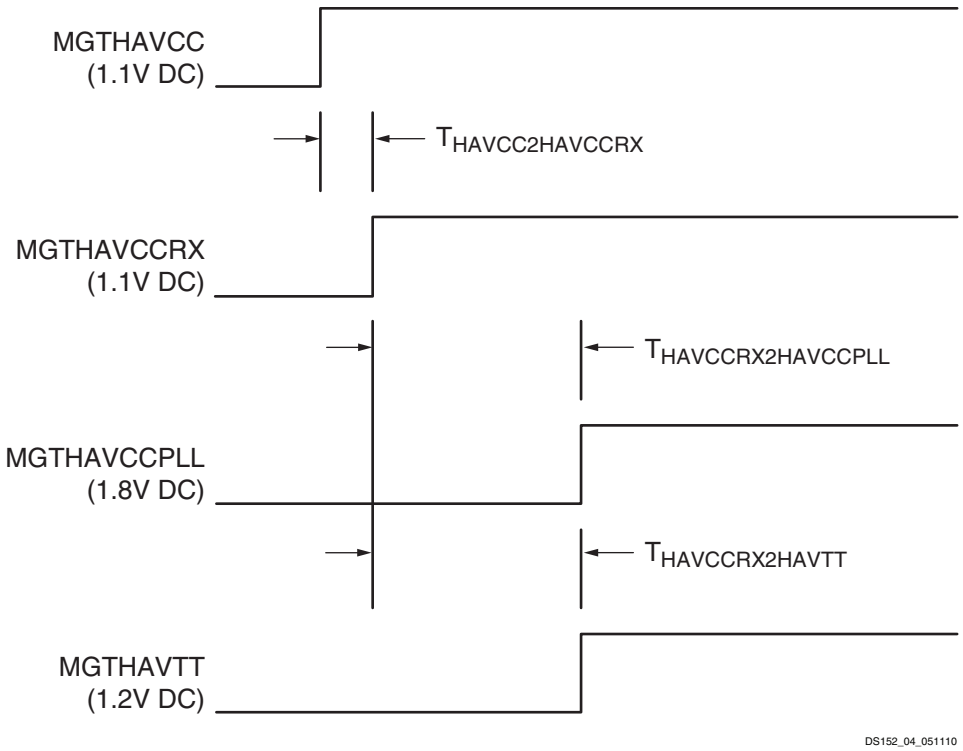


Figure 4: **GTH Transceiver Power Supply Power-On Sequencing**

Table 28: **GTH Transceiver Supply Current**

Symbol	Description	Typ(1)	Max	Units
$I_{MGTHAVCC}$	MGTHAVCC supply current for one GTH Quad (4 lanes)	571	Note 2	mA
$I_{MGTHAVCCRX}$	MGTHAVCCRX supply current for a GTH Quad (4 lanes)	254	Note 2	mA
$I_{MGTHAVTT}$	MGTHAVTT supply current for one GTH Quad (4 lanes)	93	Note 2	mA
$I_{MGTHAVCCPLL}$	MGTHAVCCPLL supply current for one GTH Quad (4 lanes)	219	Note 2	mA
$MGTR_{REF}$	Precision reference resistor for internal calibration termination	1000.0 ± 1% tolerance		Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C, with a 10.3125 Gb/s line rate.
2. Values for currents other than the values specified in this table can be obtained by using the XPower Estimator (XPE) or XPower Analyzer (XPA) tools.

Table 29: **GTH Transceiver Quiescent Supply Current(1)(2)**

Symbol	Description	Typ(3)	Max	Units
$I_{MGTHAVCCQ}$	Quiescent MGTHAVCC Supply Current for one GTH Quad (4 lanes)	65	Note 4	mA
$I_{MGTHAVCCRXQ}$	Quiescent MGTHAVCCRX Supply Current for one GTH Quad (4 lanes)	17	Note 4	mA
$I_{MGTHAVTTQ}$	Quiescent MGTHAVTT Supply Current for one GTH Quad (4 lanes)	1	Note 4	mA
$I_{MGTHAVCCPLLQ}$	Quiescent MGTHAVCCPLL Supply Current for one GTH Quad (4 lanes)	1	Note 4	mA

Notes:

1. Device powered and unconfigured.
2. GTH transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTH transceivers.
3. Typical values are specified at nominal voltage, 25°C.
4. Currents for conditions other than values specified in this table can be obtained by using the XPE or XPA tools.

Table 35: **GTH Transceiver User Clock Switching Characteristics (1)**

Symbol	Description	Conditions	Speed Grade			Units
			-3	-2	-1	
F_{TXOUT}	TXUSERCLKOUT maximum frequency		350	350	323	MHz
F_{RXOUT}	RXUSERCLKOUT maximum frequency		350	350	323	MHz
F_{TXIN}	TXUSERCLKIN maximum frequency	16-bit data path	350	350	323	MHz
		20-bit data path	280	280	258	MHz
		32-bit data path	350	350	323	MHz
		40-bit data path	280	280	258	MHz
		64-bit data path	175	175	162	MHz
		80-bit data path	140	140	129	MHz
		64B/66B-bit data path	170	170	157	MHz
F_{RXIN}	RXUSERCLKIN maximum frequency	16-bit data path	350	350	323	MHz
		20-bit data path	280	280	258	MHz
		32-bit data path	350	350	323	MHz
		40-bit data path	280	280	258	MHz
		64-bit data path	175	175	162	MHz
		80-bit data path	140	140	129	MHz
		64B/66B-bit data path	170	170	157	MHz

Notes:

1. Clocking must be implemented as described in UG371:*Virtex-6 FPGA GTH Transceivers User Guide*.

Table 36: **GTH Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
T_{RTX}	TX Rise time	20%–80%	–	50(3)	–	ps
T_{FTX}	TX Fall time	80%–20%	–	50(3)	–	ps
T_{LLSKEW}	TX lane-to-lane skew	within one GTH Quad	–	–	300	ps
Transmitter Output Jitter(1)(2)						
$TJ_{11.18}$	Total Jitter	11.181 Gb/s	–	–	0.280	UI
$DJ_{11.18}$	Deterministic Jitter		–	–	0.170	UI
$TJ_{10.3125}$	Total Jitter	10.3125 Gb/s	–	–	0.280	UI
$DJ_{10.3125}$	Deterministic Jitter		–	–	0.170	UI
$TJ_{9.953}$	Total Jitter	9.953 Gb/s	–	–	0.280	UI
$DJ_{9.953}$	Deterministic Jitter		–	–	0.170	UI
$TJ_{2.667}$	Total Jitter	2.667 Gb/s	–	–	0.110	UI
$DJ_{2.667}$	Deterministic Jitter		–	–	0.060	UI
$TJ_{2.488}$	Total Jitter	2.488 Gb/s	–	–	0.110	UI
$DJ_{2.488}$	Deterministic Jitter		–	–	0.060	UI

Notes:

1. These values are NOT intended for protocol specific compliance determinations.
2. All jitter values are based on a bit-error ratio of $1e^{-12}$.
3. Rise and fall times are specified at the transmitter package balls.

Switching Characteristics

All values represented in this data sheet are based on these speed specifications: v1.17 for -3, -2, and -1; and v1.10 for -1L. Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device.

Table 42 correlates the current status of each Virtex-6 device on a per speed grade basis.

Table 42: **Virtex-6 Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC6VLX75T			-3, -2, -1, -1L
XC6VLX130T			-3, -2, -1, -1L
XC6VLX195T			-3, -2, -1, -1L
XC6VLX240T			-3, -2, -1, -1L
XC6VLX365T			-3, -2, -1, -1L
XC6VLX550T			-2, -1, -1L
XC6VLX760			-2, -1, -1L
XC6VSX315T			-3, -2, -1, -1L
XC6VSX475T			-2, -1, -1L
XC6VHX250T			-3, -2, -1
XC6VHX255T			-3, -2, -1
XC6VHX380T			-3, -2, -1
XC6VHX565T			-2, -1
XQ6VLX130T			-2, -1, -1L
XQ6VLX240T			-2, -1, -1L
XQ6VLX550T			-1, -1L
XQ6VSX315T			-2, -1, -1L
XQ6VSX475T			-1, -1L

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-6 devices.

Table 44: **IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
LVCMOS25, Fast, 24 mA	0.51	0.57	0.66	0.70	1.66	1.79	1.99	1.96	1.66	1.79	1.99	1.96	ns
LVCMOS18, Slow, 2 mA	0.55	0.61	0.71	0.73	4.21	4.47	4.87	4.30	4.21	4.47	4.87	4.30	ns
LVCMOS18, Slow, 4 mA	0.55	0.61	0.71	0.73	2.79	2.96	3.21	2.94	2.79	2.96	3.21	2.94	ns
LVCMOS18, Slow, 6 mA	0.55	0.61	0.71	0.73	2.30	2.43	2.64	2.47	2.30	2.43	2.64	2.47	ns
LVCMOS18, Slow, 8 mA	0.55	0.61	0.71	0.73	2.01	2.11	2.27	2.24	2.01	2.11	2.27	2.24	ns
LVCMOS18, Slow, 12 mA	0.55	0.61	0.71	0.73	1.88	1.99	2.15	2.10	1.88	1.99	2.15	2.10	ns
LVCMOS18, Slow, 16 mA	0.55	0.61	0.71	0.73	1.84	1.95	2.11	2.04	1.84	1.95	2.11	2.04	ns
LVCMOS18, Fast, 2 mA	0.55	0.61	0.71	0.73	4.00	4.23	4.57	4.08	4.00	4.23	4.57	4.08	ns
LVCMOS18, Fast, 4 mA	0.55	0.61	0.71	0.73	2.62	2.76	2.97	2.74	2.62	2.76	2.97	2.74	ns
LVCMOS18, Fast, 6 mA	0.55	0.61	0.71	0.73	2.15	2.28	2.46	2.32	2.15	2.28	2.46	2.32	ns
LVCMOS18, Fast, 8 mA	0.55	0.61	0.71	0.73	1.90	1.99	2.13	2.14	1.90	1.99	2.13	2.14	ns
LVCMOS18, Fast, 12 mA	0.55	0.61	0.71	0.73	1.69	1.80	1.97	1.88	1.69	1.80	1.97	1.88	ns
LVCMOS18, Fast, 16 mA	0.55	0.61	0.71	0.73	1.63	1.74	1.91	1.88	1.63	1.74	1.91	1.88	ns
LVCMOS15, Slow, 2 mA	0.64	0.73	0.85	0.85	3.43	3.77	4.29	3.91	3.43	3.77	4.29	3.91	ns
LVCMOS15, Slow, 4 mA	0.64	0.73	0.85	0.85	2.58	2.79	3.10	2.93	2.58	2.79	3.10	2.93	ns
LVCMOS15, Slow, 6 mA	0.64	0.73	0.85	0.85	2.08	2.32	2.68	2.50	2.08	2.32	2.68	2.50	ns
LVCMOS15, Slow, 8 mA	0.64	0.73	0.85	0.85	1.81	1.98	2.23	2.24	1.81	1.98	2.23	2.24	ns
LVCMOS15, Slow, 12 mA	0.64	0.73	0.85	0.85	1.76	1.91	2.13	2.07	1.76	1.91	2.13	2.07	ns
LVCMOS15, Slow, 16 mA	0.64	0.73	0.85	0.85	1.69	1.83	2.04	1.98	1.69	1.83	2.04	1.98	ns
LVCMOS15, Fast, 2 mA	0.64	0.73	0.85	0.85	3.44	3.77	4.28	3.91	3.44	3.77	4.28	3.91	ns
LVCMOS15, Fast, 4 mA	0.64	0.73	0.85	0.85	2.37	2.53	2.78	2.66	2.37	2.53	2.78	2.66	ns
LVCMOS15, Fast, 6 mA	0.64	0.73	0.85	0.85	1.80	2.05	2.42	2.16	1.80	2.05	2.42	2.16	ns
LVCMOS15, Fast, 8 mA	0.64	0.73	0.85	0.85	1.76	1.90	2.11	2.04	1.76	1.90	2.11	2.04	ns
LVCMOS15, Fast, 12 mA	0.64	0.73	0.85	0.85	1.64	1.77	1.97	1.90	1.64	1.77	1.97	1.90	ns
LVCMOS15, Fast, 16 mA	0.64	0.73	0.85	0.85	1.62	1.76	1.96	1.92	1.62	1.76	1.96	1.92	ns
LVCMOS12, Slow, 2 mA	0.72	0.81	0.93	0.95	3.14	3.39	3.75	3.54	3.14	3.39	3.75	3.54	ns
LVCMOS12, Slow, 4 mA	0.72	0.81	0.93	0.95	2.43	2.63	2.93	2.79	2.43	2.63	2.93	2.79	ns
LVCMOS12, Slow, 6 mA	0.72	0.81	0.93	0.95	1.92	2.11	2.41	2.26	1.92	2.11	2.41	2.26	ns
LVCMOS12, Slow, 8 mA	0.72	0.81	0.93	0.95	1.87	2.02	2.25	2.17	1.87	2.02	2.25	2.17	ns
LVCMOS12, Fast, 2 mA	0.72	0.81	0.93	0.95	2.71	2.98	3.39	3.11	2.71	2.98	3.39	3.11	ns
LVCMOS12, Fast, 4 mA	0.72	0.81	0.93	0.95	1.93	2.16	2.51	2.31	1.93	2.16	2.51	2.31	ns
LVCMOS12, Fast, 6 mA	0.72	0.81	0.93	0.95	1.75	1.89	2.11	2.05	1.75	1.89	2.11	2.05	ns
LVCMOS12, Fast, 8 mA	0.72	0.81	0.93	0.95	1.69	1.82	2.02	1.98	1.69	1.82	2.02	1.98	ns
LVDCI_25	0.51	0.57	0.66	0.70	2.05	2.14	2.26	2.26	2.05	2.14	2.26	2.26	ns
LVDCI_18	0.55	0.61	0.71	0.73	2.07	2.23	2.47	2.38	2.07	2.23	2.47	2.38	ns
LVDCI_15	0.64	0.73	0.85	0.85	1.85	2.01	2.24	2.18	1.85	2.01	2.24	2.18	ns

Table 45: **IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices *(Cont'd)***

I/O Standard	T_{IOPI}			T_{IOOP}			T_{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
LVCMOS25, Fast, 16 mA	0.57	0.66	0.70	1.92	2.15	2.08	1.92	2.15	2.08	ns
LVCMOS25, Fast, 24 mA	0.57	0.66	0.70	1.79	2.15	1.96	1.79	2.15	1.96	ns
LVCMOS18, Slow, 2 mA	0.61	0.71	0.73	4.47	4.87	4.30	4.47	4.87	4.30	ns
LVCMOS18, Slow, 4 mA	0.61	0.71	0.73	2.96	3.21	2.94	2.96	3.21	2.94	ns
LVCMOS18, Slow, 6 mA	0.61	0.71	0.73	2.43	2.64	2.47	2.43	2.64	2.47	ns
LVCMOS18, Slow, 8 mA	0.61	0.71	0.73	2.11	2.41	2.24	2.11	2.41	2.24	ns
LVCMOS18, Slow, 12 mA	0.61	0.71	0.73	1.99	2.30	2.10	1.99	2.30	2.10	ns
LVCMOS18, Slow, 16 mA	0.61	0.71	0.73	1.95	2.30	2.04	1.95	2.30	2.04	ns
LVCMOS18, Fast, 2 mA	0.61	0.71	0.73	4.23	4.57	4.08	4.23	4.57	4.08	ns
LVCMOS18, Fast, 4 mA	0.61	0.71	0.73	2.76	2.97	2.74	2.76	2.97	2.74	ns
LVCMOS18, Fast, 6 mA	0.61	0.71	0.73	2.28	2.46	2.32	2.28	2.46	2.32	ns
LVCMOS18, Fast, 8 mA	0.61	0.71	0.73	1.99	2.34	2.14	1.99	2.34	2.14	ns
LVCMOS18, Fast, 12 mA	0.61	0.71	0.73	1.80	2.19	1.88	1.80	2.19	1.88	ns
LVCMOS18, Fast, 16 mA	0.61	0.71	0.73	1.74	2.18	1.88	1.74	2.18	1.88	ns
LVCMOS15, Slow, 2 mA	0.73	0.85	0.85	3.77	4.29	3.91	3.77	4.29	3.91	ns
LVCMOS15, Slow, 4 mA	0.73	0.85	0.85	2.79	3.10	2.93	2.79	3.10	2.93	ns
LVCMOS15, Slow, 6 mA	0.73	0.85	0.85	2.32	2.68	2.50	2.32	2.68	2.50	ns
LVCMOS15, Slow, 8 mA	0.73	0.85	0.85	1.98	2.29	2.24	1.98	2.29	2.24	ns
LVCMOS15, Slow, 12 mA	0.73	0.85	0.85	1.91	2.23	2.07	1.91	2.23	2.07	ns
LVCMOS15, Slow, 16 mA	0.73	0.85	0.85	1.83	2.23	1.98	1.83	2.23	1.98	ns
LVCMOS15, Fast, 2 mA	0.73	0.85	0.85	3.77	4.28	3.91	3.77	4.28	3.91	ns
LVCMOS15, Fast, 4 mA	0.73	0.85	0.85	2.53	2.78	2.66	2.53	2.78	2.66	ns
LVCMOS15, Fast, 6 mA	0.73	0.85	0.85	2.05	2.42	2.16	2.05	2.42	2.16	ns
LVCMOS15, Fast, 8 mA	0.73	0.85	0.85	1.90	2.20	2.04	1.90	2.20	2.04	ns
LVCMOS15, Fast, 12 mA	0.73	0.85	0.85	1.77	2.11	1.90	1.77	2.11	1.90	ns
LVCMOS15, Fast, 16 mA	0.73	0.85	0.85	1.76	2.11	1.92	1.76	2.11	1.92	ns
LVCMOS12, Slow, 2 mA	0.81	0.93	0.95	3.39	3.75	3.54	3.39	3.75	3.54	ns
LVCMOS12, Slow, 4 mA	0.81	0.93	0.95	2.63	2.93	2.79	2.63	2.93	2.79	ns
LVCMOS12, Slow, 6 mA	0.81	0.93	0.95	2.11	2.67	2.26	2.11	2.67	2.26	ns
LVCMOS12, Slow, 8 mA	0.81	0.93	0.95	2.02	2.25	2.17	2.02	2.25	2.17	ns
LVCMOS12, Fast, 2 mA	0.81	0.93	0.95	2.98	3.39	3.11	2.98	3.39	3.11	ns
LVCMOS12, Fast, 4 mA	0.81	0.93	0.95	2.16	2.70	2.31	2.16	2.70	2.31	ns
LVCMOS12, Fast, 6 mA	0.81	0.93	0.95	1.89	2.34	2.05	1.89	2.34	2.05	ns
LVCMOS12, Fast, 8 mA	0.81	0.93	0.95	1.82	2.10	1.98	1.82	2.10	1.98	ns
LVDCI_25	0.57	0.70	0.70	2.14	2.82	2.26	2.14	2.82	2.26	ns
LVDCI_18	0.61	0.71	0.73	2.23	2.78	2.38	2.23	2.78	2.38	ns
LVDCI_15	0.73	0.85	0.85	2.01	2.75	2.18	2.01	2.75	2.18	ns
LVDCI_DV2_25	0.57	0.70	0.70	1.83	2.37	2.00	1.83	2.37	2.00	ns

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

Table 47 shows the test setup parameters used for measuring input delay.

Table 47: **Input Delay Measurement Methodology**

Description	I/O Standard Attribute	V_L (1)(2)	V_H (1)(2)	V_{MEAS} (1)(4)(5)	V_{REF} (1)(3)(5)
LVCMOS, 2.5V	LVCMOS25	0	2.5	1.25	–
LVCMOS, 1.8V	LVCMOS18	0	1.8	0.9	–
LVCMOS, 1.5V	LVCMOS15	0	1.5	0.75	–
HSTL (High-Speed Transceiver Logic), Class I & II	HSTL_I, HSTL_II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.75
HSTL, Class III	HSTL_III	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL, Class III 1.8V	HSTL_III_18	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	1.08
SSTL (Stub Terminated Transceiver Logic), Class I & II, 3.3V	SSTL3_I, SSTL3_II	V_{REF} – 1.00	V_{REF} + 1.00	V_{REF}	1.5
SSTL, Class I & II, 2.5V	SSTL2_I, SSTL2_II	V_{REF} – 0.75	V_{REF} + 0.75	V_{REF}	1.25
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	1.2 – 0.125	1.2 + 0.125	0(6)	–
LVDSEXT (LVDS Extended Mode), 2.5V	LVDSEXT_25	1.2 – 0.125	1.2 + 0.125	0(6)	–
HT (HyperTransport), 2.5V	LDT_25	0.6 – 0.125	0.6 + 0.125	0(6)	–

Notes:

1. The input delay measurement methodology parameters for LVDCI are the same for LVCMOS standards of the same voltage. Input delay measurement methodology parameters for HSLVDCI are the same as for HSTL_II standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H.
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 6.
6. The value given is the differential input voltage.

Table 48: **Output Delay Measurement Methodology *(Cont'd)***

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
HT (HyperTransport), 2.5V	LDT_25	100	0	0[2]	0.6
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V	LVPECL_25	100	0	0[2]	0
LVDCI/HSLVDCI, 2.5V	LVDCI_25, HSLVDCI_25	1M	0	1.25	0
LVDCI/HSLVDCI, 1.8V	LVDCI_18, HSLVDCI_18	1M	0	0.9	0
LVDCI/HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	1M	0	0.75	0
HSTL (High-Speed Transceiver Logic), Class I & II, with DCI	HSTL_I_DCI, HSTL_II_DCI	50	0	V_{REF}	0.75
HSTL, Class III, with DCI	HSTL_III_DCI	50	0	0.9	1.5
HSTL, Class I & II, 1.8V, with DCI	HSTL_I_DCI_18, HSTL_II_DCI_18	50	0	V_{REF}	0.9
HSTL, Class III, 1.8V, with DCI	HSTL_III_DCI_18	50	0	1.1	1.8
SSTL (Stub Series Termi.Logic), Class I & II, 1.8V, with DCI	SSTL18_I_DCI, SSTL18_II_DCI	50	0	V_{REF}	0.9
SSTL, Class I & II, 2.5V, with DCI	SSTL2_I_DCI, SSTL2_II_DCI	50	0	V_{REF}	1.25

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Input/Output Logic Switching Characteristics

Table 49: **ILOGIC Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Setup/Hold						
T_{ICE1CK}/T_{ICKCE1}	CE1 pin Setup/Hold with respect to CLK	0.21/ 0.03	0.25/ 0.04	0.27/ 0.04	0.31/ 0.05	ns
T_{ISRCK}/T_{ICKSR}	SR pin Setup/Hold with respect to CLK	0.66/ –0.08	0.78/ –0.08	0.96/ –0.08	1.09/ –0.11	ns
T_{IDOCK}/T_{IOCKD}	D pin Setup/Hold with respect to CLK without Delay	0.07/ 0.41	0.08/ 0.46	0.10/ 0.54	0.11/ 0.64	ns
T_{IDOCKD}/T_{IOCKDD}	DDLY pin Setup/Hold with respect to CLK (using IODELAY)	0.10/ 0.32	0.12/ 0.36	0.14/ 0.42	0.16/ 0.50	ns
Combinatorial						
T_{IDI}	D pin to O pin propagation delay, no Delay	0.15	0.17	0.20	0.23	ns
T_{IDID}	DDLY pin to O pin propagation delay (using IODELAY)	0.19	0.22	0.25	0.28	ns
Sequential Delays						
T_{IDLO}	D pin to Q1 pin using flip-flop as a latch without Delay	0.48	0.54	0.64	0.73	ns
T_{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IODELAY)	0.52	0.58	0.68	0.78	ns
T_{ICKQ}	CLK to Q outputs	0.54	0.61	0.70	0.93	ns
T_{RQ_ILOGIC}	SR pin to OQ/TQ out	0.85	0.97	1.15	1.32	ns
T_{GSRQ_ILOGIC}	Global Set/Reset to Q outputs	7.60	7.60	10.51	10.51	ns
Set/Reset						
T_{RPW_ILOGIC}	Minimum Pulse Width, SR inputs	0.78	0.95	1.20	1.30	ns, Min

Table 54: **CLB Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{ITO}	An – Dn inputs to A – D Q outputs	0.59	0.67	0.79	0.85	ns, Max
T_{AXA}	AX inputs to AMUX output	0.31	0.35	0.42	0.44	ns, Max
T_{AXB}	AX inputs to BMUX output	0.35	0.39	0.47	0.50	ns, Max
T_{AXC}	AX inputs to CMUX output	0.39	0.44	0.52	0.56	ns, Max
T_{AXD}	AX inputs to DMUX output	0.42	0.47	0.55	0.60	ns, Max
T_{BXB}	BX inputs to BMUX output	0.30	0.34	0.39	0.44	ns, Max
T_{BXD}	BX inputs to DMUX output	0.38	0.43	0.50	0.55	ns, Max
T_{CXC}	CX inputs to CMUX output	0.26	0.29	0.34	0.37	ns, Max
T_{CXD}	CX inputs to DMUX output	0.30	0.34	0.40	0.44	ns, Max
T_{DXD}	DX inputs to DMUX output	0.30	0.33	0.38	0.43	ns, Max
T_{OPCYA}	An input to COUT output	0.32	0.36	0.41	0.47	ns, Max
T_{OPCYB}	Bn input to COUT output	0.32	0.36	0.41	0.47	ns, Max
T_{OPCYC}	Cn input to COUT output	0.27	0.30	0.34	0.40	ns, Max
T_{OPCYD}	Dn input to COUT output	0.25	0.28	0.32	0.37	ns, Max
T_{AXCY}	AX input to COUT output	0.25	0.28	0.33	0.36	ns, Max
T_{BXCY}	BX input to COUT output	0.22	0.24	0.28	0.31	ns, Max
T_{CXCY}	CX input to COUT output	0.15	0.17	0.20	0.22	ns, Max
T_{DXCY}	DX input to COUT output	0.14	0.16	0.19	0.21	ns, Max
T_{BYP}	CIN input to COUT output	0.06	0.07	0.08	0.09	ns, Max
T_{CINA}	CIN input to AMUX output	0.21	0.24	0.28	0.30	ns, Max
T_{CINB}	CIN input to BMUX output	0.23	0.25	0.29	0.31	ns, Max
T_{CINC}	CIN input to CMUX output	0.23	0.26	0.30	0.33	ns, Max
T_{CIND}	CIN input to DMUX output	0.25	0.29	0.33	0.36	ns, Max
Sequential Delays						
T_{CKO}	Clock to AQ – DQ outputs	0.29	0.33	0.39	0.44	ns, Max
T_{SHCKO}	Clock to AMUX – DMUX outputs	0.36	0.40	0.47	0.53	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK						
T_{DICK}/T_{CKDI}	A – D input to CLK on A – D Flip Flops	0.30/0.17	0.36/0.18	0.43/0.20	0.44/0.25	ns, Min
$T_{CECK\_CLB}/T_{CKCE\_CLB}$	CE input to CLK on A – D Flip Flops	0.20/0.00	0.25/0.00	0.32/0.00	0.32/0.01	ns, Min
T_{SRCK}/T_{CKSR}	SR input to CLK on A – D Flip Flops	0.39/–0.07	0.44/–0.07	0.52/–0.07	0.58/–0.08	ns, Min
T_{CINCK}/T_{CKCIN}	CIN input to CLK on A – D Flip Flops	0.16/0.12	0.19/0.14	0.24/0.16	0.23/0.22	ns, Min
Set/Reset						
T_{SRMIN}	SR input minimum pulse width	0.90	0.90	0.97	0.80	ns, Min
T_{RQ}	Delay from SR input to AQ – DQ flip-flops	0.52	0.58	0.68	0.77	ns, Max
T_{CEO}	Delay from CE input to AQ – DQ flip-flops	0.41	0.48	0.59	0.61	ns, Max
F_{TOG}	Toggle frequency (for export control)	1412.00	1286.40	1098.00	1098.00	MHz

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
2. These items are of interest for Carry Chain applications.

Block RAM and FIFO Switching Characteristics

Table 57: **Block RAM and FIFO Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Block RAM and FIFO Clock-to-Out Delays						
T_{RCKO_DO} and $T_{RCKO\_DO\_REG}$[1]	Clock CLK to DOUT output (without output register)[2][3]	1.60	1.79	2.08	2.36	ns, Max
	Clock CLK to DOUT output (with output register)[4][5]	0.60	0.66	0.75	0.83	ns, Max
$T_{RCKO\_DO\_ECC}$ and $T_{RCKO\_DO\_ECC\_REG}$	Clock CLK to DOUT output with ECC (without output register)[2][3]	2.62	2.89	3.30	3.73	ns, Max
	Clock CLK to DOUT output with ECC (with output register)[4][5]	0.71	0.77	0.86	0.94	ns, Max
T_{RCKO_CASC} and $T_{RCKO\_CASC\_REG}$	Clock CLK to DOUT output with Cascade (without output register)[2]	2.49	2.77	3.18	3.61	ns, Max
	Clock CLK to DOUT output with Cascade (with output register)[4]	1.29	1.41	1.58	1.79	ns, Max
T_{RCKO_FLAGS}	Clock CLK to FIFO flags outputs[6]	0.74	0.81	0.91	0.98	ns, Max
$T_{RCKO\_POINTERS}$	Clock CLK to FIFO pointers outputs[7]	0.90	0.98	1.09	1.21	ns, Max
$T_{RCKO\_SDBIT\_ECC}$ and $T_{RCKO\_SDBIT\_ECC\_REG}$	Clock CLK to BITERR (with output register)	0.62	0.68	0.76	0.82	ns, Max
	Clock CLK to BITERR (without output register)	2.21	2.46	2.84	3.23	ns, Max
$T_{RCKO\_PARITY\_ECC}$	Clock CLK to ECCPARITY in ECC encode only mode	0.86	0.94	1.06	1.18	ns, Max
$T_{RCKO\_RDADDR\_ECC}$ and $T_{RCKO\_RDADDR\_ECC\_REG}$	Clock CLK to RDADDR output with ECC (without output register)	0.73	0.79	0.90	1.00	ns, Max
	Clock CLK to RDADDR output with ECC (with output register)	0.76	0.82	0.92	1.02	ns, Max
Setup and Hold Times Before/After Clock CLK						
$T_{RCCK\_ADDR}/T_{RCKC\_ADDR}$	ADDR inputs[8]	0.47/ 0.27	0.53/ 0.29	0.62/ 0.32	0.66/ 0.34	ns, Min
T_{RDCK_DI}/T_{RCKD_DI}	DIN inputs[9]	0.84/ 0.30	0.95/ 0.32	1.11/ 0.34	1.26/ 0.36	ns, Min
$T_{RDCK\_DI\_ECC}/T_{RCKD\_DI\_ECC}$	DIN inputs with block RAM ECC in standard mode[9]	0.47/ 0.30	0.52/ 0.32	0.59/ 0.34	0.68/ 0.36	ns, Min
	DIN inputs with block RAM ECC encode only[9]	0.68/ 0.30	0.75/ 0.32	0.85/ 0.34	0.97/ 0.36	ns, Min
	DIN inputs with FIFO ECC in standard mode[9]	0.77/ 0.30	0.87/ 0.32	1.02/ 0.34	1.16/ 0.36	ns, Min
$T_{RCCK\_CLK}/T_{RCKC\_CLK}$	Inject single/double bit error in ECC mode	0.90/ 0.27	1.02/ 0.28	1.20/ 0.29	1.56/ 0.29	ns, Min
$T_{RCCK\_RDEN}/T_{RCKC\_RDEN}$	Block RAM Enable (EN) input	0.31/ 0.26	0.35/ 0.27	0.41/ 0.30	0.44/ 0.31	ns, Min
$T_{RCCK\_REGCE}/T_{RCKC\_REGCE}$	CE input of output register	0.18/ 0.25	0.19/ 0.27	0.22/ 0.31	0.24/ 0.33	ns, Min
$T_{RCCK\_RSTREG}/T_{RCKC\_RSTREG}$	Synchronous RSTREG input	0.22/ 0.23	0.24/ 0.24	0.28/ 0.26	0.31/ 0.27	ns, Min
$T_{RCCK\_RSTRAM}/T_{RCKC\_RSTRAM}$	Synchronous RSTRAM input	0.32/ 0.23	0.36/ 0.24	0.41/ 0.27	0.46/ 0.29	ns, Min

Table 62: **Regional Clock Switching Characteristics (BUFR) *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{BRDO_O}	Propagation delay from CLR to O	0.69	0.74	0.80	1.12	ns
Maximum Frequency						
F_{MAX}[1]	Regional clock tree (BUFR)	500	420	300	300	MHz

Notes:

1. The maximum input frequency to the BUFR is the BUFIO F_{MAX} frequency.

Table 63: **Horizontal Clock Buffer Switching Characteristics (BUFH)**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{BHCKO_O}	BUFH delay from I to O	0.10	0.11	0.13	0.15	ns
$T_{BHCCK\_CE}/T_{BHCKC\_CE}$	CE pin Setup and Hold	0.04/ 0.04	0.04/ 0.04	0.05/ 0.05	0.04/ 0.04	ns
Maximum Frequency						
F_{MAX}	Horizontal clock buffer (BUFH)	800	750	700	667	MHz

MMCM Switching Characteristics

Table 64: **MMCM Specification**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
F_{INMAX}	Maximum Input Clock Frequency[1]	800	750	700	700	MHz
F_{INMIN}	Minimum Input Clock Frequency	10	10	10	10	MHz
$F_{INJITTER}$	Maximum Input Clock Period Jitter	< 20% of clock input period or 1 ns Max				
F_{INDUTY}[2]	Allowable Input Duty Cycle: 10—49 MHz	25/75				%
	Allowable Input Duty Cycle: 50—199 MHz	30/70				%
	Allowable Input Duty Cycle: 200—399 MHz	35/65				%
	Allowable Input Duty Cycle: 400—499 MHz	40/60				%
	Allowable Input Duty Cycle: >500 MHz	45/55				%
F_{MIN_PSCLK}	Minimum Dynamic Phase Shift Clock Frequency	0.01	0.01	0.01	0.01	MHz
F_{MAX_PSCLK}	Maximum Dynamic Phase Shift Clock Frequency	550	500	450	450	MHz
F_{VCOMIN}	Minimum MMCM VCO Frequency	600	600	600	600	MHz
F_{VCOMAX}	Maximum MMCM VCO Frequency	1600	1440	1200	1200	MHz
$F_{BANDWIDTH}$	Low MMCM Bandwidth at Typical[3]	1.00	1.00	1.00	1.00	MHz
	High MMCM Bandwidth at Typical[3]	4.00	4.00	4.00	4.00	MHz
$T_{STATPHAOFFSET}$	Static Phase Offset of the MMCM Outputs[4]	0.12	0.12	0.12	0.12	ns
$T_{OUTJITTER}$	MMCM Output Jitter[5]	Note 3				
$T_{OUTDUTY}$	MMCM Output Clock Duty Cycle Precision[6]	0.15	0.20	0.20	0.20	ns
$T_{LOCKMAX}$	MMCM Maximum Lock Time	100	100	100	100	µs
F_{OUTMAX}	MMCM Maximum Output Frequency	800	750	700	700	MHz
F_{OUTMIN}	MMCM Minimum Output Frequency[7][8]	4.69	4.69	4.69	4.69	MHz
$T_{EXTFDVAR}$	External Clock Feedback Variation	< 20% of clock input period or 1 ns Max				

Virtex-6 Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 65. Values are expressed in nanoseconds unless otherwise noted.

Table 65: **Global Clock Input to Output Delay Without MMCM**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *without* MMCM.							
T_{ICKOF}	Global Clock input and OUTFF *without* MMCM	XC6VLX75T	4.91	5.32	5.88	6.02	ns
		XC6VLX130T	4.89	5.33	6.00	6.13	ns
		XC6VLX195T	5.02	5.46	6.13	6.27	ns
		XC6VLX240T	5.02	5.46	6.13	6.27	ns
		XC6VLX365T	5.30	5.75	6.43	6.37	ns
		XC6VLX550T	N/A	6.02	6.72	6.60	ns
		XC6VLX760	N/A	6.26	6.97	6.87	ns
		XC6VSX315T	5.40	5.85	6.54	6.49	ns
		XC6VSX475T	N/A	6.01	6.71	6.61	ns
		XC6VHX250T	5.18	5.63	6.30	N/A	ns
		XC6VHX255T	5.20	5.66	6.34	N/A	ns
		XC6VHX380T	5.38	5.84	6.53	N/A	ns
		XC6VHX565T	N/A	6.03	6.71	N/A	ns
		XQ6VLX130T	N/A	5.33	6.00	6.13	ns
		XQ6VLX240T	N/A	5.46	6.13	6.27	ns
		XQ6VLX550T	N/A	N/A	6.72	6.60	ns
		XQ6VSX315T	N/A	5.85	6.54	6.49	ns
		XQ6VSX475T	N/A	N/A	6.71	6.61	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 67: **Clock-Capable Clock Input to Output Delay With MMCM**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
LVCMOS25 Clock-capable Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* MMCM.							
$T_{ICKOFMMCMCC}$	Clock-capable Clock Input and OUTFF *with* MMCM	XC6VLX75T	2.22	2.38	2.63	2.72	ns
		XC6VLX130T	2.24	2.39	2.65	2.74	ns
		XC6VLX195T	2.24	2.40	2.65	2.75	ns
		XC6VLX240T	2.24	2.40	2.65	2.75	ns
		XC6VLX365T	2.25	2.42	2.65	2.76	ns
		XC6VLX550T	N/A	2.43	2.68	2.80	ns
		XC6VLX760	N/A	2.42	2.69	2.79	ns
		XC6VSX315T	2.23	2.38	2.65	2.73	ns
		XC6VSX475T	N/A	2.30	2.57	2.66	ns
		XC6VHX250T	2.25	2.41	2.67	N/A	ns
		XC6VHX255T	2.35	2.51	2.78	N/A	ns
		XC6VHX380T	2.27	2.43	2.69	N/A	ns
		XC6VHX565T	N/A	2.41	2.68	N/A	ns
		XQ6VLX130T	N/A	2.39	2.65	2.74	ns
		XQ6VLX240T	N/A	2.40	2.65	2.75	ns
		XQ6VLX550T	N/A	N/A	2.68	2.80	ns
		XQ6VSX315T	N/A	2.38	2.65	2.73	ns
		XQ6VSX475T	N/A	N/A	2.57	2.66	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 69: **Global Clock Input Setup and Hold With MMCM**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)							
$T_{PSMMCMGC}$/ $T_{PHMMCMGC}$	No Delay Global Clock Input and IFF(2) with MMCM	XC6VLX75T	1.45/ –0.18	1.57/ –0.18	1.72/ –0.18	1.78/ –0.08	ns
		XC6VLX130T	1.53/ –0.18	1.65/ –0.18	1.81/ –0.18	1.87/ –0.07	ns
		XC6VLX195T	1.54/ –0.17	1.66/ –0.17	1.82/ –0.17	1.87/ –0.08	ns
		XC6VLX240T	1.54/ –0.17	1.66/ –0.17	1.82/ –0.17	1.87/ –0.08	ns
		XC6VLX365T	1.55/ –0.18	1.67/ –0.18	1.83/ –0.18	1.87/ –0.07	ns
		XC6VLX550T	N/A	1.84/ –0.17	2.02/ –0.17	2.06/ –0.06	ns
		XC6VLX760	N/A	2.26/ –0.13	2.49/ –0.13	2.06/ –0.03	ns
		XC6VSX315T	1.56/ –0.18	1.68/ –0.18	1.84/ –0.18	1.89/ –0.08	ns
		XC6VSX475T	N/A	1.85/ –0.23	2.03/ –0.23	2.07/ –0.13	ns
		XC6VHX250T	1.52/ –0.17	1.64/ –0.17	1.80/ –0.17	N/A	ns
		XC6VHX255T	1.52/ –0.12	1.64/ –0.12	1.85/ –0.12	N/A	ns
		XC6VHX380T	1.68/ –0.16	1.81/ –0.16	1.99/ –0.16	N/A	ns
		XC6VHX565T	N/A	1.81/ –0.01	1.99/ –0.01	N/A	ns
		XQ6VLX130T	N/A	1.65/ –0.18	1.81/ –0.18	1.87/ –0.07	ns
		XQ6VLX240T	N/A	1.66/ –0.17	1.82/ –0.17	1.87/ –0.08	ns
		XQ6VLX550T	N/A	N/A	2.02/ –0.17	2.06/ –0.06	ns
		XQ6VSX315T	N/A	1.68/ –0.18	1.84/ –0.18	1.89/ –0.08	ns
		XQ6VSX475T	N/A	N/A	2.03/ –0.23	2.07/ –0.13	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 70: **Clock-Capable Clock Input Setup and Hold With MMCM**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
Input Setup and Hold Time Relative to Clock-capable Clock Input Signal for LVCMOS25 Standard.(1)							
$T_{PSMMCMCC}$/ $T_{PHMMCMCC}$	No Delay Clock-capable Clock Input and IFF(2) with MMCM	XC6VLX75T	1.56/ –0.25	1.69/ –0.25	1.86/ –0.25	1.91/ –0.15	ns
		XC6VLX130T	1.64/ –0.25	1.78/ –0.25	1.95/ –0.25	2.00/ –0.14	ns
		XC6VLX195T	1.65/ –0.24	1.79/ –0.24	1.96/ –0.24	2.01/ –0.15	ns
		XC6VLX240T	1.65/ –0.24	1.79/ –0.24	1.96/ –0.24	2.01/ –0.15	ns
		XC6VLX365T	1.66/ –0.25	1.79/ –0.25	1.97/ –0.25	2.02/ –0.15	ns
		XC6VLX550T	N/A	1.97/ –0.24	2.16/ –0.24	2.19/ –0.14	ns
		XC6VLX760	N/A	2.39/ –0.20	2.63/ –0.20	2.21/ –0.10	ns
		XC6VSX315T	1.67/ –0.25	1.80/ –0.25	1.98/ –0.25	2.03/ –0.16	ns
		XC6VSX475T	N/A	1.98/ –0.29	2.17/ –0.29	2.21/ –0.20	ns
		XC6VHX250T	1.63/ –0.24	1.76/ –0.24	1.94/ –0.24	N/A	ns
		XC6VHX255T	1.63/ –0.19	1.76/ –0.19	1.99/ –0.19	N/A	ns
		XC6VHX380T	1.80/ –0.23	1.94/ –0.23	2.13/ –0.23	N/A	ns
		XC6VHX565T	N/A	1.94/ –0.08	2.13/ –0.08	N/A	ns
		XQ6VLX130T	N/A	1.78/ –0.25	1.95/ –0.25	2.00/ –0.14	ns
		XQ6VLX240T	N/A	1.79/ –0.24	1.96/ –0.24	2.01/ –0.15	ns
		XQ6VLX550T	N/A	N/A	2.16/ –0.24	2.19/ –0.14	ns
		XQ6VSX315T	N/A	1.80/ –0.25	1.98/ –0.25	2.03/ –0.16	ns
		XQ6VSX475T	N/A	N/A	2.17/ –0.29	2.21/ –0.20	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Clock Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-6 FPGA clock transmitter and receiver data-valid windows.

Table 71: **Duty Cycle Distortion and Clock-Tree Skew**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
T_{DCD_CLK}	Global Clock Tree Duty Cycle Distortion(1)	All	0.12	0.12	0.12	0.12	ns
T_{CKSKEW}	Global Clock Tree Skew(2)	XC6VLX75T	0.15	0.16	0.18	0.17	ns
		XC6VLX130T	0.25	0.26	0.29	0.28	ns
		XC6VLX195T	0.26	0.27	0.31	0.30	ns
		XC6VLX240T	0.26	0.27	0.31	0.30	ns
		XC6VLX365T	0.28	0.29	0.31	0.31	ns
		XC6VLX550T	N/A	0.50	0.54	0.54	ns
		XC6VLX760	N/A	0.51	0.56	0.56	ns
		XC6VSX315T	0.27	0.28	0.32	0.30	ns
		XC6VSX475T	N/A	0.39	0.44	0.42	ns
		XC6VHX250T	0.25	0.26	0.29	N/A	ns
		XC6VHX255T	0.35	0.37	0.41	N/A	ns
		XC6VHX380T	0.45	0.47	0.52	N/A	ns
		XC6VHX565T	N/A	0.46	0.51	N/A	ns
		XQ6VLX130T	N/A	0.26	0.29	0.28	ns
		XQ6VLX240T	N/A	0.27	0.31	0.30	ns
		XQ6VLX550T	N/A	N/A	0.54	0.54	ns
		XQ6VSX315T	N/A	0.28	0.32	0.30	ns
		XQ6VSX475T	N/A	N/A	0.44	0.42	ns
T_{DCD_BUFIO}	I/O clock tree duty cycle distortion	All	0.08	0.08	0.08	0.08	ns
$T_{BUFIOSKEW}$	I/O clock tree skew across one clock region	All	0.03	0.03	0.03	0.02	ns
$T_{BUFIOSKEW2}$	I/O clock tree skew across three clock regions	All	0.10	0.12	0.23	0.12	ns
T_{DCD_BUFR}	Regional clock tree duty cycle distortion	All	0.15	0.15	0.15	0.15	ns

Notes:

1. These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
2. The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

Table 72: **Package Skew**

Symbol	Description	Device	Package	Value	Units
$T_{PKGSKEW}$	Package Skew(1)	XC6VLX75T	FF484	95	ps
			FF784	146	ps
		XC6VLX130T	FF484	95	ps
			FF784	146	ps
			FF1156	165	ps
		XC6VLX195T	FF784	145	ps
			FF1156	182	ps
		XC6VLX240T	FF784	146	ps
			FF1156	182	ps
			FF1759	187	ps
		XC6VLX365T	FF1156	189	ps
			FF1759	184	ps
		XC6VLX550T	FF1759	196	ps
			FF1760	249	ps
		XC6VLX760	FF1760	236	ps
		XC6VSX315T	FF1156	168	ps
			FF1759	190	ps
		XC6VSX475T	FF1156	168	ps
			FF1759	204	ps
		XC6VHX250T	FF1154	166	ps
		XC6VHX255T	FF1155	168	ps
			FF1923	228	ps
		XC6VHX380T	FF1154	159	ps
			FF1155	172	ps
			FF1923	227	ps
			FF1924	220	ps
		XC6VHX565T	FF1923	232	ps
			FF1924	197	ps
		XQ6VLX130T	RF784	146	ps
			RF1156	165	ps
			FFG1156	165	ps
		XQ6VLX240T	RF784	146	ps
			RF1156	182	ps
			FFG1156	182	ps
			RF1759	187	ps
		XQ6VLX550T	RF1759	196	ps
		XQ6VSX315T	RF1156	168	ps
			FFG1156	168	ps
			RF1759	190	ps
		XQ6VSX475T	RF1156	168	ps
			FFG1156	168	ps
			RF1759	204	ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest flight time to longest flight time from Pad to Ball (7.0 ps per mm).
2. Package trace length information is available for these device/package combinations. This information can be used to deskew the package.