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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	37200
Number of Logic Elements/Cells	476160
Total RAM Bits	39223296
Number of I/O	600
Number of Gates	-
Voltage - Supply	0.95V ~ 1.05V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1156-BBGA, FCBGA
Supplier Device Package	1156-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6vsx475t-2ffg1156c

Table 2: Recommended Operating Conditions

Symbol	Description	Min	Max	Units
V_{CCINT}	Internal supply voltage relative to GND for all devices except -1L devices.	0.95	1.05	V
	For -1L commercial temperature range devices: internal supply voltage relative to GND, $T_j = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	0.87	0.93	V
	For -1L industrial temperature range devices: internal supply voltage relative to GND, $T_j = -40^{\circ}\text{C}$ to $+100^{\circ}\text{C}$	0.91	0.97	V
V_{CCAUX}	Auxiliary supply voltage relative to GND	2.375	2.625	V
$V_{CCO}^{(1)(2)(3)}$	Supply voltage relative to GND	1.14	2.625	V
V_{IN}	2.5V supply voltage relative to GND	GND – 0.20	2.625	V
	2.5V and below supply voltage relative to GND	GND – 0.20	$V_{CCO} + 0.2$	V
$I_{IN}^{(5)}$	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	–	10	mA
$V_{BATT}^{(6)}$	Battery voltage relative to GND	1.0	2.5	V
$V_{FS}^{(7)}$	External voltage supply for eFUSE programming	2.375	2.625	V
T_j	Junction temperature operating range for commercial (C) temperature devices	0	85	$^{\circ}\text{C}$
	Junction temperature operating range for extended (E) temperature devices	0	100	$^{\circ}\text{C}$
	Junction temperature operating range for industrial (I) temperature devices	–40	100	$^{\circ}\text{C}$
	Junction temperature operating range for military (M) temperature devices	–55	125	$^{\circ}\text{C}$

Notes:

- Configuration data is retained even if V_{CCO} drops to 0V.
- Includes V_{CCO} of 1.2V, 1.5V, 1.8V, and 2.5V.
- The configuration supply voltage V_{CC_CONFIG} is also known as V_{CCO_0} .
- All voltages are relative to ground.
- A total of 100 mA per bank should not be exceeded.
- V_{BATT} is required only when using bitstream encryption. If battery is not used, connect V_{BATT} to either ground or V_{CCAUX} .
- During eFUSE programming, V_{FS} must be within the recommended operating range and $T_j = +15^{\circ}\text{C}$ to $+85^{\circ}\text{C}$. Otherwise, V_{FS} can be connected to GND.

Table 3: DC Characteristics Over Recommended Operating Conditions (1)(2)

Symbol	Description	Min	Typ	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	0.75	–	–	V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	2.0	–	–	V
I_{REF}	V_{REF} leakage current per pin	–	–	10	μA
I_L	Input or output leakage current per pin (sample-tested)	–	–	10	μA
$C_{IN}^{(3)}$	Die input capacitance at the pad	–	–	8	pF
I_{RPU}	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 2.5V$	20	–	80	μA
	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 1.8V$	8	–	40	μA
	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 1.5V$	5	–	30	μA
	Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 1.2V$	1	–	20	μA
I_{RPD}	Pad pull-down (when selected) @ $V_{IN} = 2.5V$	3	–	80	μA
I_{BATT}	Battery supply current	–	–	150	nA
n	Temperature diode ideality factor	–	1.0002	–	n
r	Series resistance	–	5	–	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. Maximum value specified for worst case process at 25°C.
3. This measurement represents the die capacitance at the pad, not including the package.

HT DC Specifications (HT_25)

Table 8: HT DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OD}	Differential Output Voltage for XC devices	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	480	600	885	mV
	Differential Output Voltage for XQ devices		480	600	930	mV
ΔV_{OD}	Change in V_{OD} Magnitude		-15	—	15	mV
V_{OCM}	Output Common Mode Voltage	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	440	600	760	mV
ΔV_{OCM}	Change in V_{OCM} Magnitude		-15	—	15	mV
V_{ID}	Input Differential Voltage		200	600	1000	mV
ΔV_{ID}	Change in V_{ID} Magnitude		-15	—	15	mV
V_{ICM}	Input Common Mode Voltage		440	600	780	mV
ΔV_{ICM}	Change in V_{ICM} Magnitude		-15	—	15	mV

LVDS DC Specifications (LVDS_25)

Table 9: LVDS DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	—	—	1.675	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	0.825	—	—	V
V_{ODIFF}	Differential Output Voltage (Q - $\overline{Q}$), Q = High ($\overline{Q}$ - Q), $\overline{Q}$ = High	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output Common-Mode Voltage for XC devices	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	1.075	1.250	1.425	V
	Output Common-Mode Voltage for XQ devices		1.000	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q - $\overline{Q}$), Q = High ($\overline{Q}$ - Q), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input Common-Mode Voltage		0.3	1.2	2.2	V

Extended LVDS DC Specifications (LVDSEXT_25)

Table 10: Extended LVDS DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	—	—	1.785	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	0.715	—	—	V
V_{ODIFF}	Differential Output Voltage (Q - $\overline{Q}$), Q = High ($\overline{Q}$ - Q), $\overline{Q}$ = High for XC devices	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	350	—	840	mV
	Differential Output Voltage (Q - $\overline{Q}$), Q = High ($\overline{Q}$ - Q), $\overline{Q}$ = High for XQ devices		350	—	850	mV
V_{OCM}	Output Common-Mode Voltage for XC devices	$R_T = 100\ \Omega$ across Q and $\overline{Q}$ signals	1.075	1.250	1.425	V
	Output Common-Mode Voltage for XQ devices		1.000	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q - $\overline{Q}$), Q = High ($\overline{Q}$ - Q), $\overline{Q}$ = High	Common-mode input voltage = 1.25V	100	—	1000	mV
V_{ICM}	Input Common-Mode Voltage	Differential input voltage = ± 350 mV	0.3	1.2	2.2	V

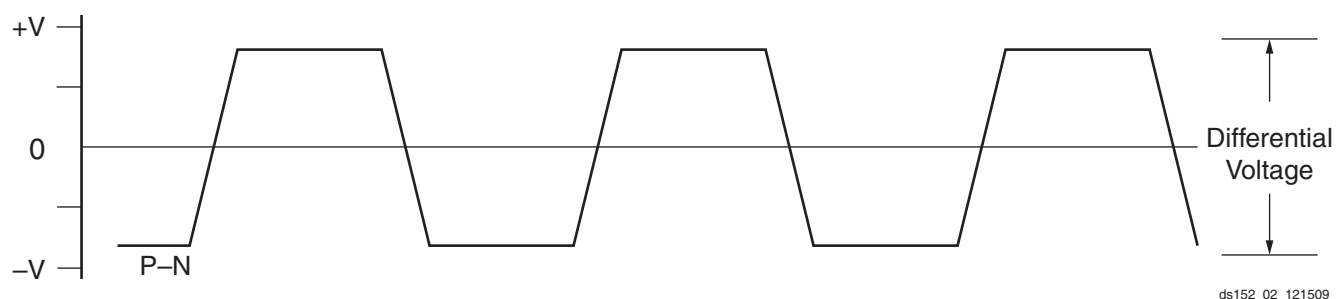


Figure 2: Differential Peak-to-Peak Voltage

Table 18 summarizes the DC specifications of the clock input of the GTX transceiver. Consult [UG366: Virtex-6 FPGA GTX Transceivers User Guide](#) for further details.

Table 18: GTX Transceiver Clock DC Input Level Specification

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	210	800	2000	mV
R_{IN}	Differential input resistance	90	100	130	Ω
C_{EXT}	Required external AC coupling capacitor	—	100	—	nF

GTX Transceiver Switching Characteristics

Consult [UG366: Virtex-6 FPGA GTX Transceivers User Guide](#) for further information.

Table 19: GTX Transceiver Performance

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
F_{GTXMAX}	Maximum GTX transceiver data rate	6.6	6.6	5.0	5.0	Gb/s
$F_{GPLLMAX}$	Maximum PLL frequency	3.3 ⁽¹⁾	3.3 ⁽¹⁾	2.7	2.7	GHz
$F_{GPLLMIN}$	Minimum PLL frequency	1.2	1.2	1.2	1.2	GHz

Notes:

- See Table 14 for MGTAVCC requirements when PLL frequency is greater than 2.7 GHz.

Table 20: GTX Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
$F_{GTXDRPCLK}$	GTXDRPCLK maximum frequency	150	150	125	100	MHz

Table 21: GTX Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range		62.5	–	650	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	45	50	55	%
T_{LOCK}	Clock recovery frequency acquisition time	Initial PLL lock	–	–	1	ms
T_{PHASE}	Clock recovery phase acquisition time	Lock to data after PLL has locked to the reference clock	–	–	200	μ s

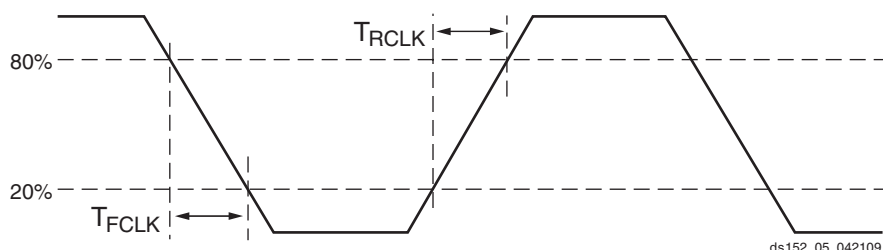


Figure 3: Reference Clock Timing Parameters

Table 22: GTX Transceiver User Clock Switching Characteristics⁽¹⁾

Symbol	Description	Conditions	Speed Grade				Units
			-3	-2	-1	-1L	
F_{TXOUT}	TXOUTCLK maximum frequency	Internal 20-bit data path	330	330	250	250	MHz
		Internal 16-bit data path	412.5	412.5	312.5	250	MHz
F_{RXREC}	RXRECCLK maximum frequency	Internal 20-bit data path	330	330	250	250	MHz
		Internal 16-bit data path	412.5	412.5	312.5	250	MHz
T_{RX}	RXUSRCLK maximum frequency		412.5 ⁽²⁾	412.5 ⁽²⁾	312.5	250	MHz
T_{RX2}	RXUSRCLK2 maximum frequency	1 byte interface	376	376	312.5	250	MHz
		2 byte interface	406.25	406.25	312.5	250	MHz
		4 byte interface	206.25	206.25	156.25	125	MHz
T_{TX}	TXUSRCLK maximum frequency		412.5 ⁽³⁾	412.5 ⁽³⁾	312.5	250	MHz
T_{TX2}	TXUSRCLK2 maximum frequency	1 byte interface	376	376	312.5	250	MHz
		2 byte interface	406.25	406.25	312.5	250	MHz
		4 byte interface	206.25	206.25	156.25	125	MHz

Notes:

1. Clocking must be implemented as described in [UG366: Virtex-6 FPGA GTX Transceivers User Guide](#).
2. 406.25 MHz when the RX elastic buffer is bypassed.
3. 406.25 MHz when the TX buffer is bypassed.

GTH Transceiver Specifications

GTH Transceiver DC Characteristics

Table 25: Absolute Maximum Ratings for GTH Transceivers⁽¹⁾

Symbol	Description	Min	Max	Units
MGTHAVCC	Analog supply voltage for the GTH transmitter, receiver, and common analog circuits	−0.5	1.125	V
MGTHAVCCR _X	Analog supply voltage for the GTH receiver circuits and common analog circuits	−0.5	1.125	V
MGTHAVTT	Analog supply voltage for the GTH transmitter termination circuits	−0.5	1.32	V
MGTHAVCCPLL	Analog supply voltage for the GTH receiver and PLL circuits	−0.5	1.935	V
V _{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	−0.5	1.125	V
V _{MGTREFCLK}	Reference clock absolute input voltage	−0.5	1.935	V

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 26: Recommended Operating Conditions for GTH Transceivers ⁽¹⁾⁽²⁾

Symbol	Description	Min	Typ	Max	Units
MGTHAVCC	Analog supply voltage for the GTH transmitter, receiver, and common analog circuits	1.075	1.1	1.125	V
MGTHAVCCR _X	Analog supply voltage for the GTH receiver circuits and common analog circuits	1.075	1.1	1.125	V
MGTHAVTT	Analog supply voltage for the GTH transmitter termination circuits	1.140	1.2	1.26	V
MGTHAVCCPLL	Analog supply voltage for the GTH receiver and PLL circuit	1.710	1.8	1.89	V

Notes:

- Each voltage listed requires the filter circuit described in [UG371: Virtex-6 FPGA GTH Transceivers User Guide](#).
- Voltages are specified for the temperature range of T_j = −40°C to +100°C.

Table 27: GTH Transceiver Power Supply Sequencing ⁽¹⁾⁽²⁾⁽³⁾

Symbol	Description	Min	Max	Units
T _{HAVCC2HAVCCR_X}	Maximum time between powering MGTHAVCC to when MGTHAVCCR _X must be powered.	0	5	ms
T _{HAVCCR_X2HAVCCPLL}	Minimum time between powering MGTHAVCCR _X to when MGTHAVCCPLL can be powered.	10	—	μs
T _{HAVCCR_X2HAVTT}	Minimum time between powering MGTHAVCCR _X to when MGTHAVTT can be powered.	10	—	μs

Notes:

- MGTHAVCCR_X must be powered simultaneously or within T_{HAVCC2HAVCCR_X} of MGTHAVCC, but it must not precede MGTHAVCC.
- MGTHAVCC and MGTHAVCCR_X must be powered before MGTHAVCCPLL and MGTHAVTT. This minimum time is defined by T_{HAVCCR_X2HAVCCPLL} and T_{HAVCCR_X2HAVTT}.
- At any time, the condition of MGTHAVCC being present and MGTHAVCCR_X not being present should not occur for more than the maximum T_{HAVCC2HAVCCR_X}.

Figure 4 shows the timing parameters in Table 27.

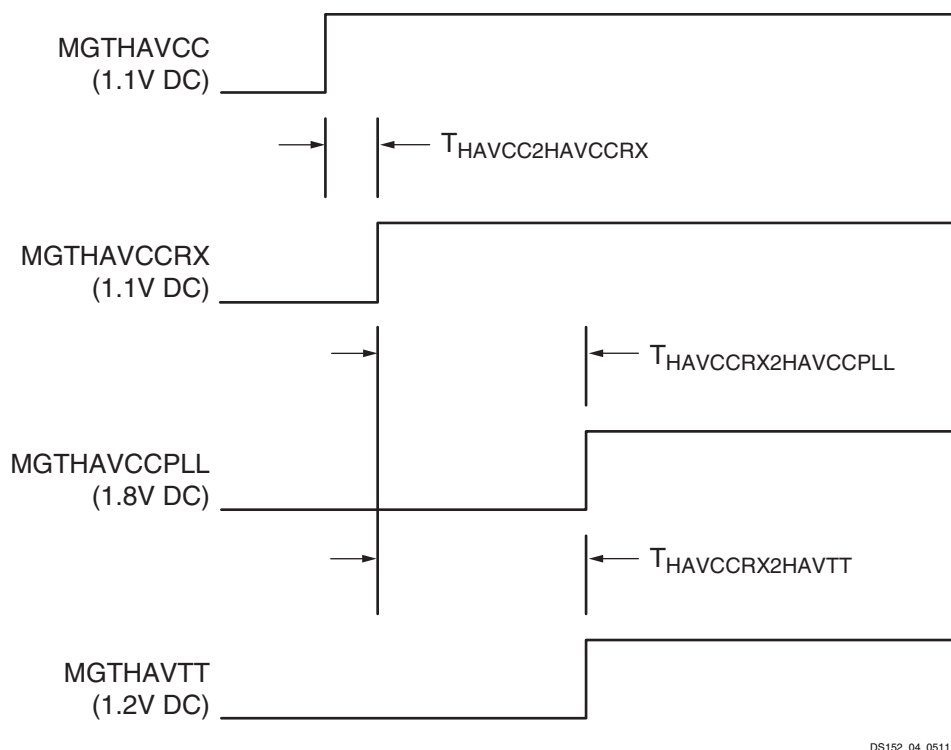


Figure 4: GTH Transceiver Power Supply Power-On Sequencing

Table 28: GTH Transceiver Supply Current

Symbol	Description	Typ ⁽¹⁾	Max	Units
$I_{MGTHAVCC}$	MGTHAVCC supply current for one GTH Quad (4 lanes)	571	Note 2	mA
$I_{MGTHAVCCR}$	MGTHAVCCR supply current for a GTH Quad (4 lanes)	254	Note 2	mA
$I_{MGTHAVTT}$	MGTHAVTT supply current for one GTH Quad (4 lanes)	93	Note 2	mA
$I_{MGTHAVCCPLL}$	MGTHAVCCPLL supply current for one GTH Quad (4 lanes)	219	Note 2	mA
$MGTR_{REF}$	Precision reference resistor for internal calibration termination	1000.0 ± 1% tolerance		Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C, with a 10.3125 Gb/s line rate.
2. Values for currents other than the values specified in this table can be obtained by using the XPower Estimator (XPE) or XPower Analyzer (XPA) tools.

Table 29: GTH Transceiver Quiescent Supply Current⁽¹⁾⁽²⁾

Symbol	Description	Typ ⁽³⁾	Max	Units
$I_{MGTHAVCCQ}$	Quiescent MGTHAVCC Supply Current for one GTH Quad (4 lanes)	65	Note 4	mA
$I_{MGTHAVCCRQ}$	Quiescent MGTHAVCCR Supply Current for one GTH Quad (4 lanes)	17	Note 4	mA
$I_{MGTHAVTTQ}$	Quiescent MGTHAVTT Supply Current for one GTH Quad (4 lanes)	1	Note 4	mA
$I_{MGTHAVCCPLLQ}$	Quiescent MGTHAVCCPLL Supply Current for one GTH Quad (4 lanes)	1	Note 4	mA

Notes:

1. Device powered and unconfigured.
2. GTH transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTH transceivers.
3. Typical values are specified at nominal voltage, 25°C.
4. Currents for conditions other than values specified in this table can be obtained by using the XPE or XPA tools.

GTH Transceiver DC Input and Output Levels

Table 30 summarizes the DC output specifications of the GTH transceivers in Virtex-6 FPGAs. Consult [UG371: Virtex-6 FPGA GTH Transceivers User Guide](#) for further details.

Table 30: GTH Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
D_{VPPIN}	Differential peak-to-peak input voltage	External AC coupled	175	–	1200	mV
D_{VPPOUT}	Differential peak-to-peak output voltage ⁽¹⁾	Transmitter output swing is set to maximum setting	800	–	1200	mV
R_{IN}	Differential input resistance		80	100	120	Ω
R_{OUT}	Differential output resistance		80	100	120	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	2	–	ps
C_{EXT}	Recommended external AC coupling capacitor ⁽²⁾		–	100	–	nF

Notes:

1. The output swing and preemphasis levels are programmable using the attributes discussed in [UG371: Virtex-6 FPGA GTH Transceivers User Guide](#) and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

Table 31 summarizes the DC specifications of the clock input of the GTH transceiver. Consult [UG371: Virtex-6 FPGA GTH Transceivers User Guide](#) for further details.

Table 31: GTH Transceiver Clock DC Input Level Specification

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	≤ 600 MHz	500	–	1600	mV
		> 600 MHz	600	–	1600	mV
R_{IN}	Differential input resistance		80	100	120	Ω
C_{EXT}	Required external AC coupling capacitor		–	100	–	nF

GTH Transceiver Switching Characteristics

Consult [UG371: Virtex-6 FPGA GTH Transceivers User Guide](#) for further information.

Table 32: GTH Transceiver Maximum Data Rate and PLL Frequency Range

Symbol	Description	Conditions	Speed Grade			Units
			-3	-2	-1	
F_{GTHMAX}	Maximum GTH transceiver data rate	PLL Output Divider = 1	11.182	11.182	10.32	Gb/s
		PLL Output Divider = 4	2.795	2.795	2.58	Gb/s
F_{GTHMIN}	Minimum GTH transceiver data rate ⁽¹⁾	PLL Output Divider = 1	9.92	9.92	9.92	Gb/s
		PLL Output Divider = 4	2.48	2.48	2.48	Gb/s
$F_{GPLLMAX}$	Maximum GTH PLL frequency		5.591	5.591	5.16	GHz
$F_{GPLLMIN}$	Minimum GTH PLL frequency		4.96	4.96	4.96	GHz

Notes:

- Lower data rates can be achieved using FPGA logic based oversampling designs.

Table 33: GTH Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
$F_{GTHDRPCLK}$	GTHDRPCLK maximum frequency	70	70	60	MHz

Table 34: GTH Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range	-1 speed grade	150	—	645	MHz
		-2 and -3 speed grades	150	—	700	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	—	200	—	ps
T_{FCLK}	Reference clock fall time	80% – 20%	—	200	—	ps
T_{DCREF}	Reference clock duty cycle	CLK	45	50	55	%
T_{LOCK}	Clock recovery frequency acquisition time	Initial PLL lock	—	—	2	ms
T_{PHASE}	Clock recovery phase acquisition time	Lock to data after PLL has locked to the reference clock	—	—	20	μs

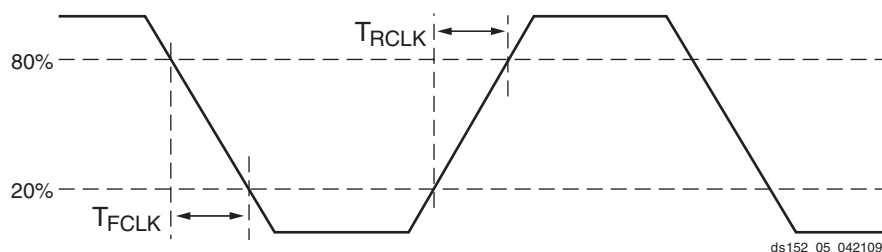


Figure 5: Reference Clock Timing Parameters

Table 35: GTH Transceiver User Clock Switching Characteristics ⁽¹⁾

Symbol	Description	Conditions	Speed Grade			Units
			-3	-2	-1	
F _{TXOUT}	TXUSERCLKOUT maximum frequency		350	350	323	MHz
F _{RXOUT}	RXUSERCLKOUT maximum frequency		350	350	323	MHz
F _{TXIN}	TXUSERCLKIN maximum frequency	16-bit data path	350	350	323	MHz
		20-bit data path	280	280	258	MHz
		32-bit data path	350	350	323	MHz
		40-bit data path	280	280	258	MHz
		64-bit data path	175	175	162	MHz
		80-bit data path	140	140	129	MHz
		64B/66B-bit data path	170	170	157	MHz
F _{RXIN}	RXUSERCLKIN maximum frequency	16-bit data path	350	350	323	MHz
		20-bit data path	280	280	258	MHz
		32-bit data path	350	350	323	MHz
		40-bit data path	280	280	258	MHz
		64-bit data path	175	175	162	MHz
		80-bit data path	140	140	129	MHz
		64B/66B-bit data path	170	170	157	MHz

Notes:

1. Clocking must be implemented as described in [UG371](#): Virtex-6 FPGA GTH Transceivers User Guide.

Table 36: GTH Transceiver Transmitter Switching Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
T _{RTX}	TX Rise time	20%–80%	–	50 ⁽³⁾	–	ps
T _{FTX}	TX Fall time	80%–20%	–	50 ⁽³⁾	–	ps
T _{LLSKEW}	TX lane-to-lane skew	within one GTH Quad	–	–	300	ps
Transmitter Output Jitter⁽¹⁾⁽²⁾						
TJ _{11.18}	Total Jitter	11.181 Gb/s	–	–	0.280	UI
DJ _{11.18}	Deterministic Jitter		–	–	0.170	UI
TJ _{10.3125}	Total Jitter	10.3125 Gb/s	–	–	0.280	UI
DJ _{10.3125}	Deterministic Jitter		–	–	0.170	UI
TJ _{9.953}	Total Jitter	9.953 Gb/s	–	–	0.280	UI
DJ _{9.953}	Deterministic Jitter		–	–	0.170	UI
TJ _{2.667}	Total Jitter	2.667 Gb/s	–	–	0.110	UI
DJ _{2.667}	Deterministic Jitter		–	–	0.060	UI
TJ _{2.488}	Total Jitter	2.488 Gb/s	–	–	0.110	UI
DJ _{2.488}	Deterministic Jitter		–	–	0.060	UI

Notes:

1. These values are NOT intended for protocol specific compliance determinations.
2. All jitter values are based on a bit-error ratio of 1e⁻¹².
3. Rise and fall times are specified at the transmitter package balls.

IOB Pad Input/Output/3-State Switching Characteristics

Table 44 (for commercial (XC) Virtex-6 devices) and **Table 45** (for the Defense-grade (XQ) Virtex-6 devices) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.

T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.

T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer.

Table 46 summarizes the value of T_{IOTPHZ} . T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state).

Table 44: IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
LVDS_25	0.85	0.94	1.09	1.08	1.45	1.54	1.68	1.62	1.45	1.54	1.68	1.62	ns
LVDSEXT_25	0.85	0.94	1.09	1.08	1.53	1.65	1.84	1.73	1.53	1.65	1.84	1.73	ns
HT_25	0.85	0.94	1.09	1.08	1.51	1.62	1.78	1.69	1.51	1.62	1.78	1.69	ns
BLVDS_25	0.85	0.94	1.09	1.08	1.39	1.50	1.67	1.65	1.39	1.50	1.67	1.65	ns
RSDS_25 (point to point)	0.85	0.94	1.09	1.08	1.45	1.54	1.68	1.62	1.45	1.54	1.68	1.62	ns
HSTL_I	0.81	0.91	1.06	1.06	1.45	1.56	1.73	1.71	1.45	1.56	1.73	1.71	ns
HSTL_II	0.81	0.91	1.06	1.06	1.44	1.56	1.74	1.72	1.44	1.56	1.74	1.72	ns
HSTL_III	0.81	0.91	1.06	1.06	1.42	1.54	1.71	1.69	1.42	1.54	1.71	1.69	ns
HSTL_I_18	0.81	0.91	1.06	1.06	1.47	1.58	1.75	1.72	1.47	1.58	1.75	1.72	ns
HSTL_II_18	0.81	0.91	1.06	1.06	1.50	1.62	1.81	1.78	1.50	1.62	1.81	1.78	ns
HSTL_III_18	0.81	0.91	1.06	1.06	1.42	1.54	1.71	1.69	1.42	1.54	1.71	1.69	ns
SSTL2_I	0.81	0.91	1.06	1.06	1.49	1.60	1.77	1.74	1.49	1.60	1.77	1.74	ns
SSTL2_II	0.81	0.91	1.06	1.06	1.42	1.54	1.72	1.71	1.42	1.54	1.72	1.71	ns
SSTL15	0.81	0.91	1.06	1.06	1.42	1.54	1.71	1.69	1.42	1.54	1.71	1.69	ns
LVC MOS25, Slow, 2 mA	0.51	0.57	0.66	0.70	5.09	5.46	6.01	5.63	5.09	5.46	6.01	5.63	ns
LVC MOS25, Slow, 4 mA	0.51	0.57	0.66	0.70	3.30	3.49	3.79	3.65	3.30	3.49	3.79	3.65	ns
LVC MOS25, Slow, 6 mA	0.51	0.57	0.66	0.70	2.62	2.81	3.08	2.95	2.62	2.81	3.08	2.95	ns
LVC MOS25, Slow, 8 mA	0.51	0.57	0.66	0.70	2.21	2.41	2.72	2.59	2.21	2.41	2.72	2.59	ns
LVC MOS25, Slow, 12 mA	0.51	0.57	0.66	0.70	1.80	1.95	2.17	2.10	1.80	1.95	2.17	2.10	ns
LVC MOS25, Slow, 16 mA	0.51	0.57	0.66	0.70	1.89	2.05	2.29	2.21	1.89	2.05	2.29	2.21	ns
LVC MOS25, Slow, 24 mA	0.51	0.57	0.66	0.70	1.68	1.82	2.02	1.98	1.68	1.82	2.02	1.98	ns
LVC MOS25, Fast, 2 mA	0.51	0.57	0.66	0.70	5.12	5.49	6.04	5.62	5.12	5.49	6.04	5.62	ns
LVC MOS25, Fast, 4 mA	0.51	0.57	0.66	0.70	3.28	3.50	3.82	3.65	3.28	3.50	3.82	3.65	ns
LVC MOS25, Fast, 6 mA	0.51	0.57	0.66	0.70	2.56	2.73	2.99	2.88	2.56	2.73	2.99	2.88	ns
LVC MOS25, Fast, 8 mA	0.51	0.57	0.66	0.70	2.11	2.33	2.65	2.53	2.11	2.33	2.65	2.53	ns
LVC MOS25, Fast, 12 mA	0.51	0.57	0.66	0.70	1.74	1.88	2.08	2.03	1.74	1.88	2.08	2.03	ns
LVC MOS25, Fast, 16 mA	0.51	0.57	0.66	0.70	1.77	1.92	2.13	2.08	1.77	1.92	2.13	2.08	ns

Table 44: IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
LVDCI_DV2_25	0.51	0.57	0.66	0.70	1.71	1.83	2.01	2.00	1.71	1.83	2.01	2.00	ns
LVDCI_DV2_18	0.55	0.61	0.71	0.73	1.69	1.81	2.00	1.98	1.69	1.81	2.00	1.98	ns
LVDCI_DV2_15	0.64	0.73	0.85	0.85	1.68	1.77	1.91	1.98	1.68	1.77	1.91	1.98	ns
LVPECL_25	0.85	0.94	1.09	1.08	1.38	1.49	1.65	1.64	1.38	1.49	1.65	1.64	ns
HSTL_I_12	0.81	0.91	1.06	1.06	1.48	1.60	1.78	1.74	1.48	1.60	1.78	1.74	ns
HSTL_I_DCI	0.81	0.91	1.06	1.06	1.40	1.50	1.66	1.64	1.40	1.50	1.66	1.64	ns
HSTL_II_DCI	0.81	0.91	1.06	1.06	1.37	1.49	1.68	1.66	1.37	1.49	1.68	1.66	ns
HSTL_II_T_DCI	0.81	0.91	1.06	1.06	1.40	1.50	1.66	1.64	1.40	1.50	1.66	1.64	ns
HSTL_III_DCI	0.81	0.91	1.06	1.06	1.34	1.45	1.62	1.61	1.34	1.45	1.62	1.61	ns
HSTL_I_DCI_18	0.81	0.91	1.06	1.06	1.42	1.53	1.68	1.66	1.42	1.53	1.68	1.66	ns
HSTL_II_DCI_18	0.81	0.91	1.06	1.06	1.36	1.46	1.62	1.59	1.36	1.46	1.62	1.59	ns
HSTL_II_T_DCI_18	0.81	0.91	1.06	1.06	1.42	1.53	1.68	1.66	1.42	1.53	1.68	1.66	ns
HSTL_III_DCI_18	0.81	0.91	1.06	1.06	1.43	1.54	1.69	1.67	1.43	1.54	1.69	1.67	ns
DIFF_HSTL_I_18	0.85	0.94	1.09	1.08	1.47	1.58	1.75	1.72	1.47	1.58	1.75	1.72	ns
DIFF_HSTL_I_DCI_18	0.85	0.94	1.09	1.08	1.42	1.53	1.68	1.66	1.42	1.53	1.68	1.66	ns
DIFF_HSTL_I	0.85	0.94	1.09	1.08	1.45	1.56	1.73	1.71	1.45	1.56	1.73	1.71	ns
DIFF_HSTL_I_DCI	0.85	0.94	1.09	1.08	1.40	1.50	1.66	1.64	1.40	1.50	1.66	1.64	ns
DIFF_HSTL_II_18	0.85	0.94	1.09	1.08	1.50	1.62	1.81	1.78	1.50	1.62	1.81	1.78	ns
DIFF_HSTL_II_DCI_18	0.85	0.94	1.09	1.08	1.36	1.46	1.62	1.59	1.36	1.46	1.62	1.59	ns
DIFF_HSTL_II_T_DCI_18	0.85	0.94	1.09	1.08	1.42	1.53	1.68	1.66	1.42	1.53	1.68	1.66	ns
DIFF_HSTL_II	0.85	0.94	1.09	1.08	1.44	1.56	1.74	1.72	1.44	1.56	1.74	1.72	ns
DIFF_HSTL_II_DCI	0.85	0.94	1.09	1.08	1.37	1.49	1.68	1.66	1.37	1.49	1.68	1.66	ns
SSTL2_I_DCI	0.81	0.91	1.06	1.06	1.42	1.53	1.70	1.68	1.42	1.53	1.70	1.68	ns
SSTL2_II_DCI	0.81	0.91	1.06	1.06	1.39	1.50	1.67	1.69	1.39	1.50	1.67	1.69	ns
SSTL2_II_T_DCI	0.81	0.91	1.06	1.06	1.42	1.53	1.70	1.68	1.42	1.53	1.70	1.68	ns
SSTL18_I	0.81	0.91	1.06	1.06	1.47	1.58	1.75	1.73	1.47	1.58	1.75	1.73	ns
SSTL18_II	0.81	0.91	1.06	1.06	1.39	1.50	1.67	1.66	1.39	1.50	1.67	1.66	ns
SSTL18_I_DCI	0.81	0.91	1.06	1.06	1.40	1.51	1.67	1.65	1.40	1.51	1.67	1.65	ns
SSTL18_II_DCI	0.81	0.91	1.06	1.06	1.36	1.47	1.63	1.62	1.36	1.47	1.63	1.62	ns
SSTL18_II_T_DCI	0.81	0.91	1.06	1.06	1.40	1.51	1.67	1.65	1.40	1.51	1.67	1.65	ns
SSTL15_T_DCI	0.81	0.91	1.06	1.06	1.41	1.52	1.68	1.66	1.41	1.52	1.68	1.66	ns
SSTL15_DCI	0.81	0.91	1.06	1.06	1.41	1.52	1.68	1.66	1.41	1.52	1.68	1.66	ns
DIFF_SSTL2_I	0.85	0.94	1.09	1.08	1.49	1.60	1.77	1.74	1.49	1.60	1.77	1.74	ns
DIFF_SSTL2_I_DCI	0.85	0.94	1.09	1.08	1.42	1.53	1.70	1.68	1.42	1.53	1.70	1.68	ns
DIFF_SSTL2_II	0.85	0.94	1.09	1.08	1.42	1.54	1.72	1.71	1.42	1.54	1.72	1.71	ns
DIFF_SSTL2_II_DCI	0.85	0.94	1.09	1.08	1.39	1.50	1.67	1.69	1.39	1.50	1.67	1.69	ns
DIFF_SSTL2_II_T_DCI	0.85	0.94	1.09	1.08	1.42	1.53	1.70	1.68	1.42	1.53	1.70	1.68	ns

Table 44: IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices (Cont'd)

I/O Standard	T _{IOPI}				T _{IOOP}				T _{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
DIFF_SSTL18_I	0.85	0.94	1.09	1.08	1.47	1.58	1.75	1.73	1.47	1.58	1.75	1.73	ns
DIFF_SSTL18_I_DCI	0.85	0.94	1.09	1.08	1.40	1.51	1.67	1.65	1.40	1.51	1.67	1.65	ns
DIFF_SSTL18_II	0.85	0.94	1.09	1.08	1.39	1.50	1.67	1.66	1.39	1.50	1.67	1.66	ns
DIFF_SSTL18_II_DCI	0.85	0.94	1.09	1.08	1.36	1.47	1.63	1.62	1.36	1.47	1.63	1.62	ns
DIFF_SSTL18_II_T_DCI	0.85	0.94	1.09	1.08	1.40	1.51	1.67	1.65	1.40	1.51	1.67	1.65	ns
DIFF_SSTL15	0.81	0.91	1.06	1.06	1.42	1.54	1.71	1.69	1.42	1.54	1.71	1.69	ns
DIFF_SSTL15_DCI	0.81	0.91	1.06	1.06	1.41	1.52	1.68	1.66	1.41	1.52	1.68	1.66	ns
DIFF_SSTL15_T_DCI	0.81	0.91	1.06	1.06	1.41	1.52	1.68	1.66	1.41	1.52	1.68	1.66	ns

Table 45: IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
LVDS_25	0.94	1.09	1.08	1.54	2.16	1.62	1.54	2.16	1.62	ns
LVDSEXT_25	0.94	1.09	1.08	1.65	2.20	1.73	1.65	2.20	1.73	ns
HT_25	0.94	1.09	1.08	1.62	2.20	1.69	1.62	2.20	1.69	ns
BLVDS_25	0.94	1.09	1.08	1.50	3.18	1.65	1.50	3.18	1.65	ns
RSDS_25 (point to point)	0.94	1.09	1.08	1.54	2.22	1.62	1.54	2.22	1.62	ns
HSTL_I	0.91	1.06	1.06	1.56	2.44	1.71	1.56	2.44	1.71	ns
HSTL_II	0.91	1.06	1.06	1.56	2.21	1.72	1.56	2.21	1.72	ns
HSTL_III	0.91	1.06	1.06	1.54	2.50	1.69	1.54	2.50	1.69	ns
HSTL_I_18	0.91	1.06	1.06	1.58	2.43	1.72	1.58	2.43	1.72	ns
HSTL_II_18	0.91	1.06	1.06	1.62	2.30	1.78	1.62	2.30	1.78	ns
HSTL_III_18	0.91	1.06	1.06	1.54	2.49	1.69	1.54	2.49	1.69	ns
SSTL2_I	0.91	1.06	1.06	1.60	2.50	1.74	1.60	2.50	1.74	ns
SSTL2_II	0.91	1.06	1.06	1.54	2.49	1.71	1.54	2.49	1.71	ns
SSTL15	0.91	1.06	1.06	1.54	2.07	1.69	1.54	2.07	1.69	ns
LVC MOS25, Slow, 2 mA	0.57	0.66	0.70	5.46	6.01	5.63	5.46	6.01	5.63	ns
LVC MOS25, Slow, 4 mA	0.57	0.66	0.70	3.49	3.79	3.65	3.49	3.79	3.65	ns
LVC MOS25, Slow, 6 mA	0.57	0.66	0.70	2.81	3.08	2.95	2.81	3.08	2.95	ns
LVC MOS25, Slow, 8 mA	0.57	0.66	0.70	2.41	2.72	2.59	2.41	2.72	2.59	ns
LVC MOS25, Slow, 12 mA	0.57	0.66	0.70	1.95	2.23	2.10	1.95	2.23	2.10	ns
LVC MOS25, Slow, 16 mA	0.57	0.66	0.70	2.05	2.29	2.21	2.05	2.29	2.21	ns
LVC MOS25, Slow, 24 mA	0.57	0.66	0.70	1.82	2.24	1.98	1.82	2.24	1.98	ns
LVC MOS25, Fast, 2 mA	0.57	0.66	0.70	5.49	6.04	5.62	5.49	6.04	5.62	ns
LVC MOS25, Fast, 4 mA	0.57	0.66	0.70	3.50	3.82	3.65	3.50	3.82	3.65	ns
LVC MOS25, Fast, 6 mA	0.57	0.66	0.70	2.73	2.99	2.88	2.73	2.99	2.88	ns
LVC MOS25, Fast, 8 mA	0.57	0.66	0.70	2.33	2.65	2.53	2.33	2.65	2.53	ns
LVC MOS25, Fast, 12 mA	0.57	0.66	0.70	1.88	2.08	2.03	1.88	2.08	2.03	ns

Table 45: IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices (Cont'd)

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
LVDCI_DV2_18	0.61	0.72	0.73	1.81	2.36	1.98	1.81	2.36	1.98	ns
LVDCI_DV2_15	0.73	0.85	0.85	1.77	2.30	1.98	1.77	2.30	1.98	ns
LVPECL_25	0.94	1.09	1.08	1.49	2.68	1.64	1.49	2.68	1.64	ns
HSTL_I_12	0.91	1.06	1.06	1.60	2.48	1.74	1.60	2.48	1.74	ns
HSTL_I_DCI	0.91	1.06	1.06	1.50	2.43	1.64	1.50	2.43	1.64	ns
HSTL_II_DCI	0.91	1.06	1.06	1.49	2.39	1.66	1.49	2.39	1.66	ns
HSTL_II_T_DCI	0.91	1.06	1.06	1.50	2.43	1.64	1.50	2.43	1.64	ns
HSTL_III_DCI	0.91	1.06	1.06	1.45	2.48	1.61	1.45	2.48	1.61	ns
HSTL_I_DCI_18	0.91	1.06	1.06	1.53	2.44	1.66	1.53	2.44	1.66	ns
HSTL_II_DCI_18	0.91	1.06	1.06	1.46	2.41	1.59	1.46	2.41	1.59	ns
HSTL_II_T_DCI_18	0.91	1.06	1.06	1.53	2.43	1.66	1.53	2.43	1.66	ns
HSTL_III_DCI_18	0.91	1.06	1.06	1.54	2.50	1.67	1.54	2.50	1.67	ns
DIFF_HSTL_I_18	0.94	1.09	1.08	1.58	2.30	1.72	1.58	2.30	1.72	ns
DIFF_HSTL_I_DCI_18	0.94	1.09	1.08	1.53	2.21	1.66	1.53	2.21	1.66	ns
DIFF_HSTL_I	0.94	1.09	1.08	1.56	2.28	1.71	1.56	2.28	1.71	ns
DIFF_HSTL_I_DCI	0.94	1.09	1.08	1.50	2.28	1.64	1.50	2.28	1.64	ns
DIFF_HSTL_II_18	0.94	1.09	1.08	1.62	2.33	1.78	1.62	2.33	1.78	ns
DIFF_HSTL_II_DCI_18	0.94	1.09	1.08	1.46	2.18	1.59	1.46	2.18	1.59	ns
DIFF_HSTL_II_T_DCI_18	0.94	1.09	1.08	1.53	2.22	1.66	1.53	2.22	1.66	ns
DIFF_HSTL_II	0.94	1.09	1.08	1.56	2.29	1.72	1.56	2.29	1.72	ns
DIFF_HSTL_II_DCI	0.94	1.09	1.08	1.49	2.26	1.66	1.49	2.26	1.66	ns
SSTL2_I_DCI	0.91	1.06	1.06	1.53	2.51	1.68	1.53	2.51	1.68	ns
SSTL2_II_DCI	0.91	1.06	1.06	1.50	2.50	1.69	1.50	2.50	1.69	ns
SSTL2_II_T_DCI	0.91	1.06	1.06	1.53	2.52	1.68	1.53	2.52	1.68	ns
SSTL18_I	0.91	1.06	1.06	1.58	2.48	1.73	1.58	2.48	1.73	ns
SSTL18_II	0.91	1.06	1.06	1.50	2.46	1.66	1.50	2.46	1.66	ns
SSTL18_I_DCI	0.91	1.06	1.06	1.51	2.49	1.65	1.51	2.49	1.65	ns
SSTL18_II_DCI	0.91	1.06	1.06	1.47	2.41	1.62	1.47	2.41	1.62	ns
SSTL18_II_T_DCI	0.91	1.06	1.06	1.51	2.49	1.65	1.51	2.49	1.65	ns
SSTL15_T_DCI	0.91	1.06	1.06	1.52	2.48	1.66	1.52	2.48	1.66	ns
SSTL15_DCI	0.91	1.06	1.06	1.52	2.48	1.66	1.52	2.48	1.66	ns
DIFF_SSTL2_I	0.94	1.09	1.08	1.60	2.34	1.74	1.60	2.34	1.74	ns
DIFF_SSTL2_I_DCI	0.94	1.09	1.08	1.53	2.25	1.68	1.53	2.25	1.68	ns
DIFF_SSTL2_II	0.94	1.09	1.08	1.54	2.29	1.71	1.54	2.29	1.71	ns
DIFF_SSTL2_II_DCI	0.94	1.09	1.08	1.50	2.23	1.69	1.50	2.23	1.69	ns
DIFF_SSTL2_II_T_DCI	0.94	1.09	1.08	1.53	2.26	1.68	1.53	2.26	1.68	ns
DIFF_SSTL18_I	0.94	1.09	1.08	1.58	2.22	1.73	1.58	2.22	1.73	ns
DIFF_SSTL18_I_DCI	0.94	1.09	1.08	1.51	2.30	1.65	1.51	2.30	1.65	ns

Table 57: Block RAM and FIFO Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{RCKK_WE}/T_{RCKC_WE}	Write Enable (WE) input (Block RAM only)	0.44/ 0.19	0.47/ 0.25	0.52/ 0.35	0.67/ 0.24	ns, Min
$T_{RCKK_WREN}/T_{RCKC_WREN}$	WREN FIFO inputs	0.47/ 0.26	0.50/ 0.27	0.55/ 0.30	0.68/ 0.31	ns, Min
$T_{RCKK_RDEN}/T_{RCKC_RDEN}$	RDEN FIFO inputs	0.46/ 0.26	0.50/ 0.27	0.55/ 0.30	0.67/ 0.31	ns, Min
Reset Delays						
T_{RCO_FLAGS}	Reset RST to FIFO Flags/Pointers ⁽¹⁰⁾	0.90	0.98	1.10	1.23	ns, Max
$T_{RCKK_RSTREG}/T_{RCKC_RSTREG}$	FIFO reset timing ⁽¹¹⁾	0.22/ 0.23	0.24/ 0.24	0.28/ 0.26	0.31/ 0.27	ns, Min
Maximum Frequency						
F_{MAX}	Block RAM in TDP and SDP modes (Write First and No Change modes)	600	540	450	340	MHz
	Block RAM (Read First mode)	525	475	400	275	MHz
	Block RAM (SDP mode) ⁽¹²⁾	525	475	400	275	MHz
$F_{MAX_CASCADE}$	Block RAM Cascade (Write First and No Change modes)	550	490	400	300	MHz
	Block RAM Cascade (Read First mode)	475	425	350	235	MHz
F_{MAX_FIFO}	FIFO in all modes	600	540	450	340	MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration	450	400	325	250	MHz

Notes:

1. TRACE will report all of these parameters as T_{RCKO_DO} .
2. T_{RCKO_DOR} includes T_{RCKO_DOW} , T_{RCKO_DOPR} , and T_{RCKO_DOPW} as well as the B port equivalent timing parameters.
3. These parameters also apply to synchronous FIFO with $DO_REG = 0$.
4. T_{RCKO_DO} includes T_{RCKO_DOP} as well as the B port equivalent timing parameters.
5. These parameters also apply to multirate (asynchronous) and synchronous FIFO with $DO_REG = 1$.
6. T_{RCKO_FLAGS} includes the following parameters: T_{RCKO_AEMPTY} , T_{RCKO_AFULL} , T_{RCKO_EMPTY} , T_{RCKO_FULL} , T_{RCKO_RDERR} , T_{RCKO_WRERR} .
7. $T_{RCKO_POINTERS}$ includes both $T_{RCKO_RDCOUNT}$ and $T_{RCKO_WRCOUNT}$.
8. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
9. T_{RCKO_DI} includes both A and B inputs as well as the parity inputs of A and B.
10. T_{RCO_FLAGS} includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
11. The FIFO reset must be asserted for at least three positive clock edges.
12. When using ISE software v12.4 or later, if the RDADDR_COLLISION_HWCONFIG attribute is set to PERFORMANCE or the block RAM is in single-port operation, then the faster F_{MAX} for WRITE_FIRST/NO_CHANGE modes apply.

DSP48E1 Switching Characteristics

Table 58: DSP48E1 Switching Characteristics

Symbol	Description	Speed Grade					Units
		-3	-2	-1 (XC)	-1 (XQ)	-1L	
Setup and Hold Times of Data/Control Pins to the Input Register Clock							
$T_{\text{DSPDCK}_{\{A, \text{ACIN}; B, \text{BCIN}\}}_{\{\text{AREG}; \text{BREG}\}}/T_{\text{DSPCKD}_{\{A, \text{ACIN}; B, \text{BCIN}\}}_{\{\text{AREG}; \text{BREG}\}}}$	{A, ACIN, B, BCIN} input to {A, B} register CLK	0.25/ 0.27	0.29/ 0.30	0.35/ 0.34	0.36/ 0.34	0.46/ 0.39	ns
$T_{\text{DSPDCK}_{\text{C_CREG}}/T_{\text{DSPCKD}_{\text{C_CREG}}}}$	C input to C register CLK	0.16/ 0.20	0.19/ 0.22	0.22/ 0.24	0.25/ 0.24	0.33/ 0.30	ns
$T_{\text{DSPDCK}_{\text{D_DREG}}/T_{\text{DSPCKD}_{\text{D_DREG}}}}$	D input to D register CLK	0.07/ 0.31	0.10/ 0.34	0.15/ 0.39	0.16/ 0.39	0.24/ 0.45	ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock							
$T_{\text{DSPDCK}_{\{A, \text{ACIN}, B, \text{BCIN}\}}_{\text{MREG_MULT}}/T_{\text{DSPCKD}_{\{A, \text{ACIN}, B, \text{BCIN}\}}_{\text{MREG_MULT}}}$	{A, ACIN, B, BCIN} input to M register CLK	2.36/ 0.04	2.70/ 0.04	3.21/ 0.04	3.21/ 0.04	3.66/ 0.02	ns
$T_{\text{DSPDCK}_{\{A, D\}}_{\text{ADREG}}/T_{\text{DSPCKD}_{\{A, D\}}_{\text{ADREG}}}$	{A, D} input to AD register CLK	1.24/ 0.10	1.42/ 0.12	1.69/ 0.13	1.69/ 0.13	1.91/ 0.16	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock							
$T_{\text{DSPDCK}_{\{A, \text{ACIN}, B, \text{BCIN}\}}_{\text{PREG_MULT}}/T_{\text{DSPCKD}_{\{A, \text{ACIN}, B, \text{BCIN}\}}_{\text{PREG_MULT}}}$	{A, ACIN, B, BCIN} input to P register CLK using multiplier	3.83/ −0.13	4.37/ −0.13	5.20/ −0.13	5.20/ −0.13	5.94/ −0.24	ns
$T_{\text{DSPDCK}_{\text{D_PREG_MULT}}/T_{\text{DSPCKD}_{\text{D_PREG_MULT}}}}$	D input to P register CLK	3.62/ −0.47	4.13/ −0.47	4.90/ −0.47	4.90/ −0.47	5.61/ −0.77	ns
$T_{\text{DSPDCK}_{\{A, \text{ACIN}, B, \text{BCIN}\}}_{\text{PREG}}/T_{\text{DSPCKD}_{\{A, \text{ACIN}, B, \text{BCIN}\}}_{\text{PREG}}}$	{A, ACIN, B, BCIN} input to P register CLK not using multiplier	1.59/ −0.13	1.81/ −0.13	2.15/ −0.13	2.15/ −0.13	2.44/ −0.24	ns
$T_{\text{DSPDCK}_{\text{C_PREG}}/T_{\text{DSPCKD}_{\text{C_PREG}}}}$	C input to P register CLK	1.42/ −0.10	1.61/ −0.10	1.91/ −0.10	1.91/ −0.10	2.16/ −0.19	ns
$T_{\text{DSPDCK}_{\{\text{PCIN}, \text{CARRYCASCIN}, \text{MULTSIGNIN}\}}_{\text{PREG}}/T_{\text{DSPCKD}_{\{\text{PCIN}, \text{CARRYCASCIN}, \text{MULTSIGNIN}\}}_{\text{PREG}}}$	{PCIN, CARRYCASCIN, MULTSIGNIN} input to P register CLK	1.23/ −0.02	1.41/ −0.02	1.67/ −0.02	1.67/ −0.02	1.91/ −0.07	ns
Setup and Hold Times of the CE Pins							
$T_{\text{DSPDCK}_{\{\text{CEA}; \text{CEB}\}}_{\{\text{AREG}; \text{BREG}\}}/T_{\text{DSPCKD}_{\{\text{CEA}; \text{CEB}\}}_{\{\text{AREG}; \text{BREG}\}}}$	{CEA; CEB} input to {A; B} register CLK	0.14/ 0.19	0.17/ 0.22	0.22/ 0.25	0.22/ 0.25	0.30/ 0.28	ns
$T_{\text{DSPDCK}_{\text{CEC_CREG}}/T_{\text{DSPCKD}_{\text{CEC_CREG}}}}$	CEC input to C register CLK	0.15/ 0.18	0.18/ 0.20	0.24/ 0.23	0.24/ 0.23	0.31/ 0.26	ns
$T_{\text{DSPDCK}_{\text{CED_DREG}}/T_{\text{DSPCKD}_{\text{CED_DREG}}}}$	CED input to D register CLK	0.20/ 0.12	0.24/ 0.13	0.31/ 0.14	0.31/ 0.14	0.43/ 0.16	ns
$T_{\text{DSPDCK}_{\text{CEM_MREG}}/T_{\text{DSPCKD}_{\text{CEM_MREG}}}}$	CEM input to M register CLK	0.16/ 0.19	0.20/ 0.21	0.26/ 0.25	0.26/ 0.25	0.32/ 0.28	ns
$T_{\text{DSPDCK}_{\text{CEP_PREG}}/T_{\text{DSPCKD}_{\text{CEP_PREG}}}}$	CEP input to P register CLK	0.32/ 0.02	0.38/ 0.02	0.46/ 0.03	0.46/ 0.03	0.54/ 0.04	ns
Setup and Hold Times of the RST Pins							
$T_{\text{DSPDCK}_{\{\text{RSTA}; \text{RSTB}\}}_{\{\text{AREG}; \text{BREG}\}}/T_{\text{DSPCKD}_{\{\text{RSTA}; \text{RSTB}\}}_{\{\text{AREG}; \text{BREG}\}}}$	{RSTA, RSTB} input to {A, B} register CLK	0.27/ 0.17	0.31/ 0.19	0.38/ 0.22	0.38/ 0.22	0.41/ 0.25	ns
$T_{\text{DSPDCK}_{\text{RSTC_CREG}}/T_{\text{DSPCKD}_{\text{RSTC_CREG}}}}$	RSTC input to C register CLK	0.18/ 0.08	0.20/ 0.08	0.23/ 0.09	0.23/ 0.09	0.27/ 0.11	ns
$T_{\text{DSPDCK}_{\text{RSTD_DREG}}/T_{\text{DSPCKD}_{\text{RSTD_DREG}}}}$	RSTD input to D register CLK	0.28/ 0.15	0.32/ 0.16	0.38/ 0.19	0.38/ 0.19	0.45/ 0.21	ns
$T_{\text{DSPDCK}_{\text{RSTM_MREG}}/T_{\text{DSPCKD}_{\text{RSTM_MREG}}}}$	RSTM input to M register CLK	0.20/ 0.24	0.23/ 0.26	0.26/ 0.30	0.26/ 0.30	0.29/ 0.34	ns

Table 59: Configuration Switching Characteristics (Cont'd)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
$T_{\text{MMCMDCK_DI}}/$ $T_{\text{MMCCKD_DI}}$	DI Setup/Hold	1.25/ 0.00	1.40/ 0.00	1.63/ 0.00	1.64/ 0.00	ns
$T_{\text{MMCMDCK_DEN}}/$ $T_{\text{MMCCKD_DEN}}$	DEN Setup/Hold time	1.25/ 0.00	1.40/ 0.00	1.63/ 0.00	1.64/ 0.00	ns
$T_{\text{MMCMDCK_DWE}}/$ $T_{\text{MMCCKD_DWE}}$	DWE Setup/Hold time	1.25/ 0.00	1.40/ 0.00	1.63/ 0.00	1.64/ 0.00	ns
$T_{\text{MMCCKO_DO}}$	CLK to out of DO ⁽³⁾	2.60	3.02	3.64	3.68	ns
$T_{\text{MMCCKO_DRDY}}$	CLK to out of DRDY	0.32	0.34	0.38	0.38	ns

Notes:

1. To support longer delays in configuration, use the design solutions described in [UG360: Virtex-6 FPGA Configuration User Guide](#).
2. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.
3. DO will hold until next DRP operation.

Clock Buffers and Networks

Table 60: Global Clock Switching Characteristics (Including BUFGCTRL)

Symbol	Description	Devices	Speed Grade				Units
			-3	-2	-1	-1L	
$T_{\text{BCCCK_CE}}/T_{\text{BCCCK_CE}}^{(1)}$	CE pins Setup/Hold	All	0.11/ 0.00	0.13/ 0.00	0.16/ 0.00	0.13/ 0.00	ns
$T_{\text{BCCCK_S}}/T_{\text{BCCCK_S}}^{(1)}$	S pins Setup/Hold	All	0.11/ 0.00	0.13/ 0.00	0.16/ 0.00	0.13/ 0.00	ns
$T_{\text{BCKO_O}}^{(2)}$	BUFGCTRL delay from I0/I1 to O	All	0.07	0.08	0.10	0.10	ns
Maximum Frequency							
F_{MAX}	Global clock tree (BUFG)	All except LX760	800	750	700	667	MHz
		LX760	N/A	700	700	667	MHz

Notes:

1. $T_{\text{BCCCK_CE}}$ and $T_{\text{BCCCK_S}}$ must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX_VIRTEX4 primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. $T_{\text{BCKO_O}}$ (BUFG delay from I0 to O) values are the same as $T_{\text{BCKO_O}}$ values.

Table 61: Input/Output Clock Switching Characteristics (BUFIO)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
$T_{\text{BIOCKO_O}}$	Clock to out delay from I to O	0.14	0.16	0.18	0.21	ns
Maximum Frequency						
F_{MAX}	I/O clock tree (BUFIO)	800	800	710	710	MHz

Table 62: Regional Clock Switching Characteristics (BUFR)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
$T_{\text{BRCKO_O}}$	Clock to out delay from I to O	0.56	0.62	0.73	0.82	ns
$T_{\text{BRCKO_O_BYP}}$	Clock to out delay from I to O with Divide Bypass attribute set	0.28	0.31	0.36	0.41	ns

Table 62: Regional Clock Switching Characteristics (BUFR) (Cont'd)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{BRDO_O}	Propagation delay from CLR to O	0.69	0.74	0.80	1.12	ns
Maximum Frequency						
$F_{MAX}^{(1)}$	Regional clock tree (BUFR)	500	420	300	300	MHz

Notes:

1. The maximum input frequency to the BUFR is the BUFIO F_{MAX} frequency.

Table 63: Horizontal Clock Buffer Switching Characteristics (BUFH)

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{BHCKO_O}	BUFH delay from I to O	0.10	0.11	0.13	0.15	ns
T_{BHCK_CE}/T_{BHCK_CE}	CE pin Setup and Hold	0.04/ 0.04	0.04/ 0.04	0.05/ 0.05	0.04/ 0.04	ns
Maximum Frequency						
F_{MAX}	Horizontal clock buffer (BUFH)	800	750	700	667	MHz

MMCM Switching Characteristics

Table 64: MMCM Specification

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
F_{INMAX}	Maximum Input Clock Frequency ⁽¹⁾	800	750	700	700	MHz
F_{INMIN}	Minimum Input Clock Frequency	10	10	10	10	MHz
$F_{INJITTER}$	Maximum Input Clock Period Jitter	< 20% of clock input period or 1 ns Max				
$F_{INDUTY}^{(2)}$	Allowable Input Duty Cycle: 10—49 MHz	25/75				%
	Allowable Input Duty Cycle: 50—199 MHz	30/70				%
	Allowable Input Duty Cycle: 200—399 MHz	35/65				%
	Allowable Input Duty Cycle: 400—499 MHz	40/60				%
	Allowable Input Duty Cycle: >500 MHz	45/55				%
F_{MIN_PSCLK}	Minimum Dynamic Phase Shift Clock Frequency	0.01	0.01	0.01	0.01	MHz
F_{MAX_PSCLK}	Maximum Dynamic Phase Shift Clock Frequency	550	500	450	450	MHz
F_{VCOMIN}	Minimum MMCM VCO Frequency	600	600	600	600	MHz
F_{VCOMAX}	Maximum MMCM VCO Frequency	1600	1440	1200	1200	MHz
$F_{BANDWIDTH}$	Low MMCM Bandwidth at Typical ⁽³⁾	1.00	1.00	1.00	1.00	MHz
	High MMCM Bandwidth at Typical ⁽³⁾	4.00	4.00	4.00	4.00	MHz
$T_{STATPHAOFFSET}$	Static Phase Offset of the MMCM Outputs ⁽⁴⁾	0.12	0.12	0.12	0.12	ns
$T_{OUTJITTER}$	MMCM Output Jitter ⁽⁵⁾	Note 3				
$T_{OUTDUTY}$	MMCM Output Clock Duty Cycle Precision ⁽⁶⁾	0.15	0.20	0.20	0.20	ns
$T_{LOCKMAX}$	MMCM Maximum Lock Time	100	100	100	100	μs
F_{OUTMAX}	MMCM Maximum Output Frequency	800	750	700	700	MHz
F_{OUTMIN}	MMCM Minimum Output Frequency ⁽⁷⁾⁽⁸⁾	4.69	4.69	4.69	4.69	MHz
$T_{EXTFDVAR}$	External Clock Feedback Variation	< 20% of clock input period or 1 ns Max				

Table 69: Global Clock Input Setup and Hold With MMCM

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard. ⁽¹⁾							
T _{PSMMCMGC} / T _{PHMMCMGC}	No Delay Global Clock Input and IFF ⁽²⁾ with MMCM	XC6VLX75T	1.45/ −0.18	1.57/ −0.18	1.72/ −0.18	1.78/ −0.08	ns
		XC6VLX130T	1.53/ −0.18	1.65/ −0.18	1.81/ −0.18	1.87/ −0.07	ns
		XC6VLX195T	1.54/ −0.17	1.66/ −0.17	1.82/ −0.17	1.87/ −0.08	ns
		XC6VLX240T	1.54/ −0.17	1.66/ −0.17	1.82/ −0.17	1.87/ −0.08	ns
		XC6VLX365T	1.55/ −0.18	1.67/ −0.18	1.83/ −0.18	1.87/ −0.07	ns
		XC6VLX550T	N/A	1.84/ −0.17	2.02/ −0.17	2.06/ −0.06	ns
		XC6VLX760	N/A	2.26/ −0.13	2.49/ −0.13	2.06/ −0.03	ns
		XC6VSX315T	1.56/ −0.18	1.68/ −0.18	1.84/ −0.18	1.89/ −0.08	ns
		XC6VSX475T	N/A	1.85/ −0.23	2.03/ −0.23	2.07/ −0.13	ns
		XC6VHX250T	1.52/ −0.17	1.64/ −0.17	1.80/ −0.17	N/A	ns
		XC6VHX255T	1.52/ −0.12	1.64/ −0.12	1.85/ −0.12	N/A	ns
		XC6VHX380T	1.68/ −0.16	1.81/ −0.16	1.99/ −0.16	N/A	ns
		XC6VHX565T	N/A	1.81/ −0.01	1.99/ −0.01	N/A	ns
		XQ6VLX130T	N/A	1.65/ −0.18	1.81/ −0.18	1.87/ −0.07	ns
		XQ6VLX240T	N/A	1.66/ −0.17	1.82/ −0.17	1.87/ −0.08	ns
		XQ6VLX550T	N/A	N/A	2.02/ −0.17	2.06/ −0.06	ns
		XQ6VSX315T	N/A	1.68/ −0.18	1.84/ −0.18	1.89/ −0.08	ns
		XQ6VSX475T	N/A	N/A	2.03/ −0.23	2.07/ −0.13	ns

Notes:

- Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
- IFF = Input Flip-Flop or Latch
- Use IBIS to determine any duty-cycle distortion incurred using various standards.

Clock Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-6 FPGA clock transmitter and receiver data-valid windows.

Table 71: Duty Cycle Distortion and Clock-Tree Skew

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
T_{DCD_CLK}	Global Clock Tree Duty Cycle Distortion ⁽¹⁾	All	0.12	0.12	0.12	0.12	ns
T_{CKSKEW}	Global Clock Tree Skew ⁽²⁾	XC6VLX75T	0.15	0.16	0.18	0.17	ns
		XC6VLX130T	0.25	0.26	0.29	0.28	ns
		XC6VLX195T	0.26	0.27	0.31	0.30	ns
		XC6VLX240T	0.26	0.27	0.31	0.30	ns
		XC6VLX365T	0.28	0.29	0.31	0.31	ns
		XC6VLX550T	N/A	0.50	0.54	0.54	ns
		XC6VLX760	N/A	0.51	0.56	0.56	ns
		XC6VSX315T	0.27	0.28	0.32	0.30	ns
		XC6VSX475T	N/A	0.39	0.44	0.42	ns
		XC6VHX250T	0.25	0.26	0.29	N/A	ns
		XC6VHX255T	0.35	0.37	0.41	N/A	ns
		XC6VHX380T	0.45	0.47	0.52	N/A	ns
		XC6VHX565T	N/A	0.46	0.51	N/A	ns
		XQ6VLX130T	N/A	0.26	0.29	0.28	ns
		XQ6VLX240T	N/A	0.27	0.31	0.30	ns
		XQ6VLX550T	N/A	N/A	0.54	0.54	ns
		XQ6VSX315T	N/A	0.28	0.32	0.30	ns
		XQ6VSX475T	N/A	N/A	0.44	0.42	ns
T_{DCD_BUFIO}	I/O clock tree duty cycle distortion	All	0.08	0.08	0.08	0.08	ns
T_{BUFIO_SKEW}	I/O clock tree skew across one clock region	All	0.03	0.03	0.03	0.02	ns
T_{BUFIO_SKEW2}	I/O clock tree skew across three clock regions	All	0.10	0.12	0.23	0.12	ns
T_{DCD_BUFR}	Regional clock tree duty cycle distortion	All	0.15	0.15	0.15	0.15	ns

Notes:

- These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
- The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.