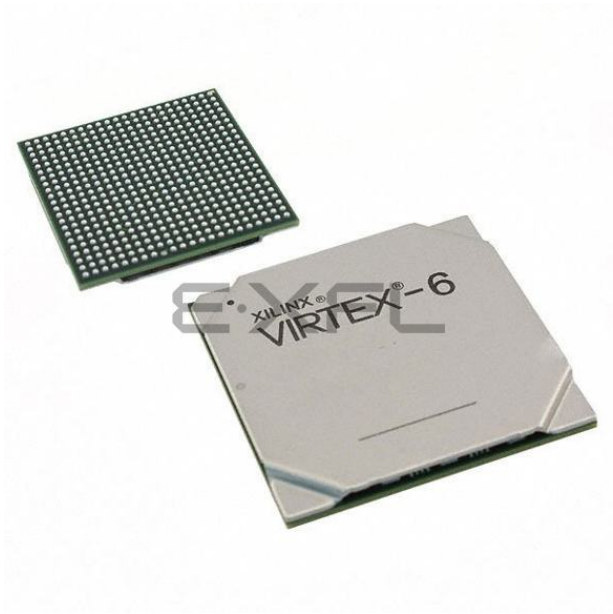
# AMD Xilinx - XC6VSX475T-2FFG1759C Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 37200 |
| Number of Logic Elements/Cells | 476160 |
| Total RAM Bits | 39223296 |
| Number of I/O | 840 |
| Number of Gates | - |
| Voltage - Supply | 0.95V ~ 1.05V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 1759-BBGA, FCBGA |
| Supplier Device Package | 1759-FCBGA (42.5x42.5) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc6vsx475t-2ffg1759c |

*Table 2:* **Recommended Operating Conditions**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $V_{CCINT}$ | Internal supply voltage relative to GND for all devices except -1L devices. | 0.95 | 1.05 | V |
| | For -1L commercial temperature range devices: internal supply voltage relative to GND, $T_j$ = 0°C to +85°C | 0.87 | 0.93 | V |
| | For -1L industrial temperature range devices: internal supply voltage relative to GND, $T_j$ = –40°C to +100°C | 0.91 | 0.97 | V |
| $V_{CCAUX}$ | Auxiliary supply voltage relative to GND | 2.375 | 2.625 | V |
| $V_{CCO}$(1)(2)(3) | Supply voltage relative to GND | 1.14 | 2.625 | V |
| $V_{IN}$ | 2.5V supply voltage relative to GND | GND – 0.20 | 2.625 | V |
| | 2.5V and below supply voltage relative to GND | GND – 0.20 | $V_{CCO}$ + 0.2 | V |
| $I_{IN}$(5) | Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode. | – | 10 | mA |
| $V_{BATT}$(6) | Battery voltage relative to GND | 1.0 | 2.5 | V |
| $V_{FS}$(7) | External voltage supply for eFUSE programming | 2.375 | 2.625 | V |
| $T_j$ | Junction temperature operating range for commercial (C) temperature devices | 0 | 85 | °C |
| | Junction temperature operating range for extended (E) temperature devices | 0 | 100 | °C |
| | Junction temperature operating range for industrial (I) temperature devices | –40 | 100 | °C |
| | Junction temperature operating range for military (M) temperature devices | –55 | 125 | °C |

**Notes:**

1. Configuration data is retained even if $V_{CCO}$ drops to 0V.
2. Includes $V_{CCO}$ of 1.2V, 1.5V, 1.8V, and 2.5V.
3. The configuration supply voltage $V_{CC\_CONFIG}$ is also known as $V_{CCO\_0}$.
4. All voltages are relative to ground.
5. A total of 100 mA per bank should not be exceeded.
6. $V_{BATT}$ is required only when using bitstream encryption. If battery is not used, connect $V_{BATT}$ to either ground or $V_{CCAUX}$.
7. During eFUSE programming, $V_{FS}$ must be within the recommended operating range and $T_j$ = +15°C to +85°C. Otherwise, $V_{FS}$ can be connected to GND.

## Important Note

Typical values for quiescent supply current are specified at nominal voltage, 85°C junction temperatures ($T_j$). Xilinx recommends analyzing static power consumption at $T_j$ = 85°C because the majority of designs operate near the high end of the commercial temperature range. Quiescent supply current is specified by speed grade for Virtex-6 devices. Use the XPower™ Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate static power consumption for conditions other than those specified in Table 4.

*Table 4:* **Typical Quiescent Supply Current**

| Symbol | Description | Device | Speed and Temperature Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | -3 (C) | -2 (C, E, & I) | -1 (C & I) | -1 (I & M)(2) | -1L (C) | -1L (I)(1) | |
| $I_{CCINTQ}$ | Quiescent $V_{CCINT}$ supply current | XC6VLX75T | 927 | 927 | 927 | N/A | 656 | 741 | mA |
| | | XC6VLX130T | 1563 | 1563 | 1563 | N/A | 1102 | 1245 | mA |
| | | XC6VLX195T | 2059 | 2059 | 2059 | N/A | 1441 | 1628 | mA |
| | | XC6VLX240T | 2478 | 2478 | 2478 | N/A | 1733 | 1957 | mA |
| | | XC6VLX365T | 3001 | 3001 | 3001 | N/A | 2092 | 2363 | mA |
| | | XC6VLX550T(3) | N/A | 4515 | 4515 | N/A | 3147 | 3555 | mA |
| | | XC6VLX760(3) | N/A | 5094 | 5094 | N/A | 3471 | 3921 | mA |
| | | XC6VSX315T | 3476 | 3476 | 3476 | N/A | 2409 | 2721 | mA |
| | | XC6VSX475T(3) | N/A | 5227 | 5227 | N/A | 3622 | 4091 | mA |
| | | XC6VHX250T | 2906 | 2906 | 2906 | N/A | N/A | N/A | mA |
| | | XC6VHX255T | 2746 | 2746 | 2746 | N/A | N/A | N/A | mA |
| | | XC6VHX380T(4) | 4160 | 4160 | 4160 | N/A | N/A | N/A | mA |
| | | XC6VHX565T(5) | N/A | 5207 | 5207 | N/A | N/A | N/A | mA |
| | | XQ6VLX130T | N/A | 1563 | N/A | 1563 | N/A | 1245 | mA |
| | | XQ6VLX240T | N/A | 2478 | N/A | 2478 | N/A | 1957 | mA |
| | | XQ6VLX550T(7) | N/A | N/A | N/A | 4515 | N/A | 3555 | mA |
| | | XQ6VSX315T | N/A | 3476 | N/A | 3476 | N/A | 2721 | mA |
| | | XQ6VSX475T(7) | N/A | N/A | N/A | 5227 | N/A | 4091 | mA |

*Table 4:* **Typical Quiescent Supply Current *(Cont'd)***

| Symbol | Description | Device | Speed and Temperature Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | -3 (C) | -2 (C, E, & I) | -1 (C & I) | -1 (I & M)(2) | -1L (C) | -1L (I)(1) | |
| $I_{CCAUXQ}$ | Quiescent $V_{CCAUX}$ supply current | XC6VLX75T | 45 | 45 | 45 | N/A | 45 | 45 | mA |
| | | XC6VLX130T | 75 | 75 | 75 | N/A | 75 | 75 | mA |
| | | XC6VLX195T | 113 | 113 | 113 | N/A | 113 | 113 | mA |
| | | XC6VLX240T | 135 | 135 | 135 | N/A | 135 | 135 | mA |
| | | XC6VLX365T | 191 | 191 | 191 | N/A | 191 | 191 | mA |
| | | XC6VLX550T(3) | N/A | 286 | 286 | N/A | 286 | 286 | mA |
| | | XC6VLX760(3) | N/A | 387 | 387 | N/A | 387 | 387 | mA |
| | | XC6VSX315T | 186 | 186 | 186 | N/A | 186 | 186 | mA |
| | | XC6VSX475T(3) | N/A | 279 | 279 | N/A | 279 | 279 | mA |
| | | XC6VHX250T | 152 | 152 | 152 | N/A | N/A | N/A | mA |
| | | XC6VHX255T | 152 | 152 | 152 | N/A | N/A | N/A | mA |
| | | XC6VHX380T(4) | 227 | 227 | 227 | N/A | N/A | N/A | mA |
| | | XC6VHX565T(5) | N/A | 315 | 315 | N/A | N/A | N/A | mA |
| | | XQ6VLX130T(6) | N/A | 75 | N/A | 75 | N/A | 75 | mA |
| | | XQ6VLX240T(6) | N/A | 135 | N/A | 135 | N/A | 135 | mA |
| | | XQ6VLX550T(7) | N/A | N/A | N/A | 286 | N/A | 286 | mA |
| | | XQ6VSX315T(6) | N/A | 186 | N/A | 186 | N/A | 186 | mA |
| | | XQ6VSX475T(7) | N/A | N/A | N/A | 279 | N/A | 279 | mA |

**Notes:**

1. Typical values are specified at nominal voltage, 85°C junction temperatures ($T_j$). -1 and -2 industrial (I) grade devices have the same typical values as commercial (C) grade devices at 85°C, but higher values at 100°C. Use the XPE tool to calculate 100°C values. -1L industrial temperature range devices have the values specified in this column.
2. Use the XPE tool to calculate 125°C values for -1M temperature range devices.
3. The -2E extended temperature range ($T_j$ = 0°C to +100°C) is only available in these devices. The -2I temperature range ($T_j$ = –40°C to +100°C) is available for all other devices except the XC6VHX565T.
4. The XC6VHX380T is available with both -2E and -2I temperature ranges.
5. The XC6VHX565T is only available in the following temperature ranges: -1C, -1I, -2C, and -2E.
6. The XQ6VLX130T, XQ6VLX240T, and XQ6VSX315T are available in -2I, -1I, -1M, and -1LI temperature ranges.
7. The XQ6VLX550T and the XQ6VSX475T are only available in -1I and -1LI temperature ranges.
8. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
9. If DCI or differential signaling is used, more accurate quiescent current estimates can be obtained by using the XPE or XPower Analyzer (XPA) tools.

## Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on sequence and ramp rate of the power supply.

The recommended power-on sequence for Virtex-6 devices is $V_{CCINT}$, $V_{CCAUX}$, and $V_{CCO}$ to meet the power-up current requirements listed in Table 5. $V_{CCINT}$ can be powered up or down at any time, but power up current specifications can vary from Table 5. The device will have no physical damage or reliability concerns if $V_{CCINT}$, $V_{CCAUX}$, and $V_{CCO}$ sequence cannot be followed.

If the recommended power-up sequence cannot be followed and the I/Os must remain 3-stated throughout configuration, then $V_{CCAUX}$ must be powered prior to $V_{CCO}$ or $V_{CCAUX}$ and $V_{CCO}$ must be powered by the same supply. Similarly, for power-down, the reverse $V_{CCAUX}$ and $V_{CCO}$ sequence is recommended if the I/Os are to remain 3-stated.

The GTH transceiver supplies must be powered using a MGTHAVCC, MGTHAVCCRX, MGTHAVCCPLL, and MGTHAVTT sequence. There are no sequencing requirement for these supplies with respect to the other FPGA supply voltages. For more detail see Table 27: *GTH Transceiver Power Supply Sequencing*. There are no sequencing requirements for the GTX transceivers power supplies.

Table 5 shows the minimum current, in addition to $I_{CCQ}$, that are required by Virtex-6 devices for proper power-on and configuration. If the current minimums shown in Table 4 and Table 5 are met, the device powers on after all three supplies have passed through their power-on reset threshold voltages. The FPGA must be configured after applying $V_{CCINT}$, $V_{CCAUX}$, and $V_{CCO}$ for the appropriate configuration banks. Once initialized and configured, use the XPE tools to estimate current drain on these supplies.

*Table 5:* **Power-On Current for Virtex-6 Devices**

| Device | $I_{CCINTMIN}$ | $I_{CCAUXMIN}$ | $I_{CCOMIN}$ | Units |
|---|---|---|---|---|
| | Typ(1) | Typ(1) | Typ(1) | |
| XC6VLX75T | See $I_{CCINTQ}$ in Table 4 | $I_{CCAUXQ}$ + 10 | $I_{CCOQ}$ + 30 mA per bank | mA |
| XC6VLX130T | See $I_{CCINTQ}$ in Table 4 | $I_{CCAUXQ}$ + 10 | $I_{CCOQ}$ + 30 mA per bank | mA |
| XC6VLX195T | See $I_{CCINTQ}$ in Table 4 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 30 mA per bank | mA |
| XC6VLX240T | See $I_{CCINTQ}$ in Table 4 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 30 mA per bank | mA |
| XC6VLX365T | See $I_{CCINTQ}$ in Table 4 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 30 mA per bank | mA |
| XC6VLX550T | See $I_{CCINTQ}$ in Table 4 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 30 mA per bank | mA |
| XC6VLX760 | See $I_{CCINTQ}$ in Table 4 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 30 mA per bank | mA |
| XC6VSX315T | See $I_{CCINTQ}$ in Table 4 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 30 mA per bank | mA |
| XC6VSX475T | See $I_{CCINTQ}$ in Table 4 | $I_{CCAUXQ}$ + 50 | $I_{CCOQ}$ + 30 mA per bank | mA |
| XC6VHX250T | See $I_{CCINTQ}$ in Table 4 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 30 mA per bank | mA |
| XC6VHX255T | See $I_{CCINTQ}$ in Table 4 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 30 mA per bank | mA |
| XC6VHX380T | See $I_{CCINTQ}$ in Table 4 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 30 mA per bank | mA |
| XC6VHX565T | See $I_{CCINTQ}$ in Table 4 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 30 mA per bank | mA |
| XQ6VLX130T | See $I_{CCINTQ}$ in Table 4 | $I_{CCAUXQ}$ + 100 | $I_{CCOQ}$ + 30 mA per bank | mA |
| XQ6VLX240T | See $I_{CCINTQ}$ in Table 4 | $I_{CCAUXQ}$ + 100 | $I_{CCOQ}$ + 30 mA per bank | mA |
| XQ6VLX550T | See $I_{CCINTQ}$ in Table 4 | $I_{CCAUXQ}$ + 100 | $I_{CCOQ}$ + 30 mA per bank | mA |
| XQ6VSX315T | See $I_{CCINTQ}$ in Table 4 | $I_{CCAUXQ}$ + 100 | $I_{CCOQ}$ + 40 mA per bank | mA |
| XQ6VSX475T | See $I_{CCINTQ}$ in Table 4 | $I_{CCAUXQ}$ + 100 | $I_{CCOQ}$ + 40 mA per bank | mA |

**Notes:**

1. Typical values are specified at nominal voltage, 25°C.
2. Use the XPower Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate maximum power-on currents.

*Table 23:* **GTX Transceiver Transmitter Switching Characteristics**

| Symbol | Description | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{GTXTX}$ | Serial data rate range | | 0.480 | – | $F_{GTXMAX}$ | Gb/s |
| $T_{RTX}$ | TX Rise time | 20%–80% | – | 120 | – | ps |
| $T_{FTX}$ | TX Fall time | 80%–20% | – | 120 | – | ps |
| $T_{LLSKEW}$ | TX lane-to-lane skew(1) | | – | – | 350 | ps |
| $V_{TXOOBVDPP}$ | Electrical idle amplitude | | – | – | 15 | mV |
| $T_{TXOOBTRANSITION}$ | Electrical idle transition time | | – | – | 75 | ns |
| $TJ_{6.5}$ | Total Jitter(2)(3) | 6.5 Gb/s | – | – | 0.33 | UI |
| $DJ_{6.5}$ | Deterministic Jitter(2)(3) | | – | – | 0.17 | UI |
| $TJ_{5.0}$ | Total Jitter(2)(3) | 5.0 Gb/s | – | – | 0.33 | UI |
| $DJ_{5.0}$ | Deterministic Jitter(2)(3) | | – | – | 0.15 | UI |
| $TJ_{4.25}$ | Total Jitter(2)(3) | 4.25 Gb/s | – | – | 0.33 | UI |
| $DJ_{4.25}$ | Deterministic Jitter(2)(3) | | – | – | 0.14 | UI |
| $TJ_{3.75}$ | Total Jitter(2)(3) | 3.75 Gb/s | – | – | 0.34 | UI |
| $DJ_{3.75}$ | Deterministic Jitter(2)(3) | | – | – | 0.16 | UI |
| $TJ_{3.125}$ | Total Jitter(2)(3) | 3.125 Gb/s | – | – | 0.2 | UI |
| $DJ_{3.125}$ | Deterministic Jitter(2)(3) | | – | – | 0.1 | UI |
| $TJ_{3.125L}$ | Total Jitter(2)(3) | 3.125 Gb/s(4) | – | – | 0.35 | UI |
| $DJ_{3.125L}$ | Deterministic Jitter(2)(3) | | – | – | 0.16 | UI |
| $TJ_{2.5}$ | Total Jitter(2)(3) | 2.5 Gb/s(5) | – | – | 0.20 | UI |
| $DJ_{2.5}$ | Deterministic Jitter(2)(3) | | – | – | 0.08 | UI |
| $TJ_{1.25}$ | Total Jitter(2)(3) | 1.25 Gb/s(6) | – | – | 0.15 | UI |
| $DJ_{1.25}$ | Deterministic Jitter(2)(3) | | – | – | 0.06 | UI |
| $TJ_{600}$ | Total Jitter(2)(3) | 600 Mb/s | – | – | 0.1 | UI |
| $DJ_{600}$ | Deterministic Jitter(2)(3) | | – | – | 0.03 | UI |
| $TJ_{480}$ | Total Jitter(2)(3) | 480 Mb/s | – | – | 0.1 | UI |
| $DJ_{480}$ | Deterministic Jitter(2)(3) | | – | – | 0.03 | UI |

**Notes:**

1. Using same REFCLK input with TXENPMAPHASEALIGN enabled for up to 12 consecutive transmitters (three fully populated GTX Quads).
2. Using PLL_DIVSEL_FB = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. All jitter values are based on a bit-error ratio of $1e^{-12}$.
4. PLL frequency at 1.5625 GHz and OUTDIV = 1.
5. PLL frequency at 2.5 GHz and OUTDIV = 2.
6. PLL frequency at 2.5 GHz and OUTDIV = 4.

# GTH Transceiver Specifications

## GTH Transceiver DC Characteristics

*Table 25:* **Absolute Maximum Ratings for GTH Transceivers(1)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| MGTHAVCC | Analog supply voltage for the GTH transmitter, receiver, and common analog circuits | –0.5 | 1.125 | V |
| MGTHAVCCRX | Analog supply voltage for the GTH receiver circuits and common analog circuits | –0.5 | 1.125 | V |
| MGTHAVTT | Analog supply voltage for the GTH transmitter termination circuits | –0.5 | 1.32 | V |
| MGTHAVCCPLL | Analog supply voltage for the GTH receiver and PLL circuits | –0.5 | 1.935 | V |
| $V_{IN}$ | Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage | –0.5 | 1.125 | V |
| $V_{MGTREFCLK}$ | Reference clock absolute input voltage | –0.5 | 1.935 | V |

**Notes:**

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

*Table 26:* **Recommended Operating Conditions for GTH Transceivers (1)(2)**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| MGTHAVCC | Analog supply voltage for the GTH transmitter, receiver, and common analog circuits | 1.075 | 1.1 | 1.125 | V |
| MGTHAVCCRX | Analog supply voltage for the GTH receiver circuits and common analog circuits | 1.075 | 1.1 | 1.125 | V |
| MGTHAVTT | Analog supply voltage for the GTH transmitter termination circuits | 1.140 | 1.2 | 1.26 | V |
| MGTHAVCCPLL | Analog supply voltage for the GTH receiver and PLL circuit | 1.710 | 1.8 | 1.89 | V |

**Notes:**

1. Each voltage listed requires the filter circuit described in UG371: *Virtex-6 FPGA GTH Transceivers User Guide*.
2. Voltages are specified for the temperature range of $T_j$ = –40°C to +100°C.

*Table 27:* **GTH Transceiver Power Supply Sequencing (1)(2)(3)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{HAVCC2HAVCCRX}$ | Maximum time between powering MGTHAVCC to when MGTHAVCCRX must be powered. | 0 | 5 | ms |
| $T_{HAVCCRX2HAVCCPLL}$ | Minimum time between powering MGTHAVCCRX to when MGTHAVCCPLL can be powered. | 10 | – | µs |
| $T_{HAVCCRX2HAVTT}$ | Minimum time between powering MGTHAVCCRX to when MGTHAVTT can be powered. | 10 | – | µs |

**Notes:**

1. MGTHAVCCRX must be powered simultaneously or within $T_{HAVCC2HAVCCRX}$ of MGTHAVCC, but it must not precede MGTHAVCC.
2. MGTHAVCC and MGTHAVCCRX must be powered before MGTHAVCCPLL and MGTHAVTT. This minimum time is defined by $T_{HAVCCRX2HAVCCPLL}$ and $T_{HAVCCRX2HAVTT}$.
3. At any time, the condition of MGTHAVCC being present and MGTHAVCCRX not being present should not occur for more than the maximum $T_{HAVCC2HAVCCRX}$.

## GTH Transceiver DC Input and Output Levels

Table 30 summarizes the DC output specifications of the GTH transceivers in Virtex-6 FPGAs. Consult UG371: *Virtex-6 FPGA GTH Transceivers User Guide* for further details.

*Table 30:* **GTH Transceiver DC Specifications**

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $D_{VPPIN}$ | Differential peak-to-peak input voltage | External AC coupled | 175 | – | 1200 | mV |
| $D_{VPPOUT}$ | Differential peak-to-peak output voltage(1) | Transmitter output swing is set to maximum setting | 800 | – | 1200 | mV |
| $R_{IN}$ | Differential input resistance | | 80 | 100 | 120 | Ω |
| $R_{OUT}$ | Differential output resistance | | 80 | 100 | 120 | Ω |
| $T_{OSKEW}$ | Transmitter output pair (TXP and TXN) intra-pair skew | | – | 2 | – | ps |
| $C_{EXT}$ | Recommended external AC coupling capacitor(2) | | – | 100 | – | nF |

**Notes:**

1. The output swing and preemphasis levels are programmable using the attributes discussed in UG371: *Virtex-6 FPGA GTH Transceivers User Guide* and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

Table 31 summarizes the DC specifications of the clock input of the GTH transceiver. Consult UG371: *Virtex-6 FPGA GTH Transceivers User Guide* for further details.

*Table 31:* **GTH Transceiver Clock DC Input Level Specification**

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IDIFF}$ | Differential peak-to-peak input voltage | ≤ 600 MHz | 500 | – | 1600 | mV |
| | | > 600 MHz | 600 | – | 1600 | mV |
| $R_{IN}$ | Differential input resistance | | 80 | 100 | 120 | Ω |
| $C_{EXT}$ | Required external AC coupling capacitor | | – | 100 | – | nF |

*Table 37:* **GTH Transceiver Receiver Switching Characteristics**

| Symbol | Description | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $R_{XRL}$ | Run length (CID) | | 8000 | – | – | UI |
| $R_{XPPMTOL}$ | Data/REFCLK PPM offset tolerance | | –200 | – | 200 | ppm |
| **SJ Jitter Tolerance**(1)(2)(3)(4) | | | | | | |
| $JT\_SJ_{11.18}$ | Sinusoidal Jitter | 11.18 Gb/s | 0.3 | – | – | UI |
| $JT\_SJ_{10.32}$ | Sinusoidal Jitter | 10.32 Gb/s | 0.3 | – | – | UI |
| $JT\_SJ_{9.95}$ | Sinusoidal Jitter | 9.95 Gb/s | 0.3 | – | – | UI |
| $JT\_SJ_{2.667}$ | Sinusoidal Jitter | 2.667 Gb/s | 0.5 | – | – | UI |
| $JT\_SJ_{2.48}$ | Sinusoidal Jitter | 2.48 Gb/s | 0.5 | – | – | UI |

**Notes:**

1. These values are NOT intended for protocol specific compliance determinations.
2. All jitter values are based on a bit error ratio of $1e^{-12}$.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. High-frequency jitter tolerance including 6 db of channel loss at a high frequency of the data rate divided by two.

## Ethernet MAC Switching Characteristics

Consult UG368: *Virtex-6 FPGA Embedded Tri-mode Ethernet MAC User Guide* for further information.

*Table 38:* **Maximum Ethernet MAC Performance**

| Symbol | Description | Conditions | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1 | -1L | |
| $F_{TEMACCLIENT}$ | Client interface maximum frequency | 10 Mb/s – 8-bit width | 2.5(1) | 2.5(1) | 2.5(1) | 2.5(1) | MHz |
| | | 100 Mb/s – 8-bit width | 25(2) | 25(2) | 25(2) | 25(2) | MHz |
| | | 1000 Mb/s – 8-bit width | 125 | 125 | 125 | 125 | MHz |
| | | 1000 Mb/s – 16-bit width | 62.5 | 62.5 | 62.5 | 62.5 | MHz |
| | | 2000 Mb/s – 16-bit width | 125 | 125 | 125 | N/A | MHz |
| | | 2500 Mb/s – 16-bit width | 156.25 | 156.25 | 156.25 | N/A | MHz |
| $F_{TEMACPHY}$ | Physical interface maximum frequency | 10 Mb/s – 4-bit width | 2.5 | 2.5 | 2.5 | 2.5 | MHz |
| | | 100 Mb/s – 4-bit width | 25 | 25 | 25 | 25 | MHz |
| | | 1000 Mb/s – 8-bit width | 125 | 125 | 125 | 125 | MHz |
| | | 2000 Mb/s – 8-bit width | 250 | 250 | 250 | N/A | MHz |
| | | 2500 Mb/s – 8-bit width | 312.5 | 312.5 | 312.5 | N/A | MHz |

**Notes:**

1. When not using clock enable, the $F_{MAX}$ is lowered to 1.25 MHz.
2. When not using clock enable, the $F_{MAX}$ is lowered to 12.5 MHz.

## Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex-6 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the Switching Characteristics, page 26.

*Table 41:* **Interface Performances**

| Description | Speed Grade | | | |
|---|---|---|---|---|
| | -3 | -2 | -1 | -1L |
| **Networking Applications** | | | | |
| SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8) | 710 Mb/s | 710 Mb/s | 650 Mb/s | 585 Mb/s |
| DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 10) | 1.4 Gb/s | 1.3 Gb/s | 1.25 Gb/s | 1.1 Gb/s |
| SDR LVDS receiver (SFI-4.1)(1) | 710 Mb/s | 710 Mb/s | 650 Mb/s | 585 Mb/s |
| DDR LVDS receiver (SPI-4.2)(1) | 1.4 Gb/s | 1.3 Gb/s | 1.1 Gb/s | 0.9 Gb/s |
| **Maximum Physical Interface (PHY) Rate for Memory Interfaces(2)(3)(4)** | | | | |
| DDR2 | 800 Mb/s | 800 Mb/s | 800 Mb/s | 606 Mb/s |
| DDR3 | 1066 Mb/s | 1066 Mb/s | 800 Mb/s | 800 Mb/s |
| QDR II + SRAM | 400 MHz | 350 MHz | 300 MHz | – |
| RLDRAM II | 500 MHz | 400 MHz | 350 MHz | – |

**Notes:**

1. LVDS receivers are typically bounded with certain applications where specific DPA algorithms dominate deterministic performance.
2. Verified on Xilinx memory characterization platforms designed according to the guidelines in UG: *Virtex-6 FPGA Memory Interface Solutions User Guide*.
3. Consult DS186: *Virtex-6 FPGA Memory Interface Solutions Data Sheet* for performance and feature information on memory interface cores (controller plus PHY).
4. Memory Interface data rates have not been tested over the junction temperature operating range for military (M) temperature devices. Customers are responsible for specifying and testing their specific M temperature grade memory implementation.

## Switching Characteristics

All values represented in this data sheet are based on these speed specifications: v1.17 for -3, -2, and -1; and v1.10 for -1L. Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

### Advance

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

### Preliminary

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

### Production

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device.

Table 42 correlates the current status of each Virtex-6 device on a per speed grade basis.

*Table 42:* **Virtex-6 Device Speed Grade Designations**

| Device | Speed Grade Designations | | |
|---|---|---|---|
| | Advance | Preliminary | Production |
| XC6VLX75T | | | -3, -2, -1, -1L |
| XC6VLX130T | | | -3, -2, -1, -1L |
| XC6VLX195T | | | -3, -2, -1, -1L |
| XC6VLX240T | | | -3, -2, -1, -1L |
| XC6VLX365T | | | -3, -2, -1, -1L |
| XC6VLX550T | | | -2, -1, -1L |
| XC6VLX760 | | | -2, -1, -1L |
| XC6VSX315T | | | -3, -2, -1, -1L |
| XC6VSX475T | | | -2, -1, -1L |
| XC6VHX250T | | | -3, -2, -1 |
| XC6VHX255T | | | -3, -2, -1 |
| XC6VHX380T | | | -3, -2, -1 |
| XC6VHX565T | | | -2, -1 |
| XQ6VLX130T | | | -2, -1, -1L |
| XQ6VLX240T | | | -2, -1, -1L |
| XQ6VLX550T | | | -1, -1L |
| XQ6VSX315T | | | -2, -1, -1L |
| XQ6VSX475T | | | -1, -1L |

## Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-6 devices.

## IOB Pad Input/Output/3-State Switching Characteristics

Table 44 (for commercial (XC) Virtex-6 devices) and Table 45 (for the Defense-grade (XQ) Virtex-6 devices) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

$T_{IOPI}$ is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.

$T_{IOOP}$ is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.

$T_{IOTP}$ is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer.

Table 46 summarizes the value of $T_{IOTPHZ}$. $T_{IOTPHZ}$ is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state).

*Table 44:* **IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices**

| I/O Standard | $T_{IOPI}$ | | | | $T_{IOOP}$ | | | | $T_{IOTP}$ | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | -3 | -2 | -1 | -1L | -3 | -2 | -1 | -1L | -3 | -2 | -1 | -1L | |
| LVDS_25 | 0.85 | 0.94 | 1.09 | 1.08 | 1.45 | 1.54 | 1.68 | 1.62 | 1.45 | 1.54 | 1.68 | 1.62 | ns |
| LVDSEXT_25 | 0.85 | 0.94 | 1.09 | 1.08 | 1.53 | 1.65 | 1.84 | 1.73 | 1.53 | 1.65 | 1.84 | 1.73 | ns |
| HT_25 | 0.85 | 0.94 | 1.09 | 1.08 | 1.51 | 1.62 | 1.78 | 1.69 | 1.51 | 1.62 | 1.78 | 1.69 | ns |
| BLVDS_25 | 0.85 | 0.94 | 1.09 | 1.08 | 1.39 | 1.50 | 1.67 | 1.65 | 1.39 | 1.50 | 1.67 | 1.65 | ns |
| RSDS_25 (point to point) | 0.85 | 0.94 | 1.09 | 1.08 | 1.45 | 1.54 | 1.68 | 1.62 | 1.45 | 1.54 | 1.68 | 1.62 | ns |
| HSTL_I | 0.81 | 0.91 | 1.06 | 1.06 | 1.45 | 1.56 | 1.73 | 1.71 | 1.45 | 1.56 | 1.73 | 1.71 | ns |
| HSTL_II | 0.81 | 0.91 | 1.06 | 1.06 | 1.44 | 1.56 | 1.74 | 1.72 | 1.44 | 1.56 | 1.74 | 1.72 | ns |
| HSTL_III | 0.81 | 0.91 | 1.06 | 1.06 | 1.42 | 1.54 | 1.71 | 1.69 | 1.42 | 1.54 | 1.71 | 1.69 | ns |
| HSTL_I_18 | 0.81 | 0.91 | 1.06 | 1.06 | 1.47 | 1.58 | 1.75 | 1.72 | 1.47 | 1.58 | 1.75 | 1.72 | ns |
| HSTL_II_18 | 0.81 | 0.91 | 1.06 | 1.06 | 1.50 | 1.62 | 1.81 | 1.78 | 1.50 | 1.62 | 1.81 | 1.78 | ns |
| HSTL_III_18 | 0.81 | 0.91 | 1.06 | 1.06 | 1.42 | 1.54 | 1.71 | 1.69 | 1.42 | 1.54 | 1.71 | 1.69 | ns |
| SSTL2_I | 0.81 | 0.91 | 1.06 | 1.06 | 1.49 | 1.60 | 1.77 | 1.74 | 1.49 | 1.60 | 1.77 | 1.74 | ns |
| SSTL2_II | 0.81 | 0.91 | 1.06 | 1.06 | 1.42 | 1.54 | 1.72 | 1.71 | 1.42 | 1.54 | 1.72 | 1.71 | ns |
| SSTL15 | 0.81 | 0.91 | 1.06 | 1.06 | 1.42 | 1.54 | 1.71 | 1.69 | 1.42 | 1.54 | 1.71 | 1.69 | ns |
| LVCMOS25, Slow, 2 mA | 0.51 | 0.57 | 0.66 | 0.70 | 5.09 | 5.46 | 6.01 | 5.63 | 5.09 | 5.46 | 6.01 | 5.63 | ns |
| LVCMOS25, Slow, 4 mA | 0.51 | 0.57 | 0.66 | 0.70 | 3.30 | 3.49 | 3.79 | 3.65 | 3.30 | 3.49 | 3.79 | 3.65 | ns |
| LVCMOS25, Slow, 6 mA | 0.51 | 0.57 | 0.66 | 0.70 | 2.62 | 2.81 | 3.08 | 2.95 | 2.62 | 2.81 | 3.08 | 2.95 | ns |
| LVCMOS25, Slow, 8 mA | 0.51 | 0.57 | 0.66 | 0.70 | 2.21 | 2.41 | 2.72 | 2.59 | 2.21 | 2.41 | 2.72 | 2.59 | ns |
| LVCMOS25, Slow, 12 mA | 0.51 | 0.57 | 0.66 | 0.70 | 1.80 | 1.95 | 2.17 | 2.10 | 1.80 | 1.95 | 2.17 | 2.10 | ns |
| LVCMOS25, Slow, 16 mA | 0.51 | 0.57 | 0.66 | 0.70 | 1.89 | 2.05 | 2.29 | 2.21 | 1.89 | 2.05 | 2.29 | 2.21 | ns |
| LVCMOS25, Slow, 24 mA | 0.51 | 0.57 | 0.66 | 0.70 | 1.68 | 1.82 | 2.02 | 1.98 | 1.68 | 1.82 | 2.02 | 1.98 | ns |
| LVCMOS25, Fast, 2 mA | 0.51 | 0.57 | 0.66 | 0.70 | 5.12 | 5.49 | 6.04 | 5.62 | 5.12 | 5.49 | 6.04 | 5.62 | ns |
| LVCMOS25, Fast, 4 mA | 0.51 | 0.57 | 0.66 | 0.70 | 3.28 | 3.50 | 3.82 | 3.65 | 3.28 | 3.50 | 3.82 | 3.65 | ns |
| LVCMOS25, Fast, 6 mA | 0.51 | 0.57 | 0.66 | 0.70 | 2.56 | 2.73 | 2.99 | 2.88 | 2.56 | 2.73 | 2.99 | 2.88 | ns |
| LVCMOS25, Fast, 8 mA | 0.51 | 0.57 | 0.66 | 0.70 | 2.11 | 2.33 | 2.65 | 2.53 | 2.11 | 2.33 | 2.65 | 2.53 | ns |
| LVCMOS25, Fast, 12 mA | 0.51 | 0.57 | 0.66 | 0.70 | 1.74 | 1.88 | 2.08 | 2.03 | 1.74 | 1.88 | 2.08 | 2.03 | ns |
| LVCMOS25, Fast, 16 mA | 0.51 | 0.57 | 0.66 | 0.70 | 1.77 | 1.92 | 2.13 | 2.08 | 1.77 | 1.92 | 2.13 | 2.08 | ns |

*Table 44:* **IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | | $T_{IOOP}$ | | | | $T_{IOTP}$ | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | -3 | -2 | -1 | -1L | -3 | -2 | -1 | -1L | -3 | -2 | -1 | -1L | |
| DIFF_SSTL18_I | 0.85 | 0.94 | 1.09 | 1.08 | 1.47 | 1.58 | 1.75 | 1.73 | 1.47 | 1.58 | 1.75 | 1.73 | ns |
| DIFF_SSTL18_I_DCI | 0.85 | 0.94 | 1.09 | 1.08 | 1.40 | 1.51 | 1.67 | 1.65 | 1.40 | 1.51 | 1.67 | 1.65 | ns |
| DIFF_SSTL18_II | 0.85 | 0.94 | 1.09 | 1.08 | 1.39 | 1.50 | 1.67 | 1.66 | 1.39 | 1.50 | 1.67 | 1.66 | ns |
| DIFF_SSTL18_II_DCI | 0.85 | 0.94 | 1.09 | 1.08 | 1.36 | 1.47 | 1.63 | 1.62 | 1.36 | 1.47 | 1.63 | 1.62 | ns |
| DIFF_SSTL18_II_T_DCI | 0.85 | 0.94 | 1.09 | 1.08 | 1.40 | 1.51 | 1.67 | 1.65 | 1.40 | 1.51 | 1.67 | 1.65 | ns |
| DIFF_SSTL15 | 0.81 | 0.91 | 1.06 | 1.06 | 1.42 | 1.54 | 1.71 | 1.69 | 1.42 | 1.54 | 1.71 | 1.69 | ns |
| DIFF_SSTL15_DCI | 0.81 | 0.91 | 1.06 | 1.06 | 1.41 | 1.52 | 1.68 | 1.66 | 1.41 | 1.52 | 1.68 | 1.66 | ns |
| DIFF_SSTL15_T_DCI | 0.81 | 0.91 | 1.06 | 1.06 | 1.41 | 1.52 | 1.68 | 1.66 | 1.41 | 1.52 | 1.68 | 1.66 | ns |

*Table 45:* **IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices**

| I/O Standard | $T_{IOPI}$ | | | $T_{IOOP}$ | | | $T_{IOTP}$ | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | Speed Grade | | | Speed Grade | | | |
| | -2 | -1 | -1L | -2 | -1 | -1L | -2 | -1 | -1L | |
| LVDS_25 | 0.94 | 1.09 | 1.08 | 1.54 | 2.16 | 1.62 | 1.54 | 2.16 | 1.62 | ns |
| LVDSEXT_25 | 0.94 | 1.09 | 1.08 | 1.65 | 2.20 | 1.73 | 1.65 | 2.20 | 1.73 | ns |
| HT_25 | 0.94 | 1.09 | 1.08 | 1.62 | 2.20 | 1.69 | 1.62 | 2.20 | 1.69 | ns |
| BLVDS_25 | 0.94 | 1.09 | 1.08 | 1.50 | 3.18 | 1.65 | 1.50 | 3.18 | 1.65 | ns |
| RSDS_25 (point to point) | 0.94 | 1.09 | 1.08 | 1.54 | 2.22 | 1.62 | 1.54 | 2.22 | 1.62 | ns |
| HSTL_I | 0.91 | 1.06 | 1.06 | 1.56 | 2.44 | 1.71 | 1.56 | 2.44 | 1.71 | ns |
| HSTL_II | 0.91 | 1.06 | 1.06 | 1.56 | 2.21 | 1.72 | 1.56 | 2.21 | 1.72 | ns |
| HSTL_III | 0.91 | 1.06 | 1.06 | 1.54 | 2.50 | 1.69 | 1.54 | 2.50 | 1.69 | ns |
| HSTL_I_18 | 0.91 | 1.06 | 1.06 | 1.58 | 2.43 | 1.72 | 1.58 | 2.43 | 1.72 | ns |
| HSTL_II_18 | 0.91 | 1.06 | 1.06 | 1.62 | 2.30 | 1.78 | 1.62 | 2.30 | 1.78 | ns |
| HSTL_III_18 | 0.91 | 1.06 | 1.06 | 1.54 | 2.49 | 1.69 | 1.54 | 2.49 | 1.69 | ns |
| SSTL2_I | 0.91 | 1.06 | 1.06 | 1.60 | 2.50 | 1.74 | 1.60 | 2.50 | 1.74 | ns |
| SSTL2_II | 0.91 | 1.06 | 1.06 | 1.54 | 2.49 | 1.71 | 1.54 | 2.49 | 1.71 | ns |
| SSTL15 | 0.91 | 1.06 | 1.06 | 1.54 | 2.07 | 1.69 | 1.54 | 2.07 | 1.69 | ns |
| LVCMOS25, Slow, 2 mA | 0.57 | 0.66 | 0.70 | 5.46 | 6.01 | 5.63 | 5.46 | 6.01 | 5.63 | ns |
| LVCMOS25, Slow, 4 mA | 0.57 | 0.66 | 0.70 | 3.49 | 3.79 | 3.65 | 3.49 | 3.79 | 3.65 | ns |
| LVCMOS25, Slow, 6 mA | 0.57 | 0.66 | 0.70 | 2.81 | 3.08 | 2.95 | 2.81 | 3.08 | 2.95 | ns |
| LVCMOS25, Slow, 8 mA | 0.57 | 0.66 | 0.70 | 2.41 | 2.72 | 2.59 | 2.41 | 2.72 | 2.59 | ns |
| LVCMOS25, Slow, 12 mA | 0.57 | 0.66 | 0.70 | 1.95 | 2.23 | 2.10 | 1.95 | 2.23 | 2.10 | ns |
| LVCMOS25, Slow, 16 mA | 0.57 | 0.66 | 0.70 | 2.05 | 2.29 | 2.21 | 2.05 | 2.29 | 2.21 | ns |
| LVCMOS25, Slow, 24 mA | 0.57 | 0.66 | 0.70 | 1.82 | 2.24 | 1.98 | 1.82 | 2.24 | 1.98 | ns |
| LVCMOS25, Fast, 2 mA | 0.57 | 0.66 | 0.70 | 5.49 | 6.04 | 5.62 | 5.49 | 6.04 | 5.62 | ns |
| LVCMOS25, Fast, 4 mA | 0.57 | 0.66 | 0.70 | 3.50 | 3.82 | 3.65 | 3.50 | 3.82 | 3.65 | ns |
| LVCMOS25, Fast, 6 mA | 0.57 | 0.66 | 0.70 | 2.73 | 2.99 | 2.88 | 2.73 | 2.99 | 2.88 | ns |
| LVCMOS25, Fast, 8 mA | 0.57 | 0.66 | 0.70 | 2.33 | 2.65 | 2.53 | 2.33 | 2.65 | 2.53 | ns |
| LVCMOS25, Fast, 12 mA | 0.57 | 0.66 | 0.70 | 1.88 | 2.08 | 2.03 | 1.88 | 2.08 | 2.03 | ns |

*Table 45:* **IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | $T_{IOOP}$ | | | $T_{IOTP}$ | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | Speed Grade | | | Speed Grade | | | |
| | -2 | -1 | -1L | -2 | -1 | -1L | -2 | -1 | -1L | |
| DIFF_SSTL18_II | 0.94 | 1.09 | 1.08 | 1.50 | 2.27 | 1.66 | 1.50 | 2.27 | 1.66 | ns |
| DIFF_SSTL18_II_DCI | 0.94 | 1.09 | 1.08 | 1.47 | 2.20 | 1.62 | 1.47 | 2.20 | 1.62 | ns |
| DIFF_SSTL18_II_T_DCI | 0.94 | 1.09 | 1.08 | 1.51 | 2.30 | 1.65 | 1.51 | 2.30 | 1.65 | ns |
| DIFF_SSTL15 | 0.91 | 1.06 | 1.06 | 1.54 | 2.25 | 1.69 | 1.54 | 2.25 | 1.69 | ns |
| DIFF_SSTL15_DCI | 0.91 | 1.06 | 1.06 | 1.52 | 2.25 | 1.66 | 1.52 | 2.25 | 1.66 | ns |
| DIFF_SSTL15_T_DCI | 0.91 | 1.06 | 1.06 | 1.52 | 2.25 | 1.66 | 1.52 | 2.25 | 1.66 | ns |

*Table 46:* **IOB 3-state ON Output Switching Characteristics ($T_{IOTPHZ}$)**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 | -1L | |
| $T_{IOTPHZ}$ | T input to Pad high-impedance | 0.86 | 0.92 | 0.99 | 0.99 | ns |

*Table 54:* **CLB Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 | -1L | |
| $T_{ITO}$ | An – Dn inputs to A – D Q outputs | 0.59 | 0.67 | 0.79 | 0.85 | ns, Max |
| $T_{AXA}$ | AX inputs to AMUX output | 0.31 | 0.35 | 0.42 | 0.44 | ns, Max |
| $T_{AXB}$ | AX inputs to BMUX output | 0.35 | 0.39 | 0.47 | 0.50 | ns, Max |
| $T_{AXC}$ | AX inputs to CMUX output | 0.39 | 0.44 | 0.52 | 0.56 | ns, Max |
| $T_{AXD}$ | AX inputs to DMUX output | 0.42 | 0.47 | 0.55 | 0.60 | ns, Max |
| $T_{BXB}$ | BX inputs to BMUX output | 0.30 | 0.34 | 0.39 | 0.44 | ns, Max |
| $T_{BXD}$ | BX inputs to DMUX output | 0.38 | 0.43 | 0.50 | 0.55 | ns, Max |
| $T_{CXC}$ | CX inputs to CMUX output | 0.26 | 0.29 | 0.34 | 0.37 | ns, Max |
| $T_{CXD}$ | CX inputs to DMUX output | 0.30 | 0.34 | 0.40 | 0.44 | ns, Max |
| $T_{DXD}$ | DX inputs to DMUX output | 0.30 | 0.33 | 0.38 | 0.43 | ns, Max |
| $T_{OPCYA}$ | An input to COUT output | 0.32 | 0.36 | 0.41 | 0.47 | ns, Max |
| $T_{OPCYB}$ | Bn input to COUT output | 0.32 | 0.36 | 0.41 | 0.47 | ns, Max |
| $T_{OPCYC}$ | Cn input to COUT output | 0.27 | 0.30 | 0.34 | 0.40 | ns, Max |
| $T_{OPCYD}$ | Dn input to COUT output | 0.25 | 0.28 | 0.32 | 0.37 | ns, Max |
| $T_{AXCY}$ | AX input to COUT output | 0.25 | 0.28 | 0.33 | 0.36 | ns, Max |
| $T_{BXCY}$ | BX input to COUT output | 0.22 | 0.24 | 0.28 | 0.31 | ns, Max |
| $T_{CXCY}$ | CX input to COUT output | 0.15 | 0.17 | 0.20 | 0.22 | ns, Max |
| $T_{DXCY}$ | DX input to COUT output | 0.14 | 0.16 | 0.19 | 0.21 | ns, Max |
| $T_{BYP}$ | CIN input to COUT output | 0.06 | 0.07 | 0.08 | 0.09 | ns, Max |
| $T_{CINA}$ | CIN input to AMUX output | 0.21 | 0.24 | 0.28 | 0.30 | ns, Max |
| $T_{CINB}$ | CIN input to BMUX output | 0.23 | 0.25 | 0.29 | 0.31 | ns, Max |
| $T_{CINC}$ | CIN input to CMUX output | 0.23 | 0.26 | 0.30 | 0.33 | ns, Max |
| $T_{CIND}$ | CIN input to DMUX output | 0.25 | 0.29 | 0.33 | 0.36 | ns, Max |
| **Sequential Delays** | | | | | | |
| $T_{CKO}$ | Clock to AQ – DQ outputs | 0.29 | 0.33 | 0.39 | 0.44 | ns, Max |
| $T_{SHCKO}$ | Clock to AMUX – DMUX outputs | 0.36 | 0.40 | 0.47 | 0.53 | ns, Max |
| **Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK** | | | | | | |
| $T_{DICK}/T_{CKDI}$ | A – D input to CLK on A – D Flip Flops | 0.30/0.17 | 0.36/0.18 | 0.43/0.20 | 0.44/0.25 | ns, Min |
| $T_{CECK\_CLB}/T_{CKCE\_CLB}$ | CE input to CLK on A – D Flip Flops | 0.20/0.00 | 0.25/0.00 | 0.32/0.00 | 0.32/0.01 | ns, Min |
| $T_{SRCK}/T_{CKSR}$ | SR input to CLK on A – D Flip Flops | 0.39/–0.07 | 0.44/–0.07 | 0.52/–0.07 | 0.58/–0.08 | ns, Min |
| $T_{CINCK}/T_{CKCIN}$ | CIN input to CLK on A – D Flip Flops | 0.16/0.12 | 0.19/0.14 | 0.24/0.16 | 0.23/0.22 | ns, Min |
| **Set/Reset** | | | | | | |
| $T_{SRMIN}$ | SR input minimum pulse width | 0.90 | 0.90 | 0.97 | 0.80 | ns, Min |
| $T_{RQ}$ | Delay from SR input to AQ – DQ flip-flops | 0.52 | 0.58 | 0.68 | 0.77 | ns, Max |
| $T_{CEO}$ | Delay from CE input to AQ – DQ flip-flops | 0.41 | 0.48 | 0.59 | 0.61 | ns, Max |
| $F_{TOG}$ | Toggle frequency (for export control) | 1412.00 | 1286.40 | 1098.00 | 1098.00 | MHz |

**Notes:**

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
2. These items are of interest for Carry Chain applications.

## CLB Distributed RAM Switching Characteristics (SLICEM Only)

*Table 55:* **CLB Distributed RAM Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 | -1L | |
| **Sequential Delays** | | | | | | |
| $T_{SHCKO}$ | Clock to A – B outputs | 0.92 | 1.10 | 1.36 | 1.49 | ns, Max |
| $T_{SHCKO\_1}$ | Clock to AMUX – BMUX outputs | 1.19 | 1.40 | 1.71 | 1.87 | ns, Max |
| **Setup and Hold Times Before/After Clock CLK** | | | | | | |
| $T_{DS}/T_{DH}$ | A – D inputs to CLK | 0.62/0.18 | 0.72/0.20 | 0.88/0.22 | 0.98/0.23 | ns, Min |
| $T_{AS}/T_{AH}$ | Address An inputs to clock | 0.19/0.52 | 0.22/0.59 | 0.27/0.66 | 0.30/0.75 | ns, Min |
| $T_{WS}/T_{WH}$ | WE input to clock | 0.27/0.00 | 0.32/0.00 | 0.40/0.00 | 0.47/–0.03 | ns, Min |
| $T_{CECK}/T_{CKCE}$ | CE input to CLK | 0.28/–0.01 | 0.34/–0.01 | 0.41/–0.01 | 0.48/–0.05 | ns, Min |
| **Clock CLK** | | | | | | |
| $T_{MPW}$ | Minimum pulse width | 0.70 | 0.82 | 1.00 | 1.04 | ns, Min |
| $T_{MCP}$ | Minimum clock period | 1.40 | 1.64 | 2.00 | 2.08 | ns, Min |

**Notes:**

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. $T_{SHCKO}$ also represents the CLK to XMUX output. Refer to TRACE report for the CLK to XMUX path.

## CLB Shift Register Switching Characteristics (SLICEM Only)

*Table 56:* **CLB Shift Register Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 | -1L | |
| **Sequential Delays** | | | | | | |
| $T_{REG}$ | Clock to A – D outputs | 1.11 | 1.30 | 1.58 | 1.74 | ns, Max |
| $T_{REG\_MUX}$ | Clock to AMUX – DMUX output | 1.37 | 1.60 | 1.93 | 2.12 | ns, Max |
| $T_{REG\_M31}$ | Clock to DMUX output via M31 output | 1.08 | 1.27 | 1.55 | 1.74 | ns, Max |
| **Setup and Hold Times Before/After Clock CLK** | | | | | | |
| $T_{WS}/T_{WH}$ | WE input | 0.05/0.00 | 0.07/0.00 | 0.09/0.00 | 0.11/0.03 | ns, Min |
| $T_{CECK}/T_{CKCE}$ | CE input to CLK | 0.06/–0.01 | 0.08/–0.01 | 0.10/–0.01 | 0.12/0.02 | ns, Min |
| $T_{DS}/T_{DH}$ | A – D inputs to CLK | 0.64/0.18 | 0.76/0.21 | 0.94/0.24 | 1.07/0.23 | ns, Min |
| **Clock CLK** | | | | | | |
| $T_{MPW}$ | Minimum pulse width | 0.60 | 0.70 | 0.85 | 0.89 | ns, Min |

**Notes:**

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

## Block RAM and FIFO Switching Characteristics

*Table 57:* **Block RAM and FIFO Switching Characteristics**

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -3 | -2 | -1 | -1L | |
| **Block RAM and FIFO Clock-to-Out Delays** | | | | | | |
| $T_{RCKO\_DO}$ and $T_{RCKO\_DO\_REG}$[1] | Clock CLK to DOUT output (without output register)[2][3] | 1.60 | 1.79 | 2.08 | 2.36 | ns, Max |
| | Clock CLK to DOUT output (with output register)[4][5] | 0.60 | 0.66 | 0.75 | 0.83 | ns, Max |
| $T_{RCKO\_DO\_ECC}$ and $T_{RCKO\_DO\_ECC\_REG}$ | Clock CLK to DOUT output with ECC (without output register)[2][3] | 2.62 | 2.89 | 3.30 | 3.73 | ns, Max |
| | Clock CLK to DOUT output with ECC (with output register)[4][5] | 0.71 | 0.77 | 0.86 | 0.94 | ns, Max |
| $T_{RCKO\_CASC}$ and $T_{RCKO\_CASC\_REG}$ | Clock CLK to DOUT output with Cascade (without output register)[2] | 2.49 | 2.77 | 3.18 | 3.61 | ns, Max |
| | Clock CLK to DOUT output with Cascade (with output register)[4] | 1.29 | 1.41 | 1.58 | 1.79 | ns, Max |
| $T_{RCKO\_FLAGS}$ | Clock CLK to FIFO flags outputs[6] | 0.74 | 0.81 | 0.91 | 0.98 | ns, Max |
| $T_{RCKO\_POINTERS}$ | Clock CLK to FIFO pointers outputs[7] | 0.90 | 0.98 | 1.09 | 1.21 | ns, Max |
| $T_{RCKO\_SDBIT\_ECC}$ and $T_{RCKO\_SDBIT\_ECC\_REG}$ | Clock CLK to BITERR (with output register) | 0.62 | 0.68 | 0.76 | 0.82 | ns, Max |
| | Clock CLK to BITERR (without output register) | 2.21 | 2.46 | 2.84 | 3.23 | ns, Max |
| $T_{RCKO\_PARITY\_ECC}$ | Clock CLK to ECCPARITY in ECC encode only mode | 0.86 | 0.94 | 1.06 | 1.18 | ns, Max |
| $T_{RCKO\_RDADDR\_ECC}$ and $T_{RCKO\_RDADDR\_ECC\_REG}$ | Clock CLK to RDADDR output with ECC (without output register) | 0.73 | 0.79 | 0.90 | 1.00 | ns, Max |
| | Clock CLK to RDADDR output with ECC (with output register) | 0.76 | 0.82 | 0.92 | 1.02 | ns, Max |
| **Setup and Hold Times Before/After Clock CLK** | | | | | | |
| $T_{RCCK\_ADDR}/T_{RCKC\_ADDR}$ | ADDR inputs[8] | 0.47/ 0.27 | 0.53/ 0.29 | 0.62/ 0.32 | 0.66/ 0.34 | ns, Min |
| $T_{RDCK\_DI}/T_{RCKD\_DI}$ | DIN inputs[9] | 0.84/ 0.30 | 0.95/ 0.32 | 1.11/ 0.34 | 1.26/ 0.36 | ns, Min |
| $T_{RDCK\_DI\_ECC}/T_{RCKD\_DI\_ECC}$ | DIN inputs with block RAM ECC in standard mode[9] | 0.47/ 0.30 | 0.52/ 0.32 | 0.59/ 0.34 | 0.68/ 0.36 | ns, Min |
| | DIN inputs with block RAM ECC encode only[9] | 0.68/ 0.30 | 0.75/ 0.32 | 0.85/ 0.34 | 0.97/ 0.36 | ns, Min |
| | DIN inputs with FIFO ECC in standard mode[9] | 0.77/ 0.30 | 0.87/ 0.32 | 1.02/ 0.34 | 1.16/ 0.36 | ns, Min |
| $T_{RCCK\_CLK}/T_{RCKC\_CLK}$ | Inject single/double bit error in ECC mode | 0.90/ 0.27 | 1.02/ 0.28 | 1.20/ 0.29 | 1.56/ 0.29 | ns, Min |
| $T_{RCCK\_RDEN}/T_{RCKC\_RDEN}$ | Block RAM Enable (EN) input | 0.31/ 0.26 | 0.35/ 0.27 | 0.41/ 0.30 | 0.44/ 0.31 | ns, Min |
| $T_{RCCK\_REGCE}/T_{RCKC\_REGCE}$ | CE input of output register | 0.18/ 0.25 | 0.19/ 0.27 | 0.22/ 0.31 | 0.24/ 0.33 | ns, Min |
| $T_{RCCK\_RSTREG}/T_{RCKC\_RSTREG}$ | Synchronous RSTREG input | 0.22/ 0.23 | 0.24/ 0.24 | 0.28/ 0.26 | 0.31/ 0.27 | ns, Min |
| $T_{RCCK\_RSTRAM}/T_{RCKC\_RSTRAM}$ | Synchronous RSTRAM input | 0.32/ 0.23 | 0.36/ 0.24 | 0.41/ 0.27 | 0.46/ 0.29 | ns, Min |

## Virtex-6 Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 65. Values are expressed in nanoseconds unless otherwise noted.

*Table 65:* **Global Clock Input to Output Delay Without MMCM**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1 | -1L | |
| LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *without* MMCM. | | | | | | | |
| $T_{ICKOF}$ | Global Clock input and OUTFF *without* MMCM | XC6VLX75T | 4.91 | 5.32 | 5.88 | 6.02 | ns |
| | | XC6VLX130T | 4.89 | 5.33 | 6.00 | 6.13 | ns |
| | | XC6VLX195T | 5.02 | 5.46 | 6.13 | 6.27 | ns |
| | | XC6VLX240T | 5.02 | 5.46 | 6.13 | 6.27 | ns |
| | | XC6VLX365T | 5.30 | 5.75 | 6.43 | 6.37 | ns |
| | | XC6VLX550T | N/A | 6.02 | 6.72 | 6.60 | ns |
| | | XC6VLX760 | N/A | 6.26 | 6.97 | 6.87 | ns |
| | | XC6VSX315T | 5.40 | 5.85 | 6.54 | 6.49 | ns |
| | | XC6VSX475T | N/A | 6.01 | 6.71 | 6.61 | ns |
| | | XC6VHX250T | 5.18 | 5.63 | 6.30 | N/A | ns |
| | | XC6VHX255T | 5.20 | 5.66 | 6.34 | N/A | ns |
| | | XC6VHX380T | 5.38 | 5.84 | 6.53 | N/A | ns |
| | | XC6VHX565T | N/A | 6.03 | 6.71 | N/A | ns |
| | | XQ6VLX130T | N/A | 5.33 | 6.00 | 6.13 | ns |
| | | XQ6VLX240T | N/A | 5.46 | 6.13 | 6.27 | ns |
| | | XQ6VLX550T | N/A | N/A | 6.72 | 6.60 | ns |
| | | XQ6VSX315T | N/A | 5.85 | 6.54 | 6.49 | ns |
| | | XQ6VSX475T | N/A | N/A | 6.71 | 6.61 | ns |

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

*Table 67:* **Clock-Capable Clock Input to Output Delay With MMCM**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1 | -1L | |
| LVCMOS25 Clock-capable Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* MMCM. | | | | | | | |
| $T_{ICKOFMMCMCC}$ | Clock-capable Clock Input and OUTFF *with* MMCM | XC6VLX75T | 2.22 | 2.38 | 2.63 | 2.72 | ns |
| | | XC6VLX130T | 2.24 | 2.39 | 2.65 | 2.74 | ns |
| | | XC6VLX195T | 2.24 | 2.40 | 2.65 | 2.75 | ns |
| | | XC6VLX240T | 2.24 | 2.40 | 2.65 | 2.75 | ns |
| | | XC6VLX365T | 2.25 | 2.42 | 2.65 | 2.76 | ns |
| | | XC6VLX550T | N/A | 2.43 | 2.68 | 2.80 | ns |
| | | XC6VLX760 | N/A | 2.42 | 2.69 | 2.79 | ns |
| | | XC6VSX315T | 2.23 | 2.38 | 2.65 | 2.73 | ns |
| | | XC6VSX475T | N/A | 2.30 | 2.57 | 2.66 | ns |
| | | XC6VHX250T | 2.25 | 2.41 | 2.67 | N/A | ns |
| | | XC6VHX255T | 2.35 | 2.51 | 2.78 | N/A | ns |
| | | XC6VHX380T | 2.27 | 2.43 | 2.69 | N/A | ns |
| | | XC6VHX565T | N/A | 2.41 | 2.68 | N/A | ns |
| | | XQ6VLX130T | N/A | 2.39 | 2.65 | 2.74 | ns |
| | | XQ6VLX240T | N/A | 2.40 | 2.65 | 2.75 | ns |
| | | XQ6VLX550T | N/A | N/A | 2.68 | 2.80 | ns |
| | | XQ6VSX315T | N/A | 2.38 | 2.65 | 2.73 | ns |
| | | XQ6VSX475T | N/A | N/A | 2.57 | 2.66 | ns |

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

*Table 70:* **Clock-Capable Clock Input Setup and Hold With MMCM**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1 | -1L | |
| **Input Setup and Hold Time Relative to Clock-capable Clock Input Signal for LVCMOS25 Standard.(1)** | | | | | | | |
| $T_{PSMMCMCC}$/ $T_{PHMMCMCC}$ | No Delay Clock-capable Clock Input and IFF(2) with MMCM | XC6VLX75T | 1.56/ –0.25 | 1.69/ –0.25 | 1.86/ –0.25 | 1.91/ –0.15 | ns |
| | | XC6VLX130T | 1.64/ –0.25 | 1.78/ –0.25 | 1.95/ –0.25 | 2.00/ –0.14 | ns |
| | | XC6VLX195T | 1.65/ –0.24 | 1.79/ –0.24 | 1.96/ –0.24 | 2.01/ –0.15 | ns |
| | | XC6VLX240T | 1.65/ –0.24 | 1.79/ –0.24 | 1.96/ –0.24 | 2.01/ –0.15 | ns |
| | | XC6VLX365T | 1.66/ –0.25 | 1.79/ –0.25 | 1.97/ –0.25 | 2.02/ –0.15 | ns |
| | | XC6VLX550T | N/A | 1.97/ –0.24 | 2.16/ –0.24 | 2.19/ –0.14 | ns |
| | | XC6VLX760 | N/A | 2.39/ –0.20 | 2.63/ –0.20 | 2.21/ –0.10 | ns |
| | | XC6VSX315T | 1.67/ –0.25 | 1.80/ –0.25 | 1.98/ –0.25 | 2.03/ –0.16 | ns |
| | | XC6VSX475T | N/A | 1.98/ –0.29 | 2.17/ –0.29 | 2.21/ –0.20 | ns |
| | | XC6VHX250T | 1.63/ –0.24 | 1.76/ –0.24 | 1.94/ –0.24 | N/A | ns |
| | | XC6VHX255T | 1.63/ –0.19 | 1.76/ –0.19 | 1.99/ –0.19 | N/A | ns |
| | | XC6VHX380T | 1.80/ –0.23 | 1.94/ –0.23 | 2.13/ –0.23 | N/A | ns |
| | | XC6VHX565T | N/A | 1.94/ –0.08 | 2.13/ –0.08 | N/A | ns |
| | | XQ6VLX130T | N/A | 1.78/ –0.25 | 1.95/ –0.25 | 2.00/ –0.14 | ns |
| | | XQ6VLX240T | N/A | 1.79/ –0.24 | 1.96/ –0.24 | 2.01/ –0.15 | ns |
| | | XQ6VLX550T | N/A | N/A | 2.16/ –0.24 | 2.19/ –0.14 | ns |
| | | XQ6VSX315T | N/A | 1.80/ –0.25 | 1.98/ –0.25 | 2.03/ –0.16 | ns |
| | | XQ6VSX475T | N/A | N/A | 2.17/ –0.29 | 2.21/ –0.20 | ns |

**Notes:**

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

## Clock Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-6 FPGA clock transmitter and receiver data-valid windows.

*Table 71:* **Duty Cycle Distortion and Clock-Tree Skew**

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1 | -1L | |
| $T_{DCD\_CLK}$ | Global Clock Tree Duty Cycle Distortion(1) | All | 0.12 | 0.12 | 0.12 | 0.12 | ns |
| $T_{CKSKEW}$ | Global Clock Tree Skew(2) | XC6VLX75T | 0.15 | 0.16 | 0.18 | 0.17 | ns |
| | | XC6VLX130T | 0.25 | 0.26 | 0.29 | 0.28 | ns |
| | | XC6VLX195T | 0.26 | 0.27 | 0.31 | 0.30 | ns |
| | | XC6VLX240T | 0.26 | 0.27 | 0.31 | 0.30 | ns |
| | | XC6VLX365T | 0.28 | 0.29 | 0.31 | 0.31 | ns |
| | | XC6VLX550T | N/A | 0.50 | 0.54 | 0.54 | ns |
| | | XC6VLX760 | N/A | 0.51 | 0.56 | 0.56 | ns |
| | | XC6VSX315T | 0.27 | 0.28 | 0.32 | 0.30 | ns |
| | | XC6VSX475T | N/A | 0.39 | 0.44 | 0.42 | ns |
| | | XC6VHX250T | 0.25 | 0.26 | 0.29 | N/A | ns |
| | | XC6VHX255T | 0.35 | 0.37 | 0.41 | N/A | ns |
| | | XC6VHX380T | 0.45 | 0.47 | 0.52 | N/A | ns |
| | | XC6VHX565T | N/A | 0.46 | 0.51 | N/A | ns |
| | | XQ6VLX130T | N/A | 0.26 | 0.29 | 0.28 | ns |
| | | XQ6VLX240T | N/A | 0.27 | 0.31 | 0.30 | ns |
| | | XQ6VLX550T | N/A | N/A | 0.54 | 0.54 | ns |
| | | XQ6VSX315T | N/A | 0.28 | 0.32 | 0.30 | ns |
| | | XQ6VSX475T | N/A | N/A | 0.44 | 0.42 | ns |
| $T_{DCD\_BUFIO}$ | I/O clock tree duty cycle distortion | All | 0.08 | 0.08 | 0.08 | 0.08 | ns |
| $T_{BUFIOSKEW}$ | I/O clock tree skew across one clock region | All | 0.03 | 0.03 | 0.03 | 0.02 | ns |
| $T_{BUFIOSKEW2}$ | I/O clock tree skew across three clock regions | All | 0.10 | 0.12 | 0.23 | 0.12 | ns |
| $T_{DCD\_BUFR}$ | Regional clock tree duty cycle distortion | All | 0.15 | 0.15 | 0.15 | 0.15 | ns |

**Notes:**

1. These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
2. The $T_{CKSKEW}$ value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.