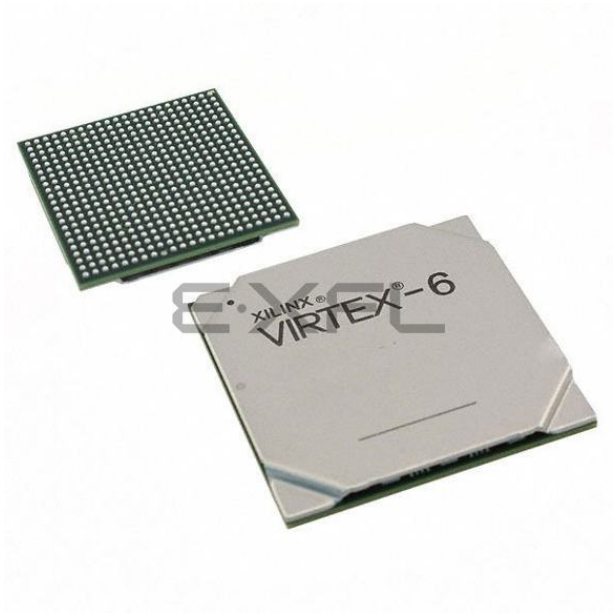
AMD Xilinx - XC6VSX475T-L1FF1759I Datasheet



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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	37200
Number of Logic Elements/Cells	476160
Total RAM Bits	39223296
Number of I/O	840
Number of Gates	-
Voltage - Supply	0.91V ~ 0.97V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1759-BBGA, FCBGA
Supplier Device Package	1759-FCBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc6vsx475t-l1ff1759i

Table 4: **Typical Quiescent Supply Current *(Cont'd)***

Symbol	Description	Device	Speed and Temperature Grade						Units
			-3 (C)	-2 (C, E, & I)	-1 (C & I)	-1 (I & M)(2)	-1L (C)	-1L (I)(1)	
I_{CCOQ}	Quiescent V_{CCO} supply current	XC6VLX75T	1	1	1	N/A	1	1	mA
		XC6VLX130T	1	1	1	N/A	1	1	mA
		XC6VLX195T	1	1	1	N/A	1	1	mA
		XC6VLX240T	2	2	2	N/A	2	2	mA
		XC6VLX365T	2	2	2	N/A	2	2	mA
		XC6VLX550T(3)	N/A	3	3	N/A	3	3	mA
		XC6VLX760(3)	N/A	3	3	N/A	3	3	mA
		XC6VSX315T	2	2	2	N/A	2	2	mA
		XC6VSX475T(3)	N/A	2	2	N/A	2	2	mA
		XC6VHX250T	1	1	1	N/A	N/A	N/A	mA
		XC6VHX255T	1	1	1	N/A	N/A	N/A	mA
		XC6VHX380T(4)	2	2	2	N/A	N/A	N/A	mA
		XC6VHX565T(5)	N/A	2	2	N/A	N/A	N/A	mA
		XQ6VLX130T	N/A	1	N/A	1	N/A	1	mA
		XQ6VLX240T	N/A	2	N/A	2	N/A	2	mA
		XQ6VLX550T(7)	N/A	N/A	N/A	3	N/A	3	mA
		XQ6VSX315T	N/A	2	N/A	2	N/A	2	mA
		XQ6VSX475T(7)	N/A	N/A	N/A	2	N/A	2	mA

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on sequence and ramp rate of the power supply.

The recommended power-on sequence for Virtex-6 devices is V_{CCINT}, V_{CCAUX}, and V_{CCO} to meet the power-up current requirements listed in Table 5. V_{CCINT} can be powered up or down at any time, but power up current specifications can vary from Table 5. The device will have no physical damage or reliability concerns if V_{CCINT}, V_{CCAUX}, and V_{CCO} sequence cannot be followed.

If the recommended power-up sequence cannot be followed and the I/Os must remain 3-stated throughout configuration, then V_{CCAUX} must be powered prior to V_{CCO} or V_{CCAUX} and V_{CCO} must be powered by the same supply. Similarly, for power-down, the reverse V_{CCAUX} and V_{CCO} sequence is recommended if the I/Os are to remain 3-stated.

The GTH transceiver supplies must be powered using a MGTHAVCC, MGTHAVCCRX, MGTHAVCCPLL, and MGTHAVTT sequence. There are no sequencing requirement for these supplies with respect to the other FPGA supply voltages. For more detail see Table 27: *GTH Transceiver Power Supply Sequencing*. There are no sequencing requirements for the GTX transceivers power supplies.

Table 5 shows the minimum current, in addition to I_{CCQ}, that are required by Virtex-6 devices for proper power-on and configuration. If the current minimums shown in Table 4 and Table 5 are met, the device powers on after all three supplies have passed through their power-on reset threshold voltages. The FPGA must be configured after applying V_{CCINT}, V_{CCAUX}, and V_{CCO} for the appropriate configuration banks. Once initialized and configured, use the XPE tools to estimate current drain on these supplies.

Table 5: **Power-On Current for Virtex-6 Devices**

Device	$I_{CCINTMIN}$	$I_{CCAUXMIN}$	I_{CCOMIN}	Units
	Typ(1)	Typ(1)	Typ(1)	
XC6VLX75T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 10	I_{CCOQ} + 30 mA per bank	mA
XC6VLX130T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 10	I_{CCOQ} + 30 mA per bank	mA
XC6VLX195T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA
XC6VLX240T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA
XC6VLX365T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA
XC6VLX550T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA
XC6VLX760	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA
XC6VSX315T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA
XC6VSX475T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 50	I_{CCOQ} + 30 mA per bank	mA
XC6VHX250T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA
XC6VHX255T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA
XC6VHX380T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA
XC6VHX565T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 40	I_{CCOQ} + 30 mA per bank	mA
XQ6VLX130T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 100	I_{CCOQ} + 30 mA per bank	mA
XQ6VLX240T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 100	I_{CCOQ} + 30 mA per bank	mA
XQ6VLX550T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 100	I_{CCOQ} + 30 mA per bank	mA
XQ6VSX315T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 100	I_{CCOQ} + 40 mA per bank	mA
XQ6VSX475T	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 100	I_{CCOQ} + 40 mA per bank	mA

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. Use the XPower Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate maximum power-on currents.

HT DC Specifications (HT_25)

Table 8: **HT DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OD}	Differential Output Voltage for XC devices	R_T = 100 Ω across Q and $\overline{Q}$ signals	480	600	885	mV
	Differential Output Voltage for XQ devices		480	600	930	mV
ΔV_{OD}	Change in V_{OD} Magnitude		–15	–	15	mV
V_{OCM}	Output Common Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	440	600	760	mV
ΔV_{OCM}	Change in V_{OCM} Magnitude		–15	–	15	mV
V_{ID}	Input Differential Voltage		200	600	1000	mV
ΔV_{ID}	Change in V_{ID} Magnitude		–15	–	15	mV
V_{ICM}	Input Common Mode Voltage		440	600	780	mV
ΔV_{ICM}	Change in V_{ICM} Magnitude		–15	–	15	mV

LVDS DC Specifications (LVDS_25)

Table 9: **LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.825	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High (Q – $\overline{Q}$), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output Common-Mode Voltage for XC devices	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.075	1.250	1.425	V
	Output Common-Mode Voltage for XQ devices		1.000	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High (Q – $\overline{Q}$), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input Common-Mode Voltage		0.3	1.2	2.2	V

Extended LVDS DC Specifications (LVDSEXT_25)

Table 10: **Extended LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	–	–	1.785	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.715	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High (Q – $\overline{Q}$), $\overline{Q}$ = High for XC devices	R_T = 100 Ω across Q and $\overline{Q}$ signals	350	–	840	mV
	Differential Output Voltage (Q – $\overline{Q}$), Q = High (Q – $\overline{Q}$), $\overline{Q}$ = High for XQ devices		350	–	850	mV
V_{OCM}	Output Common-Mode Voltage for XC devices	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.075	1.250	1.425	V
	Output Common-Mode Voltage for XQ devices		1.000	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High (Q – $\overline{Q}$), $\overline{Q}$ = High	Common-mode input voltage = 1.25V	100	–	1000	mV
V_{ICM}	Input Common-Mode Voltage	Differential input voltage = ±350 mV	0.3	1.2	2.2	V

Table 16: **GTX Transceiver Quiescent Supply Current (per Lane) (1)(2)(3)**

Symbol	Description	Typ(4)	Max	Units
$I_{MGTAVTTQ}$	Quiescent MGTAVTT supply current for one GTX transceiver	0.9	Note 2	mA
$I_{MGTAVCCQ}$	Quiescent MGTAVCC supply current for one GTX transceiver	3.5		mA

Notes:

1. Device powered and unconfigured.
2. Currents for conditions other than values specified in this table can be obtained by using the XPE or XPA tools.
3. GTX transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTX transceivers.
4. Typical values are specified at nominal voltage, 25°C.

GTX Transceiver DC Input and Output Levels

Table 17 summarizes the DC output specifications of the GTX transceivers in Virtex-6 FPGAs. Consult UG366: *Virtex-6 FPGA GTX Transceivers User Guide* for further details.

Table 17: **GTX Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage	External AC coupled ≤ 4.25 Gb/s	125	–	2000	mV
		External AC coupled > 4.25 Gb/s	175	–	2000	mV
V_{IN}	Absolute input voltage	DC coupled MGTAVTT = 1.2V	–400	–	MGTAVTT	mV
V_{CMIN}	Common mode input voltage	DC coupled MGTAVTT = 1.2V	–	2/3 MGTAVTT	–	mV
DV_{PPOUT}	Differential peak-to-peak output voltage(1)	Transmitter output swing is set to maximum setting	–	–	1000	mV
$V_{CMOUTDC}$	DC common mode output voltage.	Equation based	MGTAVTT – DV_{PPOUT}/4			mV
R_{IN}	Differential input resistance		80	100	130	Ω
R_{OUT}	Differential output resistance		80	100	120	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	2	8	ps
C_{EXT}	Recommended external AC coupling capacitor(2)		–	100	–	nF

Notes:

1. The output swing and preemphasis levels are programmable using the attributes discussed in UG366: *Virtex-6 FPGA GTX Transceivers User Guide* and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

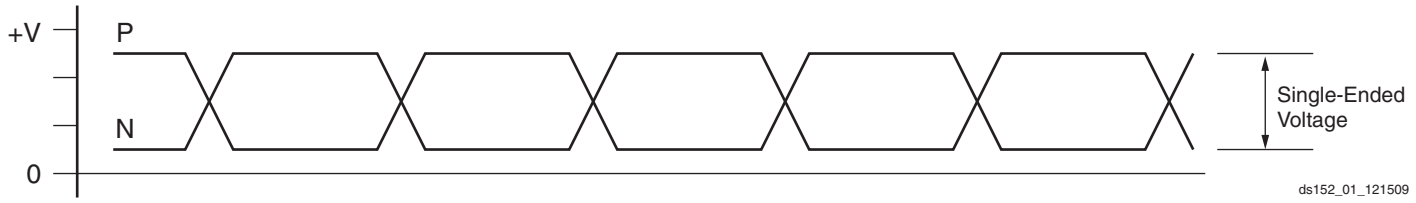

Figure 1: **Single-Ended Peak-to-Peak Voltage**

GTH Transceiver Specifications

GTH Transceiver DC Characteristics

Table 25: **Absolute Maximum Ratings for GTH Transceivers(1)**

Symbol	Description	Min	Max	Units
MGTHAVCC	Analog supply voltage for the GTH transmitter, receiver, and common analog circuits	–0.5	1.125	V
MGTHAVCCRX	Analog supply voltage for the GTH receiver circuits and common analog circuits	–0.5	1.125	V
MGTHAVTT	Analog supply voltage for the GTH transmitter termination circuits	–0.5	1.32	V
MGTHAVCCPLL	Analog supply voltage for the GTH receiver and PLL circuits	–0.5	1.935	V
V_{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	–0.5	1.125	V
$V_{MGTREFCLK}$	Reference clock absolute input voltage	–0.5	1.935	V

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 26: **Recommended Operating Conditions for GTH Transceivers (1)(2)**

Symbol	Description	Min	Typ	Max	Units
MGTHAVCC	Analog supply voltage for the GTH transmitter, receiver, and common analog circuits	1.075	1.1	1.125	V
MGTHAVCCRX	Analog supply voltage for the GTH receiver circuits and common analog circuits	1.075	1.1	1.125	V
MGTHAVTT	Analog supply voltage for the GTH transmitter termination circuits	1.140	1.2	1.26	V
MGTHAVCCPLL	Analog supply voltage for the GTH receiver and PLL circuit	1.710	1.8	1.89	V

Notes:

1. Each voltage listed requires the filter circuit described in UG371: *Virtex-6 FPGA GTH Transceivers User Guide*.
2. Voltages are specified for the temperature range of T_j = –40°C to +100°C.

Table 27: **GTH Transceiver Power Supply Sequencing (1)(2)(3)**

Symbol	Description	Min	Max	Units
$T_{HAVCC2HAVCCRX}$	Maximum time between powering MGTHAVCC to when MGTHAVCCRX must be powered.	0	5	ms
$T_{HAVCCRX2HAVCCPLL}$	Minimum time between powering MGTHAVCCRX to when MGTHAVCCPLL can be powered.	10	–	µs
$T_{HAVCCRX2HAVTT}$	Minimum time between powering MGTHAVCCRX to when MGTHAVTT can be powered.	10	–	µs

Notes:

1. MGTHAVCCRX must be powered simultaneously or within $T_{HAVCC2HAVCCRX}$ of MGTHAVCC, but it must not precede MGTHAVCC.
2. MGTHAVCC and MGTHAVCCRX must be powered before MGTHAVCCPLL and MGTHAVTT. This minimum time is defined by $T_{HAVCCRX2HAVCCPLL}$ and $T_{HAVCCRX2HAVTT}$.
3. At any time, the condition of MGTHAVCC being present and MGTHAVCCRX not being present should not occur for more than the maximum $T_{HAVCC2HAVCCRX}$.

Table 37: **GTH Transceiver Receiver Switching Characteristics**

Symbol	Description		Min	Typ	Max	Units
R_{XRL}	Run length (CID)		8000	–	–	UI
$R_{XPPMTOL}$	Data/REFCLK PPM offset tolerance		–200	–	200	ppm
SJ Jitter Tolerance(1)(2)(3)(4)						
$JT\_SJ_{11.18}$	Sinusoidal Jitter	11.18 Gb/s	0.3	–	–	UI
$JT\_SJ_{10.32}$	Sinusoidal Jitter	10.32 Gb/s	0.3	–	–	UI
$JT\_SJ_{9.95}$	Sinusoidal Jitter	9.95 Gb/s	0.3	–	–	UI
$JT\_SJ_{2.667}$	Sinusoidal Jitter	2.667 Gb/s	0.5	–	–	UI
$JT\_SJ_{2.48}$	Sinusoidal Jitter	2.48 Gb/s	0.5	–	–	UI

Notes:

1. These values are NOT intended for protocol specific compliance determinations.
2. All jitter values are based on a bit error ratio of $1e^{-12}$.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. High-frequency jitter tolerance including 6 db of channel loss at a high frequency of the data rate divided by two.

Ethernet MAC Switching Characteristics

Consult UG368: *Virtex-6 FPGA Embedded Tri-mode Ethernet MAC User Guide* for further information.

Table 38: **Maximum Ethernet MAC Performance**

Symbol	Description	Conditions	Speed Grade				Units
			-3	-2	-1	-1L	
$F_{TEMACCLIENT}$	Client interface maximum frequency	10 Mb/s – 8-bit width	2.5(1)	2.5(1)	2.5(1)	2.5(1)	MHz
		100 Mb/s – 8-bit width	25(2)	25(2)	25(2)	25(2)	MHz
		1000 Mb/s – 8-bit width	125	125	125	125	MHz
		1000 Mb/s – 16-bit width	62.5	62.5	62.5	62.5	MHz
		2000 Mb/s – 16-bit width	125	125	125	N/A	MHz
		2500 Mb/s – 16-bit width	156.25	156.25	156.25	N/A	MHz
$F_{TEMACPHY}$	Physical interface maximum frequency	10 Mb/s – 4-bit width	2.5	2.5	2.5	2.5	MHz
		100 Mb/s – 4-bit width	25	25	25	25	MHz
		1000 Mb/s – 8-bit width	125	125	125	125	MHz
		2000 Mb/s – 8-bit width	250	250	250	N/A	MHz
		2500 Mb/s – 8-bit width	312.5	312.5	312.5	N/A	MHz

Notes:

1. When not using clock enable, the F_{MAX} is lowered to 1.25 MHz.
2. When not using clock enable, the F_{MAX} is lowered to 12.5 MHz.

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex-6 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the Switching Characteristics, page 26.

Table 41: **Interface Performances**

Description	Speed Grade			
	-3	-2	-1	-1L
Networking Applications				
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	710 Mb/s	710 Mb/s	650 Mb/s	585 Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 10)	1.4 Gb/s	1.3 Gb/s	1.25 Gb/s	1.1 Gb/s
SDR LVDS receiver (SFI-4.1)(1)	710 Mb/s	710 Mb/s	650 Mb/s	585 Mb/s
DDR LVDS receiver (SPI-4.2)(1)	1.4 Gb/s	1.3 Gb/s	1.1 Gb/s	0.9 Gb/s
Maximum Physical Interface (PHY) Rate for Memory Interfaces(2)(3)(4)				
DDR2	800 Mb/s	800 Mb/s	800 Mb/s	606 Mb/s
DDR3	1066 Mb/s	1066 Mb/s	800 Mb/s	800 Mb/s
QDR II + SRAM	400 MHz	350 MHz	300 MHz	–
RLDRAM II	500 MHz	400 MHz	350 MHz	–

Notes:

1. LVDS receivers are typically bounded with certain applications where specific DPA algorithms dominate deterministic performance.
2. Verified on Xilinx memory characterization platforms designed according to the guidelines in UG: *Virtex-6 FPGA Memory Interface Solutions User Guide*.
3. Consult DS186: *Virtex-6 FPGA Memory Interface Solutions Data Sheet* for performance and feature information on memory interface cores (controller plus PHY).
4. Memory Interface data rates have not been tested over the junction temperature operating range for military (M) temperature devices. Customers are responsible for specifying and testing their specific M temperature grade memory implementation.

Table 44: **IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
LVCMOS25, Fast, 24 mA	0.51	0.57	0.66	0.70	1.66	1.79	1.99	1.96	1.66	1.79	1.99	1.96	ns
LVCMOS18, Slow, 2 mA	0.55	0.61	0.71	0.73	4.21	4.47	4.87	4.30	4.21	4.47	4.87	4.30	ns
LVCMOS18, Slow, 4 mA	0.55	0.61	0.71	0.73	2.79	2.96	3.21	2.94	2.79	2.96	3.21	2.94	ns
LVCMOS18, Slow, 6 mA	0.55	0.61	0.71	0.73	2.30	2.43	2.64	2.47	2.30	2.43	2.64	2.47	ns
LVCMOS18, Slow, 8 mA	0.55	0.61	0.71	0.73	2.01	2.11	2.27	2.24	2.01	2.11	2.27	2.24	ns
LVCMOS18, Slow, 12 mA	0.55	0.61	0.71	0.73	1.88	1.99	2.15	2.10	1.88	1.99	2.15	2.10	ns
LVCMOS18, Slow, 16 mA	0.55	0.61	0.71	0.73	1.84	1.95	2.11	2.04	1.84	1.95	2.11	2.04	ns
LVCMOS18, Fast, 2 mA	0.55	0.61	0.71	0.73	4.00	4.23	4.57	4.08	4.00	4.23	4.57	4.08	ns
LVCMOS18, Fast, 4 mA	0.55	0.61	0.71	0.73	2.62	2.76	2.97	2.74	2.62	2.76	2.97	2.74	ns
LVCMOS18, Fast, 6 mA	0.55	0.61	0.71	0.73	2.15	2.28	2.46	2.32	2.15	2.28	2.46	2.32	ns
LVCMOS18, Fast, 8 mA	0.55	0.61	0.71	0.73	1.90	1.99	2.13	2.14	1.90	1.99	2.13	2.14	ns
LVCMOS18, Fast, 12 mA	0.55	0.61	0.71	0.73	1.69	1.80	1.97	1.88	1.69	1.80	1.97	1.88	ns
LVCMOS18, Fast, 16 mA	0.55	0.61	0.71	0.73	1.63	1.74	1.91	1.88	1.63	1.74	1.91	1.88	ns
LVCMOS15, Slow, 2 mA	0.64	0.73	0.85	0.85	3.43	3.77	4.29	3.91	3.43	3.77	4.29	3.91	ns
LVCMOS15, Slow, 4 mA	0.64	0.73	0.85	0.85	2.58	2.79	3.10	2.93	2.58	2.79	3.10	2.93	ns
LVCMOS15, Slow, 6 mA	0.64	0.73	0.85	0.85	2.08	2.32	2.68	2.50	2.08	2.32	2.68	2.50	ns
LVCMOS15, Slow, 8 mA	0.64	0.73	0.85	0.85	1.81	1.98	2.23	2.24	1.81	1.98	2.23	2.24	ns
LVCMOS15, Slow, 12 mA	0.64	0.73	0.85	0.85	1.76	1.91	2.13	2.07	1.76	1.91	2.13	2.07	ns
LVCMOS15, Slow, 16 mA	0.64	0.73	0.85	0.85	1.69	1.83	2.04	1.98	1.69	1.83	2.04	1.98	ns
LVCMOS15, Fast, 2 mA	0.64	0.73	0.85	0.85	3.44	3.77	4.28	3.91	3.44	3.77	4.28	3.91	ns
LVCMOS15, Fast, 4 mA	0.64	0.73	0.85	0.85	2.37	2.53	2.78	2.66	2.37	2.53	2.78	2.66	ns
LVCMOS15, Fast, 6 mA	0.64	0.73	0.85	0.85	1.80	2.05	2.42	2.16	1.80	2.05	2.42	2.16	ns
LVCMOS15, Fast, 8 mA	0.64	0.73	0.85	0.85	1.76	1.90	2.11	2.04	1.76	1.90	2.11	2.04	ns
LVCMOS15, Fast, 12 mA	0.64	0.73	0.85	0.85	1.64	1.77	1.97	1.90	1.64	1.77	1.97	1.90	ns
LVCMOS15, Fast, 16 mA	0.64	0.73	0.85	0.85	1.62	1.76	1.96	1.92	1.62	1.76	1.96	1.92	ns
LVCMOS12, Slow, 2 mA	0.72	0.81	0.93	0.95	3.14	3.39	3.75	3.54	3.14	3.39	3.75	3.54	ns
LVCMOS12, Slow, 4 mA	0.72	0.81	0.93	0.95	2.43	2.63	2.93	2.79	2.43	2.63	2.93	2.79	ns
LVCMOS12, Slow, 6 mA	0.72	0.81	0.93	0.95	1.92	2.11	2.41	2.26	1.92	2.11	2.41	2.26	ns
LVCMOS12, Slow, 8 mA	0.72	0.81	0.93	0.95	1.87	2.02	2.25	2.17	1.87	2.02	2.25	2.17	ns
LVCMOS12, Fast, 2 mA	0.72	0.81	0.93	0.95	2.71	2.98	3.39	3.11	2.71	2.98	3.39	3.11	ns
LVCMOS12, Fast, 4 mA	0.72	0.81	0.93	0.95	1.93	2.16	2.51	2.31	1.93	2.16	2.51	2.31	ns
LVCMOS12, Fast, 6 mA	0.72	0.81	0.93	0.95	1.75	1.89	2.11	2.05	1.75	1.89	2.11	2.05	ns
LVCMOS12, Fast, 8 mA	0.72	0.81	0.93	0.95	1.69	1.82	2.02	1.98	1.69	1.82	2.02	1.98	ns
LVDCI_25	0.51	0.57	0.66	0.70	2.05	2.14	2.26	2.26	2.05	2.14	2.26	2.26	ns
LVDCI_18	0.55	0.61	0.71	0.73	2.07	2.23	2.47	2.38	2.07	2.23	2.47	2.38	ns
LVDCI_15	0.64	0.73	0.85	0.85	1.85	2.01	2.24	2.18	1.85	2.01	2.24	2.18	ns

Table 44: **IOB Switching Characteristics for the Commercial (XC) Virtex-6 Devices *(Cont'd)***

I/O Standard	T_{IOPI}				T_{IOOP}				T_{IOTP}				Units
	Speed Grade				Speed Grade				Speed Grade				
	-3	-2	-1	-1L	-3	-2	-1	-1L	-3	-2	-1	-1L	
DIFF_SSTL18_I	0.85	0.94	1.09	1.08	1.47	1.58	1.75	1.73	1.47	1.58	1.75	1.73	ns
DIFF_SSTL18_I_DCI	0.85	0.94	1.09	1.08	1.40	1.51	1.67	1.65	1.40	1.51	1.67	1.65	ns
DIFF_SSTL18_II	0.85	0.94	1.09	1.08	1.39	1.50	1.67	1.66	1.39	1.50	1.67	1.66	ns
DIFF_SSTL18_II_DCI	0.85	0.94	1.09	1.08	1.36	1.47	1.63	1.62	1.36	1.47	1.63	1.62	ns
DIFF_SSTL18_II_T_DCI	0.85	0.94	1.09	1.08	1.40	1.51	1.67	1.65	1.40	1.51	1.67	1.65	ns
DIFF_SSTL15	0.81	0.91	1.06	1.06	1.42	1.54	1.71	1.69	1.42	1.54	1.71	1.69	ns
DIFF_SSTL15_DCI	0.81	0.91	1.06	1.06	1.41	1.52	1.68	1.66	1.41	1.52	1.68	1.66	ns
DIFF_SSTL15_T_DCI	0.81	0.91	1.06	1.06	1.41	1.52	1.68	1.66	1.41	1.52	1.68	1.66	ns

Table 45: **IOB Switching Characteristics for the Defense-grade (XQ) Virtex-6 Devices**

I/O Standard	T_{IOPI}			T_{IOOP}			T_{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
LVDS_25	0.94	1.09	1.08	1.54	2.16	1.62	1.54	2.16	1.62	ns
LVDSEXT_25	0.94	1.09	1.08	1.65	2.20	1.73	1.65	2.20	1.73	ns
HT_25	0.94	1.09	1.08	1.62	2.20	1.69	1.62	2.20	1.69	ns
BLVDS_25	0.94	1.09	1.08	1.50	3.18	1.65	1.50	3.18	1.65	ns
RSDS_25 (point to point)	0.94	1.09	1.08	1.54	2.22	1.62	1.54	2.22	1.62	ns
HSTL_I	0.91	1.06	1.06	1.56	2.44	1.71	1.56	2.44	1.71	ns
HSTL_II	0.91	1.06	1.06	1.56	2.21	1.72	1.56	2.21	1.72	ns
HSTL_III	0.91	1.06	1.06	1.54	2.50	1.69	1.54	2.50	1.69	ns
HSTL_I_18	0.91	1.06	1.06	1.58	2.43	1.72	1.58	2.43	1.72	ns
HSTL_II_18	0.91	1.06	1.06	1.62	2.30	1.78	1.62	2.30	1.78	ns
HSTL_III_18	0.91	1.06	1.06	1.54	2.49	1.69	1.54	2.49	1.69	ns
SSTL2_I	0.91	1.06	1.06	1.60	2.50	1.74	1.60	2.50	1.74	ns
SSTL2_II	0.91	1.06	1.06	1.54	2.49	1.71	1.54	2.49	1.71	ns
SSTL15	0.91	1.06	1.06	1.54	2.07	1.69	1.54	2.07	1.69	ns
LVCMOS25, Slow, 2 mA	0.57	0.66	0.70	5.46	6.01	5.63	5.46	6.01	5.63	ns
LVCMOS25, Slow, 4 mA	0.57	0.66	0.70	3.49	3.79	3.65	3.49	3.79	3.65	ns
LVCMOS25, Slow, 6 mA	0.57	0.66	0.70	2.81	3.08	2.95	2.81	3.08	2.95	ns
LVCMOS25, Slow, 8 mA	0.57	0.66	0.70	2.41	2.72	2.59	2.41	2.72	2.59	ns
LVCMOS25, Slow, 12 mA	0.57	0.66	0.70	1.95	2.23	2.10	1.95	2.23	2.10	ns
LVCMOS25, Slow, 16 mA	0.57	0.66	0.70	2.05	2.29	2.21	2.05	2.29	2.21	ns
LVCMOS25, Slow, 24 mA	0.57	0.66	0.70	1.82	2.24	1.98	1.82	2.24	1.98	ns
LVCMOS25, Fast, 2 mA	0.57	0.66	0.70	5.49	6.04	5.62	5.49	6.04	5.62	ns
LVCMOS25, Fast, 4 mA	0.57	0.66	0.70	3.50	3.82	3.65	3.50	3.82	3.65	ns
LVCMOS25, Fast, 6 mA	0.57	0.66	0.70	2.73	2.99	2.88	2.73	2.99	2.88	ns
LVCMOS25, Fast, 8 mA	0.57	0.66	0.70	2.33	2.65	2.53	2.33	2.65	2.53	ns
LVCMOS25, Fast, 12 mA	0.57	0.66	0.70	1.88	2.08	2.03	1.88	2.08	2.03	ns

Table 48: **Output Delay Measurement Methodology *(Cont'd)***

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
HT (HyperTransport), 2.5V	LDT_25	100	0	0[2]	0.6
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V	LVPECL_25	100	0	0[2]	0
LVDCI/HSLVDCI, 2.5V	LVDCI_25, HSLVDCI_25	1M	0	1.25	0
LVDCI/HSLVDCI, 1.8V	LVDCI_18, HSLVDCI_18	1M	0	0.9	0
LVDCI/HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	1M	0	0.75	0
HSTL (High-Speed Transceiver Logic), Class I & II, with DCI	HSTL_I_DCI, HSTL_II_DCI	50	0	V_{REF}	0.75
HSTL, Class III, with DCI	HSTL_III_DCI	50	0	0.9	1.5
HSTL, Class I & II, 1.8V, with DCI	HSTL_I_DCI_18, HSTL_II_DCI_18	50	0	V_{REF}	0.9
HSTL, Class III, 1.8V, with DCI	HSTL_III_DCI_18	50	0	1.1	1.8
SSTL (Stub Series Termi.Logic), Class I & II, 1.8V, with DCI	SSTL18_I_DCI, SSTL18_II_DCI	50	0	V_{REF}	0.9
SSTL, Class I & II, 2.5V, with DCI	SSTL2_I_DCI, SSTL2_II_DCI	50	0	V_{REF}	1.25

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Input/Output Logic Switching Characteristics

Table 49: **ILOGIC Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
Setup/Hold						
T_{ICE1CK}/T_{ICKCE1}	CE1 pin Setup/Hold with respect to CLK	0.21/ 0.03	0.25/ 0.04	0.27/ 0.04	0.31/ 0.05	ns
T_{ISRCK}/T_{ICKSR}	SR pin Setup/Hold with respect to CLK	0.66/ –0.08	0.78/ –0.08	0.96/ –0.08	1.09/ –0.11	ns
T_{IDOCK}/T_{IOCKD}	D pin Setup/Hold with respect to CLK without Delay	0.07/ 0.41	0.08/ 0.46	0.10/ 0.54	0.11/ 0.64	ns
T_{IDOCKD}/T_{IOCKDD}	DDLY pin Setup/Hold with respect to CLK (using IODELAY)	0.10/ 0.32	0.12/ 0.36	0.14/ 0.42	0.16/ 0.50	ns
Combinatorial						
T_{IDI}	D pin to O pin propagation delay, no Delay	0.15	0.17	0.20	0.23	ns
T_{IDID}	DDLY pin to O pin propagation delay (using IODELAY)	0.19	0.22	0.25	0.28	ns
Sequential Delays						
T_{IDLO}	D pin to Q1 pin using flip-flop as a latch without Delay	0.48	0.54	0.64	0.73	ns
T_{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IODELAY)	0.52	0.58	0.68	0.78	ns
T_{ICKQ}	CLK to Q outputs	0.54	0.61	0.70	0.93	ns
T_{RQ_ILOGIC}	SR pin to OQ/TQ out	0.85	0.97	1.15	1.32	ns
T_{GSRQ_ILOGIC}	Global Set/Reset to Q outputs	7.60	7.60	10.51	10.51	ns
Set/Reset						
T_{RPW_ILOGIC}	Minimum Pulse Width, SR inputs	0.78	0.95	1.20	1.30	ns, Min

Table 50: **OLOGIC Switching Characteristics**

Symbol	Description	Speed Grade					Units
		-3	-2	-1 (XC)	-1 (XQ)	-1L	
Setup/Hold							
T_{ODCK}/T_{OCKD}	D1/D2 pins Setup/Hold with respect to CLK	0.45/ –0.08	0.50/ –0.08	0.54/ –0.08	0.54/ –0.08	0.69/ –0.11	ns
T_{OOCECK}/T_{OCKOCE}	OCE pin Setup/Hold with respect to CLK	0.17/ –0.03	0.20/ –0.03	0.22/ –0.03	0.27/ –0.05	0.27/ –0.04	ns
T_{OSRCK}/T_{OCKSR}	SR pin Setup/Hold with respect to CLK	0.59/ –0.24	0.62/ –0.24	0.54/ –0.08	0.54/ –0.08	0.79/ –0.35	ns
T_{OTCK}/T_{OCKT}	T1/T2 pins Setup/Hold with respect to CLK	0.44/ –0.07	0.51/ –0.07	0.56/ –0.07	0.60/ –0.10	0.68/ –0.13	ns
T_{OTCECK}/T_{OCKTCE}	TCE pin Setup/Hold with respect to CLK	0.15/ –0.04	0.19/ –0.04	0.21/ –0.04	0.27/ –0.05	0.29/ –0.05	ns
Combinatorial							
T_{DOQ}	D1 to OQ out or T1 to TQ out	0.78	0.87	1.01	1.01	1.15	ns
Sequential Delays							
T_{OCKQ}	CLK to OQ/TQ out	0.54	0.61	0.71	0.71	0.80	ns
T_{RQ}	SR pin to OQ/TQ out	0.80	0.90	1.05	1.05	1.19	ns
T_{GSRQ}	Global Set/Reset to Q outputs	7.60	7.60	10.51	10.51	10.51	ns
Set/Reset							
T_{RPW}	Minimum Pulse Width, SR inputs	0.78	0.95	1.20	1.20	1.30	ns, Min

Input Serializer/Deserializer Switching Characteristics

Table 51: **ISERDES Switching Characteristics**

Symbol	Description	Speed Grade					Units
		-3	-2	-1 (XC)	-1 (XQ)	-1L	
Setup/Hold for Control Lines							
$T_{ISCCK\_BITSLIP}$/ $T_{ISCKC\_BITSLIP}$	BITSLIP pin Setup/Hold with respect to CLKDIV	0.07/ 0.15	0.08/ 0.16	0.09/ 0.17	0.09/ 0.17	0.14/ 0.17	ns
T_{ISCCK_CE} / T_{ISCKC_CE}(2)	CE pin Setup/Hold with respect to CLK (for CE1)	0.20/ 0.03	0.25/ 0.04	0.27/ 0.04	0.27/ 0.04	0.31/ 0.05	ns
T_{ISCCK_CE2} / T_{ISCKC_CE2}(2)	CE pin Setup/Hold with respect to CLKDIV (for CE2)	0.01/ 0.27	0.01 0.29	0.01/ 0.31	0.01/ 0.31	–0.05/ 0.35	ns
Setup/Hold for Data Lines							
T_{ISDCK_D} /T_{ISCKD_D}	D pin Setup/Hold with respect to CLK	0.07/ 0.08	0.08/ 0.09	0.09/ 0.11	0.09/ 0.11	0.11/ 0.19	ns
T_{ISDCK_DDLY} /T_{ISCKD_DDLY}	DDLY pin Setup/Hold with respect to CLK (using IODELAY)(1)	0.10/ 0.05	0.12/ 0.06	0.14/ 0.07	0.14/ 0.07	0.16/ 0.15	ns
$T_{ISDCK\_D\_DDR}$ /$T_{ISCKD\_D\_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode	0.07/ 0.08	0.08/ 0.09	0.09/ 0.11	0.09/ 0.11	0.11/ 0.19	ns
$T_{ISDCK\_DDLY\_DDR}$ $T_{ISCKD\_DDLY\_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode (using IODELAY)(1)	0.10/ 0.05	0.12/ 0.06	0.14/ 0.07	0.14/ 0.07	0.16/ 0.15	ns
Sequential Delays							
T_{ISCKO_Q}	CLKDIV to out at Q pin	0.57	0.66	0.75	0.80	0.88	ns
Propagation Delays							
T_{ISDO_DO}	D input to DO output pin	0.19	0.22	0.25	0.25	0.28	ns

Notes:

1. Recorded at 0 tap value.
2. T_{ISCCK_CE2} and T_{ISCKC_CE2} are reported as T_{ISCCK_CE}/T_{ISCKC_CE} in TRACE report.

DSP48E1 Switching Characteristics

Table 58: **DSP48E1 Switching Characteristics**

Symbol	Description	Speed Grade					Units
		-3	-2	-1 (XC)	-1 (XQ)	-1L	
Setup and Hold Times of Data/Control Pins to the Input Register Clock							
$T_{DSPDCK\_\{A, ACIN; B, BCIN\}\_\{AREG; BREG\}}$/ $T_{DSPCKD\_\{A, ACIN; B, BCIN\}\_\{AREG; BREG\}}$	{A, ACIN, B, BCIN} input to {A, B} register CLK	0.25/ 0.27	0.29/ 0.30	0.35/ 0.34	0.36/ 0.34	0.46/ 0.39	ns
$T_{DSPDCK\_C\_CREG}$/$T_{DSPCKD\_C\_CREG}$	C input to C register CLK	0.16/ 0.20	0.19/ 0.22	0.22/ 0.24	0.25/ 0.24	0.33/ 0.30	ns
$T_{DSPDCK\_D\_DREG}$/$T_{DSPCKD\_D\_DREG}$	D input to D register CLK	0.07/ 0.31	0.10/ 0.34	0.15/ 0.39	0.16/ 0.39	0.24/ 0.45	ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock							
$T_{DSPDCK\_\{A, ACIN, B, BCIN\}\_MREG\_MULT}$/ $T_{DSPCKD\_\{A, ACIN, B, BCIN\}\_MREG\_MULT}$	{A, ACIN, B, BCIN} input to M register CLK	2.36/ 0.04	2.70/ 0.04	3.21/ 0.04	3.21/ 0.04	3.66/ 0.02	ns
$T_{DSPDCK\_\{A, D\}\_ADREG}$/ $T_{DSPCKD\_\{A, D\}\_ADREG}$	{A, D} input to AD register CLK	1.24/ 0.10	1.42/ 0.12	1.69/ 0.13	1.69/ 0.13	1.91/ 0.16	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock							
$T_{DSPDCK\_\{A, ACIN, B, BCIN\}\_PREG\_MULT}$/ $T_{DSPCKD\_\{A, ACIN, B, BCIN\}\_PREG\_MULT}$	{A, ACIN, B, BCIN} input to P register CLK using multiplier	3.83/ –0.13	4.37/ –0.13	5.20/ –0.13	5.20/ –0.13	5.94/ –0.24	ns
$T_{DSPDCK\_D\_PREG\_MULT}$/ $T_{DSPCKD\_D\_PREG\_MULT}$	D input to P register CLK	3.62/ –0.47	4.13/ –0.47	4.90/ –0.47	4.90/ –0.47	5.61/ –0.77	ns
$T_{DSPDCK\_\{A, ACIN, B, BCIN\}\_PREG}$/ $T_{DSPCKD\_\{A, ACIN, B, BCIN\}\_PREG}$	{A, ACIN, B, BCIN} input to P register CLK not using multiplier	1.59/ –0.13	1.81/ –0.13	2.15/ –0.13	2.15/ –0.13	2.44/ –0.24	ns
$T_{DSPDCK\_C\_PREG}$/ $T_{DSPCKD\_C\_PREG}$	C input to P register CLK	1.42/ –0.10	1.61/ –0.10	1.91/ –0.10	1.91/ –0.10	2.16/ –0.19	ns
$T_{DSPDCK\_\{PCIN, CARRYCASCIN, MULTSIGNIN\}\_PREG}$/ $T_{DSPCKD\_\{PCIN, CARRYCASCIN, MULTSIGNIN\}\_PREG}$	{PCIN, CARRYCASCIN, MULTSIGNIN} input to P register CLK	1.23/ –0.02	1.41/ –0.02	1.67/ –0.02	1.67/ –0.02	1.91/ –0.07	ns
Setup and Hold Times of the CE Pins							
$T_{DSPDCK\_\{CEA; CEB\}\_\{AREG; BREG\}}$/ $T_{DSPCKD\_\{CEA; CEB\}\_\{AREG; BREG\}}$	{CEA; CEB} input to {A; B} register CLK	0.14/ 0.19	0.17/ 0.22	0.22/ 0.25	0.22/ 0.25	0.30/ 0.28	ns
$T_{DSPDCK\_CEC\_CREG}$/ $T_{DSPCKD\_CEC\_CREG}$	CEC input to C register CLK	0.15/ 0.18	0.18/ 0.20	0.24/ 0.23	0.24/ 0.23	0.31/ 0.26	ns
$T_{DSPDCK\_CED\_DREG}$/ $T_{DSPCKD\_CED\_DREG}$	CED input to D register CLK	0.20/ 0.12	0.24/ 0.13	0.31/ 0.14	0.31/ 0.14	0.43/ 0.16	ns
$T_{DSPDCK\_CEM\_MREG}$/ $T_{DSPCKD\_CEM\_MREG}$	CEM input to M register CLK	0.16/ 0.19	0.20/ 0.21	0.26/ 0.25	0.26/ 0.25	0.32/ 0.28	ns
$T_{DSPDCK\_CEP\_PREG}$/ $T_{DSPCKD\_CEP\_PREG}$	CEP input to P register CLK	0.32/ 0.02	0.38/ 0.02	0.46/ 0.03	0.46/ 0.03	0.54/ 0.04	ns
Setup and Hold Times of the RST Pins							
$T_{DSPDCK\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$/ $T_{DSPCKD\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$	{RSTA, RSTB} input to {A, B} register CLK	0.27/ 0.17	0.31/ 0.19	0.38/ 0.22	0.38/ 0.22	0.41/ 0.25	ns
$T_{DSPDCK\_RSTC\_CREG}$/ $T_{DSPCKD\_RSTC\_CREG}$	RSTC input to C register CLK	0.18/ 0.08	0.20/ 0.08	0.23/ 0.09	0.23/ 0.09	0.27/ 0.11	ns
$T_{DSPDCK\_RSTD\_DREG}$/ $T_{DSPCKD\_RSTD\_DREG}$	RSTD input to D register CLK	0.28/ 0.15	0.32/ 0.16	0.38/ 0.19	0.38/ 0.19	0.45/ 0.21	ns
$T_{DSPDCK\_RSTM\_MREG}$/ $T_{DSPCKD\_RSTM\_MREG}$	RSTM input to M register CLK	0.20/ 0.24	0.23/ 0.26	0.26/ 0.30	0.26/ 0.30	0.29/ 0.34	ns

Table 58: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade					Units
		-3	-2	-1 (XC)	-1 (XQ)	-1L	
$T_{DSPDCK\_RSTP\_PREG}$/ $T_{DSPCKD\_RSTP\_PREG}$	RSTP input to P register CLK	0.26/ 0.04	0.30/ 0.04	0.35/ 0.05	0.35/ 0.05	0.43/ 0.06	ns
Combinatorial Delays from Input Pins to Output Pins							
$T_{DSPDO\_\{A, B\}\_\{P, CARRYOUT\}\_MULT}$	{A, B} input to {P, CARRYOUT} output using multiplier	3.76	4.29	5.08	5.08	5.87	ns
$T_{DSPDO\_D\_\{P, CARRYOUT\}\_MULT}$	D input to {P, CARRYOUT} output using multiplier	3.57	4.07	4.82	4.82	5.57	ns
$T_{DSPDO\_\{A, B\}\_\{P, CARRYOUT\}}$	{A, B} input to {P, CARRYOUT} output not using multiplier	1.55	1.76	2.07	2.07	2.41	ns
$T_{DSPDO\_\{C, CARRYIN\}\_\{P, CARRYOUT\}}$	{C, CARRYIN} input to {P, CARRYOUT} output	1.38	1.56	1.83	1.83	2.13	ns
Combinatorial Delays from Input Pins to Cascading Output Pins							
$T_{DSPDO\_\{A; B\}\_\{ACOUT; BCOUT\}}$	{A, B} input to {ACOUT, BCOUT} output	0.49	0.56	0.65	0.65	0.73	ns
$T_{DSPDO\_\{A, B\}\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_MULT}$	{A, B} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	3.87	4.42	5.24	5.24	6.09	ns
$T_{DSPDO\_D\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_MULT}$	D input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	3.66	4.17	4.94	4.94	5.76	ns
$T_{DSPDO\_\{A, B\}\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}}$	{A, B} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	1.64	1.86	2.19	2.19	2.60	ns
$T_{DSPDO\_\_\{C, CARRYIN\}\_\{PCOUT, CARRYCASCOUT,MULTSIGNOUT\}}$	{C, CARRYIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	1.46	1.66	1.95	1.95	2.32	ns
Combinatorial Delays from Cascading Input Pins to All Output Pins							
$T_{DSPDO\_\{ACIN, BCIN\}\_\{P, CARRYOUT\}\_MULT}$	{ACIN, BCIN} input to {P, CARRYOUT} output using multiplier	3.67	4.19	4.97	4.97	5.75	ns
$T_{DSPDO\_\{ACIN, BCIN\}\_\{P, CARRYOUT}$	{ACIN, BCIN} input to {P, CARRYOUT} output not using multiplier	1.43	1.63	1.92	1.92	2.25	ns
$T_{DSPDO\_\{ACIN; BCIN\}\_\{ACOUT; BCOUT\}}$	{ACIN, BCIN} input to {ACOUT, BCOUT} output	0.36	0.42	0.49	0.49	0.56	ns
$T_{DSPDO\_\{ACIN, BCIN\}\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}\_MULT}$	{ACIN, BCIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	3.76	4.29	5.10	5.10	5.94	ns
$T_{DSPDO\_\{ACIN, BCIN\}\_\{PCOUT, CARRYCASCOUT, MULTSIGNOUT\}}$	{ACIN, BCIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	1.52	1.73	2.05	2.05	2.44	ns
$T_{DSPDO\_\{PCIN, CARRYCASCIN, MULTSIGNIN\}\_\{P, CARRYOUT\}}$	{PCIN, CARRYCASCIN, MULTSIGNIN} input to {P, CARRYOUT} output	1.19	1.35	1.60	1.60	1.87	ns

Table 59: **Configuration Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
T_{SMCKBY}	CCLK to BUSY out in readback at 2.5V	6	6	6	7	ns, Max
	CCLK to BUSY out in readback at 1.8V	6	6	6	7	ns, Max
F_{SMCCK}	Maximum Frequency with respect to nominal CCLK	100	100	100	70	MHz, Max
F_{RBCCK}	Maximum Readback Frequency with respect to nominal CCLK	100	100	100	60	MHz, Max
$F_{MCCKTOL}$	Frequency tolerance, master mode with respect to nominal CCLK	55	55	55	60	%
Boundary-Scan Port Timing Specifications						
T_{TAPTCK}/T_{TCKTAP}	TMS and TDI Setup time before TCK/ Hold time after TCK	3.0/2.0	3.0/2.0	3.0/2.0	4.0/2.0	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output valid at 2.5V	6	6	6	7	ns, Max
	TCK falling edge to TDO output valid at 1.8V	6	6	6	7	ns, Max
F_{TCK}	Maximum configuration TCK clock frequency	66	66	66	33	MHz, Max
F_{TCKB_MIN}	Minimum boundary-scan TCK clock frequency when using IEEE Std 1149.6 (AC-JTAG). Minimum operating temperature for IEEE Std 1149.6 is 0°C.	15	15	15	15	MHz, Min
F_{TCKB}	Maximum boundary-scan TCK clock frequency	66	66	66	33	MHz, Max
BPI Master Flash Mode Programming Switching						
T_{BPICCO}[(2)]	ADDR[25:0], RS[1:0], FCS_B, FOE_B, FWE_B outputs valid after CCLK rising edge at 2.5V	6	6	6	7	ns
	ADDR[25:0], RS[1:0], FCS_B, FOE_B, FWE_B outputs valid after CCLK rising edge at 1.8V	6	6	6	7	ns
T_{BPIDCC}/T_{BPICCD}	Setup/Hold on D[15:0] data input pins	4.0/0.0	4.0/0.0	4.0/0.0	5.0/0.0	ns
$T_{INITADDR}$	Minimum period of initial ADDR[25:0] address cycles	3	3	3	3	CCLK cycles
SPI Master Flash Mode Programming Switching						
$T_{SPIDCC}/T_{SPIDCCD}$	DIN Setup/Hold before/after the rising CCLK edge	3.0/0.0	3.0/0.0	3.0/0.0	3.5/0.0	ns
T_{SPICCM}	MOSI clock to out at 2.5V	6	6	6	7	ns
	MOSI clock to out at 1.8V	6	6	6	7	ns
$T_{SPICCFC}$	FCS_B clock to out at 2.5V	6	6	6	7	ns
	FCS_B clock to out at 1.8V	6	6	6	7	ns
$T_{FSINIT}/T_{FSINITH}$	FS[2:0] to INIT_B rising edge Setup and Hold	2	2	2	2	µs
CCLK Output (Master Modes)						
T_{MCCKL}	Master CCLK clock Low time duty cycle	45/55	45/55	45/55	40/60	%, Min/Max
T_{MCCKH}	Master CCLK clock High time duty cycle	45/55	45/55	45/55	40/60	%, Min/Max
CCLK Input (Slave Modes)						
T_{SCCKL}	Slave CCLK clock minimum Low time	2.5	2.5	2.5	2.5	ns, Min
T_{SCCKH}	Slave CCLK clock minimum High time	2.5	2.5	2.5	2.5	ns, Min
Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK						
F_{DCK}	Maximum frequency for DCLK	200	200	200	200	MHz
$T_{MMCMDCK\_DADDR}$/ $T_{MMCMCKD\_DADDR}$	DADDR Setup/Hold	1.25/ 0.00	1.40/ 0.00	1.63/ 0.00	1.64/ 0.00	ns

Table 64: **MMCM Specification *(Cont'd)***

Symbol	Description	Speed Grade				Units
		-3	-2	-1	-1L	
$RST_{MINPULSE}$	Minimum Reset Pulse Width	1.5	1.5	1.5	1.5	ns
F_{PFDMAX}	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to High or Optimized(9)	550	500	450	450	MHz
	Maximum Frequency at the Phase Frequency Detector with Bandwidth Set to Low	300	300	300	300	MHz
F_{PFDMIN}	Minimum Frequency at the Phase Frequency Detector with Bandwidth Set to High or Optimized	135	135	135	135	MHz
	Minimum Frequency at the Phase Frequency Detector with Bandwidth Set to Low	10	10	10	10	MHz
$T_{FBDELAY}$	Maximum Delay in the Feedback Path	3 ns Max or one CLKIN cycle				
$T_{MMCMDCK\_PSEN}$/ $T_{MMCMCKD\_PSEN}$	Setup and Hold of Phase Shift Enable	1.04 0.00	1.04 0.00	1.04 0.00	1.04 0.00	ns
$T_{MMCMDCK\_PSINCDEC}$/ $T_{MMCMCKD\_PSINCDEC}$	Setup and Hold of Phase Shift Increment/Decrement	1.04 0.00	1.04 0.00	1.04 0.00	1.04 0.00	ns
$T_{MMCMCKO\_PSDONE}$	Phase Shift Clock-to-Out of PSDONE	0.32	0.34	0.38	0.38	ns

Notes:

1. When DIVCLK_DIVIDE = 3 or 4, F_{INMAX} is 315 MHz.
2. This duty cycle specification does not apply to the GTH_QUAD (GTH) to MMCM connection. The GTH transceivers drive the MMCMs at the following maximum frequencies: 323 MHz for -1 speed grade devices, 350 MHz for -2 speed grade devices, or 350 MHz for -3 speed grade devices.
3. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
4. The static offset is measured between any MMCM outputs with identical phase.
5. Values for this parameter are available in the Clocking Wizard. See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
6. Includes global clock buffer.
7. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.
8. When CASCADE4_OUT = TRUE, F_{OUTMIN} is 0.036 MHz.
9. In ISE software 12.3 (or earlier versions supporting the Virtex-6 family), the phase frequency detector Optimized bandwidth setting is equivalent to the High bandwidth setting. Starting with ISE software 12.4, the Optimized bandwidth setting is automatically adjusted to Low when the software can determine that the phase frequency detector input is less than 135 MHz.

Table 66: **Global Clock Input to Output Delay With MMCM**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* MMCM.							
$T_{ICKOFMMCMGC}$	Global Clock Input and OUTFF *with* MMCM	XC6VLX75T	2.34	2.50	2.77	2.85	ns
		XC6VLX130T	2.35	2.51	2.78	2.87	ns
		XC6VLX195T	2.36	2.52	2.79	2.88	ns
		XC6VLX240T	2.36	2.52	2.79	2.88	ns
		XC6VLX365T	2.37	2.53	2.79	2.89	ns
		XC6VLX550T	N/A	2.55	2.82	2.93	ns
		XC6VLX760	N/A	2.54	2.82	2.92	ns
		XC6VSX315T	2.35	2.51	2.79	2.87	ns
		XC6VSX475T	N/A	2.43	2.70	2.79	ns
		XC6VHX250T	2.36	2.53	2.80	N/A	ns
		XC6VHX255T	2.46	2.63	2.91	N/A	ns
		XC6VHX380T	2.39	2.59	2.83	N/A	ns
		XC6VHX565T	N/A	2.54	2.81	N/A	ns
		XQ6VLX130T	N/A	2.51	2.78	2.87	ns
		XQ6VLX240T	N/A	2.52	2.79	2.88	ns
		XQ6VLX550T	N/A	N/A	2.82	2.93	ns
		XQ6VSX315T	N/A	2.51	2.79	2.87	ns
		XQ6VSX475T	N/A	N/A	2.70	2.79	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Virtex-6 Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 68. Values are expressed in nanoseconds unless otherwise noted.

Table 68: **Global Clock Input Setup and Hold Without MMCM**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)							
T_{PSFD}/ T_{PHFD}	Full Delay (Legacy Delay or Default Delay) Global Clock Input and IFF(2) without MMCM	XC6VLX75T	1.33/ 0.03	1.44/ 0.03	1.75/ 0.03	2.18/ –0.22	ns
		XC6VLX130T	1.31/ –0.08	1.54/ –0.08	1.88/ –0.08	2.31/ –0.12	ns
		XC6VLX195T	1.36/ –0.11	1.60/ –0.11	1.97/ –0.11	2.40/ –0.25	ns
		XC6VLX240T	1.36/ –0.11	1.60/ –0.11	1.97/ –0.11	2.40/ –0.25	ns
		XC6VLX365T	1.79/ –0.28	1.87/ –0.28	2.17/ –0.28	2.48/ –0.24	ns
		XC6VLX550T	N/A	2.22/ –0.12	2.36/ –0.12	2.77/ –0.26	ns
		XC6VLX760	N/A	2.19/ –0.24	2.35/ –0.24	2.71/ –0.21	ns
		XC6VSX315T	1.75/ –0.09	1.85/ –0.09	2.06/ –0.09	2.47/ –0.24	ns
		XC6VSX475T	N/A	2.14/ –0.14	2.31/ –0.14	2.71/ –0.30	ns
		XC6VHX250T	1.93/ –0.22	2.04/ –0.22	2.25/ –0.22	N/A	ns
		XC6VHX255T	1.81/ –0.33	2.11/ –0.33	2.56/ –0.33	N/A	ns
		XC6VHX380T	1.93/ –0.11	2.04/ –0.11	2.25/ –0.11	N/A	ns
		XC6VHX565T	N/A	2.20/ –0.12	2.39/ –0.12	N/A	ns
		XQ6VLX130T	N/A	1.54/ –0.08	1.88/ –0.08	2.31/ –0.12	ns
		XQ6VLX240T	N/A	1.60/ –0.11	1.97/ –0.11	2.40/ –0.25	ns
		XQ6VLX550T	N/A	N/A	2.36/ –0.12	2.77/ –0.26	ns
		XQ6VSX315T	N/A	1.85/ –0.09	2.06/ –0.09	2.47/ –0.24	ns
		XQ6VSX475T	N/A	N/A	2.31/ –0.14	2.71/ –0.30	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Table 69: **Global Clock Input Setup and Hold With MMCM**

Symbol	Description	Device	Speed Grade				Units
			-3	-2	-1	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)							
$T_{PSMMCMGC}$/ $T_{PHMMCMGC}$	No Delay Global Clock Input and IFF(2) with MMCM	XC6VLX75T	1.45/ –0.18	1.57/ –0.18	1.72/ –0.18	1.78/ –0.08	ns
		XC6VLX130T	1.53/ –0.18	1.65/ –0.18	1.81/ –0.18	1.87/ –0.07	ns
		XC6VLX195T	1.54/ –0.17	1.66/ –0.17	1.82/ –0.17	1.87/ –0.08	ns
		XC6VLX240T	1.54/ –0.17	1.66/ –0.17	1.82/ –0.17	1.87/ –0.08	ns
		XC6VLX365T	1.55/ –0.18	1.67/ –0.18	1.83/ –0.18	1.87/ –0.07	ns
		XC6VLX550T	N/A	1.84/ –0.17	2.02/ –0.17	2.06/ –0.06	ns
		XC6VLX760	N/A	2.26/ –0.13	2.49/ –0.13	2.06/ –0.03	ns
		XC6VSX315T	1.56/ –0.18	1.68/ –0.18	1.84/ –0.18	1.89/ –0.08	ns
		XC6VSX475T	N/A	1.85/ –0.23	2.03/ –0.23	2.07/ –0.13	ns
		XC6VHX250T	1.52/ –0.17	1.64/ –0.17	1.80/ –0.17	N/A	ns
		XC6VHX255T	1.52/ –0.12	1.64/ –0.12	1.85/ –0.12	N/A	ns
		XC6VHX380T	1.68/ –0.16	1.81/ –0.16	1.99/ –0.16	N/A	ns
		XC6VHX565T	N/A	1.81/ –0.01	1.99/ –0.01	N/A	ns
		XQ6VLX130T	N/A	1.65/ –0.18	1.81/ –0.18	1.87/ –0.07	ns
		XQ6VLX240T	N/A	1.66/ –0.17	1.82/ –0.17	1.87/ –0.08	ns
		XQ6VLX550T	N/A	N/A	2.02/ –0.17	2.06/ –0.06	ns
		XQ6VSX315T	N/A	1.68/ –0.18	1.84/ –0.18	1.89/ –0.08	ns
		XQ6VSX475T	N/A	N/A	2.03/ –0.23	2.07/ –0.13	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 72: **Package Skew**

Symbol	Description	Device	Package	Value	Units
$T_{PKGSKEW}$	Package Skew(1)	XC6VLX75T	FF484	95	ps
			FF784	146	ps
		XC6VLX130T	FF484	95	ps
			FF784	146	ps
			FF1156	165	ps
		XC6VLX195T	FF784	145	ps
			FF1156	182	ps
		XC6VLX240T	FF784	146	ps
			FF1156	182	ps
			FF1759	187	ps
		XC6VLX365T	FF1156	189	ps
			FF1759	184	ps
		XC6VLX550T	FF1759	196	ps
			FF1760	249	ps
		XC6VLX760	FF1760	236	ps
		XC6VSX315T	FF1156	168	ps
			FF1759	190	ps
		XC6VSX475T	FF1156	168	ps
			FF1759	204	ps
		XC6VHX250T	FF1154	166	ps
		XC6VHX255T	FF1155	168	ps
			FF1923	228	ps
		XC6VHX380T	FF1154	159	ps
			FF1155	172	ps
			FF1923	227	ps
			FF1924	220	ps
		XC6VHX565T	FF1923	232	ps
			FF1924	197	ps
		XQ6VLX130T	RF784	146	ps
			RF1156	165	ps
			FFG1156	165	ps
		XQ6VLX240T	RF784	146	ps
			RF1156	182	ps
			FFG1156	182	ps
			RF1759	187	ps
		XQ6VLX550T	RF1759	196	ps
		XQ6VSX315T	RF1156	168	ps
			FFG1156	168	ps
			RF1759	190	ps
		XQ6VSX475T	RF1156	168	ps
			FFG1156	168	ps
			RF1759	204	ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest flight time to longest flight time from Pad to Ball (7.0 ps per mm).
2. Package trace length information is available for these device/package combinations. This information can be used to deskew the package.