Intel - EP2SGX130GF1508C3 Datasheet

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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	6627
Number of Logic Elements/Cells	132540
Total RAM Bits	6747840
Number of I/O	734
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1508-BBGA, FCBGA
Supplier Device Package	1508-FBGA, FC (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2sgx130gf1508c3

- Support for multiple intellectual property megafunctions from Altera® MegaCore® functions and Altera Megafunction Partners Program (AMPP^{SM}) megafunctions
- Support for design security using configuration bitstream encryption
- Support for remote configuration updates

- Transceiver block features:
  - High-speed serial transceiver channels with clock data recovery (CDR) provide 600-megabits per second (Mbps) to 6.375-Gbps full-duplex transceiver operation per channel
  - Devices available with 4, 8, 12, 16, or 20 high-speed serial transceiver channels providing up to 255 Gbps of serial bandwidth (full duplex)
  - Dynamically programmable voltage output differential (V_{OD}) and pre-emphasis settings for improved signal integrity
  - Support for CDR-based serial protocols, including PCI Express, Gigabit Ethernet, SDI, Altera's SerialLite II, XAUI, CEI-6G, CPRI, Serial RapidIO, SONET/SDH
  - Dynamic reconfiguration of transceiver channels to switch between multiple protocols and data rates
  - Individual transmitter and receiver channel power-down capability for reduced power consumption during non-operation
  - Adaptive equalization (AEQ) capability at the receiver to compensate for changing link characteristics
  - Selectable on-chip termination resistors (100, 120, or 150 Ω) for improved signal integrity on a variety of transmission media
  - Programmable transceiver-to-FPGA interface with support for 8-, 10-, 16-, 20-, 32-, and 40-bit wide data transfer
  - 1.2- and 1.5-V pseudo current mode logic (PCML) for 600 Mbps to 6.375 Gbps (AC coupling)
  - Receiver indicator for loss of signal (available only in PIPE mode)
  - Built-in self test (BIST)
  - Hot socketing for hot plug-in or hot swap and power sequencing support without the use of external devices
  - Rate matcher, byte-reordering, bit-reordering, pattern detector, and word aligner support programmable patterns
  - Dedicated circuitry that is compliant with PIPE, XAUI, and GIGE
  - Built-in byte ordering so that a frame or packet always starts in a known byte lane
  - Transmitters with two PLL inputs for each transceiver block with independent clock dividers to provide varying clock rates on each of its transmitters

Table 1–1. Stratix II GX Device Features (Part 2 of 2)

Feature	EP2SGX30C/D		EP2SGX60C/D/E			EP2SGX90E/F		EP2SGX130/G
	C	D	C	D	E	E	F	G
Package	780-pin FineLine BGA		780-pin FineLine BGA		1,152-pin FineLine BGA	1,152-pin FineLine BGA	1,508-pin FineLine BGA	1,508-pin FineLine BGA

Note to Table 1–1:
(1) Includes two sets of dual-purpose differential pins that can be used as two additional channels for the differential receiver or differential clock inputs.

Stratix II GX devices are available in space-saving FineLine BGA packages (refer to Table 1–2). All Stratix II GX devices support vertical migration within the same package. Vertical migration means that you can migrate to devices whose dedicated pins, configuration pins, and power pins are the same for a given package across device densities. For I/O pin migration across densities, you must cross-reference the available I/O pins using the device pin-outs for all planned densities of a given package type to identify which I/O pins are migratable. Table 1–3 lists the Stratix II GX device package sizes.

Table 1–2. Stratix II GX Package Options (Pin Counts and Transceiver Channels)

Device	Transceiver Channels	Source-Synchronous Channels		Maximum User I/O Pin Count		
		Receive *(1)*	Transmit	780-Pin FineLine BGA (29 mm)	1,152-Pin FineLine BGA (35 mm)	1,508-Pin FineLine BGA (40 mm)
EP2SGX30C	4	31	29	361	—	—
EP2SGX60C	4	31	29	364	—	—
EP2SGX30D	8	31	29	361	—	—
EP2SGX60D	8	31	29	364	—	—
EP2SGX60E	12	42	42	—	534	—
EP2SGX90E	12	47	45	—	558	—
EP2SGX90F	16	59	59	—	—	650
EP2SGX130G	20	73	71	—	—	734

Note to Table 1–2:
(1) Includes two differential clock inputs that can also be used as two additional channels for the differential receiver.

Table 2–18. Stratix II GX Device Routing Scheme (Part 2 of 2)

Source	Destination															
	Shared Arithmetic Chain	Carry Chain	Register Chain	Local Interconnect	Direct Link Interconnect	R4 Interconnect	R24 Interconnect	C4 Interconnect	C16 Interconnect	ALM	M512 RAM Block	M4K RAM Block	M-RAM Block	DSP Blocks	Column IOE	Row IOE
Column IOE					✓			✓	✓							
Row IOE					✓	✓	✓	✓								

TriMatrix Memory

TriMatrix memory consists of three types of RAM blocks: M512, M4K, and M-RAM. Although these memory blocks are different, they can all implement various types of memory with or without parity, including true dual-port, simple dual-port, and single-port RAM, ROM, and FIFO buffers. Table 2–19 shows the size and features of the different RAM blocks.

Table 2–19. TriMatrix Memory Features (Part 1 of 2)

Memory Feature	M512 RAM Block (32 × 18 Bits)	M4K RAM Block (128 × 36 Bits)	M-RAM Block (4K × 144 Bits)
Maximum performance	500 MHz	550 MHz	420 MHz
True dual-port memory		✓	✓
Simple dual-port memory	✓	✓	✓
Single-port memory	✓	✓	✓
Shift register	✓	✓	
ROM	✓	✓	*(1)*
FIFO buffer	✓	✓	✓
Pack mode		✓	✓
Byte enable	✓	✓	✓
Address clock enable		✓	✓
Parity bits	✓	✓	✓
Mixed clock mode	✓	✓	✓
Memory initialization (**.mif**)	✓	✓	

Table 2–26 shows the enhanced PLL and fast PLL features in Stratix II GX devices.

Table 2–26. Stratix II GX PLL Features

Feature	Enhanced PLL	Fast PLL
Clock multiplication and division	*m*/(*n* × post-scale counter) *(1)*	*m*/(*n* × post-scale counter) *(2)*
Phase shift	Down to 125-ps increments *(3)*, *(4)*	Down to 125-ps increments *(3)*, *(4)*
Clock switchover	✓	✓ *(5)*
PLL reconfiguration	✓	✓
Reconfigurable bandwidth	✓	✓
Spread spectrum clocking	✓	
Programmable duty cycle	✓	✓
Number of internal clock outputs	6	4
Number of external clock outputs	Three differential/six single-ended	*(6)*
Number of feedback clock inputs	One single-ended or differential *(7)*, *(8)*	

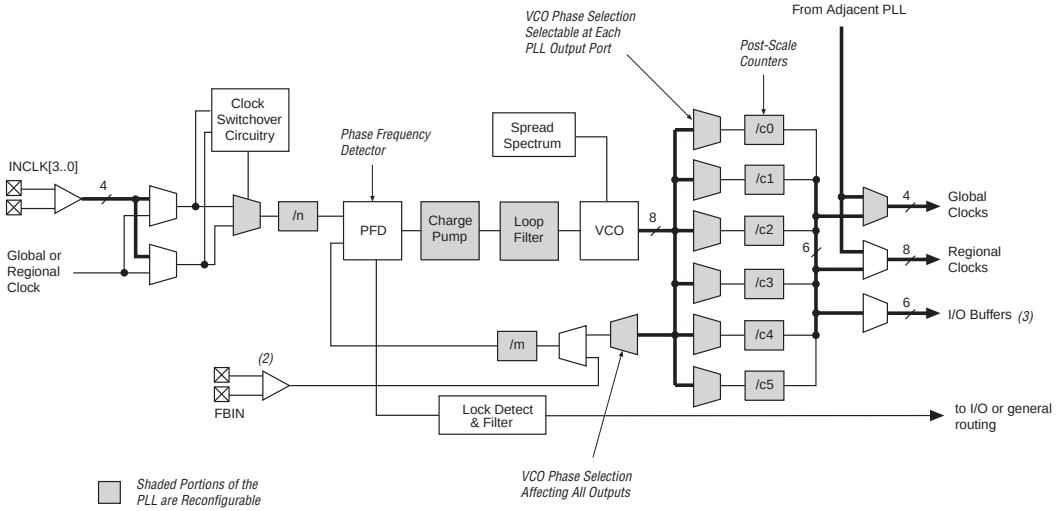
Notes to Table 2–26:

(1) For enhanced PLLs, *m*, *n* range from 1 to 256 and post-scale counters range from 1 to 512 with 50% duty cycle.
(2) For fast PLLs, *m*, and post-scale counters range from 1 to 32. The *n* counter ranges from 1 to 4.
(3) The smallest phase shift is determined by the voltage controlled oscillator (VCO) period divided by 8.
(4) For degree increments, Stratix II GX devices can shift all output frequencies in increments of at least 45. Smaller degree increments are possible depending on the frequency and divide parameters.
(5) Stratix II GX fast PLLs only support manual clock switchover.
(6) Fast PLLs can drive to any I/O pin as an external clock. For high-speed differential I/O pins, the device uses a data channel to generate `txclkout`.
(7) If the feedback input is used, you will lose one (or two, if f_{BIN} is differential) external clock output pin.
(8) Every Stratix II GX device has at least two enhanced PLLs with one single-ended or differential external feedback input per PLL.

Enhanced PLLs

Stratix II GX devices contain up to four enhanced PLLs with advanced clock management features. These features include support for external clock feedback mode, spread-spectrum clocking, and counter cascading. Figure 2–74 shows a diagram of the enhanced PLL.

Figure 2–74. Stratix II GX Enhanced PLL *Note (1)*



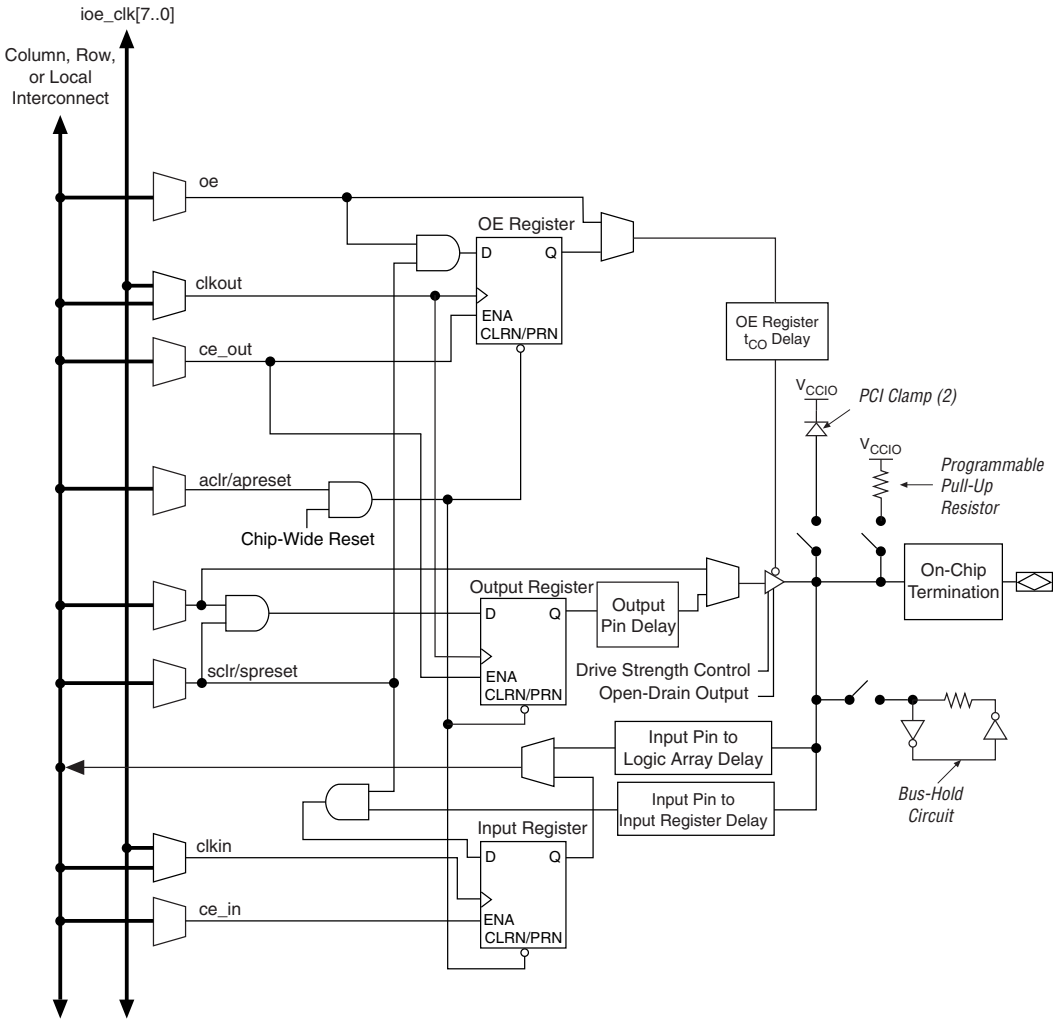
Notes to Figure 2–74:

(1) Each clock source can come from any of the four clock pins that are physically located on the same side of the device as the PLL.
(2) If the feedback input is used, you will lose one (or two, if FBIN is differential) external clock output pin.
(3) Each enhanced PLL has three differential external clock outputs or six single-ended external clock outputs.
(4) The global or regional clock input can be driven by an output from another PLL, a pin-driven dedicated global or regional clock, or through a clock control block provided the clock control block is fed by an output from another PLL or a pin-driven dedicated global or regional clock. An internally generated global signal cannot drive the PLL.

Fast PLLs

Stratix II GX devices contain up to four fast PLLs with high-speed serial interfacing ability. The fast PLLs offer high-speed outputs to manage the high-speed differential I/O interfaces. Figure 2–75 shows a diagram of the fast PLL.

Figure 2–81. Stratix II GX IOE in Bidirectional I/O Configuration *Note (1)*



Notes to Figure 2–81:
(1) All input signals to the IOE can be inverted at the IOE.
(2) The optional PCI clamp is only available on column I/O pins.

The Stratix II GX device IOE includes programmable delays that can be activated to ensure input IOE register-to-logic array register transfers, input pin-to-logic array register transfers, or output IOE register-to-pin transfers.

16 transmitter channels in I/O bank 1 or a maximum of 29 transmitter channels in I/O banks 1 and 2. The Quartus II software can also merge receiver and transmitter PLLs when a receiver is driving a transmitter. In this case, one fast PLL can drive both the maximum numbers of receiver and transmitter channels.

Table 2–38. EP2SGX30 Device Differential Channels *Note (1)*

Package	Transmitter/Receiver	Total Channels	Center Fast PLLs Package	
			PLL1	PLL2
780-pin FineLine BGA	Transmitter	29	16	13
	Receiver	31	17	14

Table 2–39. EP2SGX60 Device Differential Channels *Note (1)*

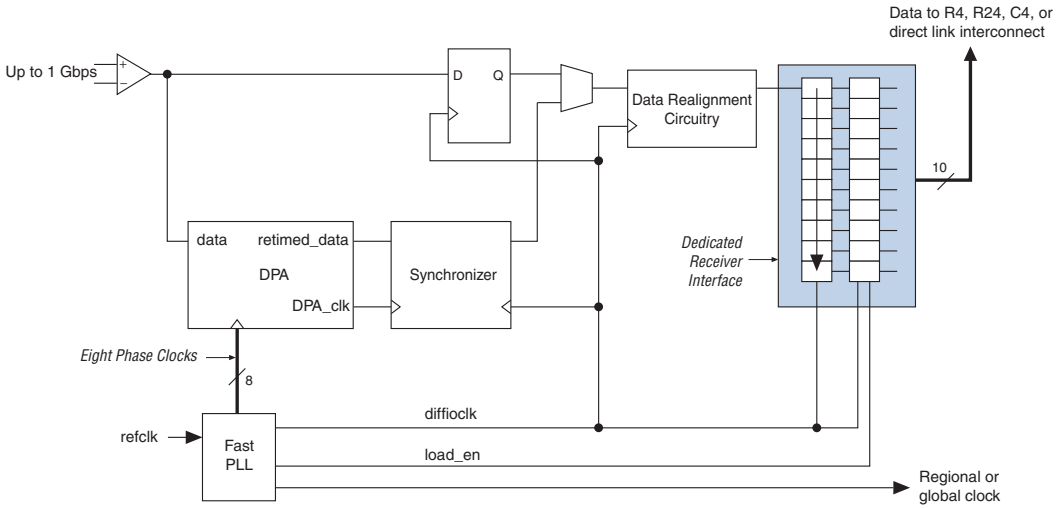
Package	Transmitter/Receiver	Total Channels	Center Fast PLLs		Corner Fast PLLs	
			PLL1	PLL2	PLL7	PLL8
780-pin FineLine BGA	Transmitter	29	16	13	—	—
	Receiver	31	17	14	—	—
1,152-pin FineLine BGA	Transmitter	42	21	21	21	21
	Receiver	42	21	21	21	21

Table 2–40. EP2SGX90 Device Differential Channels *Note (1)*

Package	Transmitter/Receiver	Total Channels	Center Fast PLLs		Corner Fast PLLs	
			PLL1	PLL2	PLL7	PLL8
1,152-pin FineLine BGA	Transmitter	45	23	22	23	22
	Receiver	47	23	24	23	24
1,508-pin FineLine BGA	Transmitter	59	30	29	29	29
	Receiver	59	30	29	29	29

Figure 2–89 shows the block diagram of the Stratix II GX receiver channel.

Figure 2–89. Stratix II GX Receiver Channel



An external pin or global or regional clock can drive the fast PLLs, which can output up to three clocks: two multiplied high-speed clocks to drive the SERDES block and/or external pin, and a low-speed clock to drive the logic array. In addition, eight phase-shifted clocks from the VCO can feed to the DPA circuitry.

For more information on the fast PLL, see the *PLLs in Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Handbook*.

The eight phase-shifted clocks from the fast PLL feed to the DPA block. The DPA block selects the closest phase to the center of the serial data eye to sample the incoming data. This allows the source-synchronous circuitry to capture incoming data correctly regardless of the channel-to-channel or clock-to-channel skew. The DPA block locks to a phase closest to the serial data phase. The phase-aligned DPA clock is used to write the data into the synchronizer.

The synchronizer sits between the DPA block and the data realignment and SERDES circuitry. Since every channel utilizing the DPA block can have a different phase selected to sample the data, the synchronizer is needed to synchronize the data to the high-speed clock domain of the data realignment and the SERDES circuitry.

Table 2–42. Document Revision History (Part 3 of 6)

Date and Document Version	Changes Made	Summary of Changes
	Moved the "Transmit State Machine" section to after the "8B/10B Encoder" section.	
	Moved the "PCI Express Receiver Detect" and "PCI Express Electric Idles (or Individual Transmitter Tri-State)" sections to after the "Transmit Buffer" section.	
	Moved the "Dynamic Reconfiguration" section to the "Other Transceiver Features" section.	
	Moved the "Calibration Block", "Receiver PLL & CRU", and "Deserializer (Serial-to-Parallel Converter)" sections to the "Receiver Path" section.	
	Moved the "8B/10B Decoder" and "Receiver State Machine" sections to after the "Rate Matcher" section.	
	Moved the "Byte Ordering Block" section to after the "Byte Deserializer" section.	
	Updated the Clocking diagrams.	
	Added the "Clock Resource for PLD-Transceiver Interface" section.	
	Added the "On-Chip Parallel Termination with Calibration" section to the "On-Chip Termination" section.	
	Updated: ● Table 2–2. ● Table 2–10 ● Table 2–14. ● Table 2–3. ● Table 2–5. ● Table 2–8. ● Table 2–13 ● Table 2–18 ● Table 2–19 ● Table 2–29.	
	Updated Figures 2–3, 2–9, 2–24, 2–25, 2–28, 2–29, 2–60, 2–62.	
	Change 622 Mbps to 600 Mbps throughout the chapter.	

Final timing numbers are based on actual device operation and testing. These numbers reflect the actual performance of the device under worst-case voltage and junction temperature conditions.

Table 4–52. Stratix II GX Device Timing Model Status

Device	Preliminary	Final
EP2SGX30		✓
EP2SGX60		✓
EP2SGX90		✓
EP2SGX130		✓

I/O Timing Measurement Methodology

Different I/O standards require different baseline loading techniques for reporting timing delays. Altera characterizes timing delays with the required termination for each I/O standard and with 0 pF (except for PCI and PCI-X which use 10 pF) loading and the timing is specified up to the output pin of the FPGA device. The Quartus II software calculates the I/O timing for each I/O standard with a default baseline loading as specified by the I/O standards.

The following measurements are made during device characterization. Altera measures clock-to-output delays (t_{CO}) at worst-case process, minimum voltage, and maximum temperature (PVT) for default loading conditions shown in Table 4–53. Use the following equations to calculate clock pin to output pin timing for Stratix II GX devices.

t_{CO} from clock pin to I/O pin = delay from clock pad to I/O output register + IOE output register clock-to-output delay + delay from output register to output pin + I/O output delay

t_{xz}/t_{zx} from clock pin to I/O pin = delay from clock pad to I/O output register + IOE output register clock-to-output delay + delay from output register to output pin + I/O output delay + output enable pin delay

Simulation using IBIS models is required to determine the delays on the PCB traces in addition to the output pin delay timing reported by the Quartus II software and the timing model in the device handbook.

1. Simulate the output driver of choice into the generalized test setup, using values from Table 4–53.
2. Record the time to V_{MEAS}.

Figure 4–10. Measurement Setup for t_{zx}

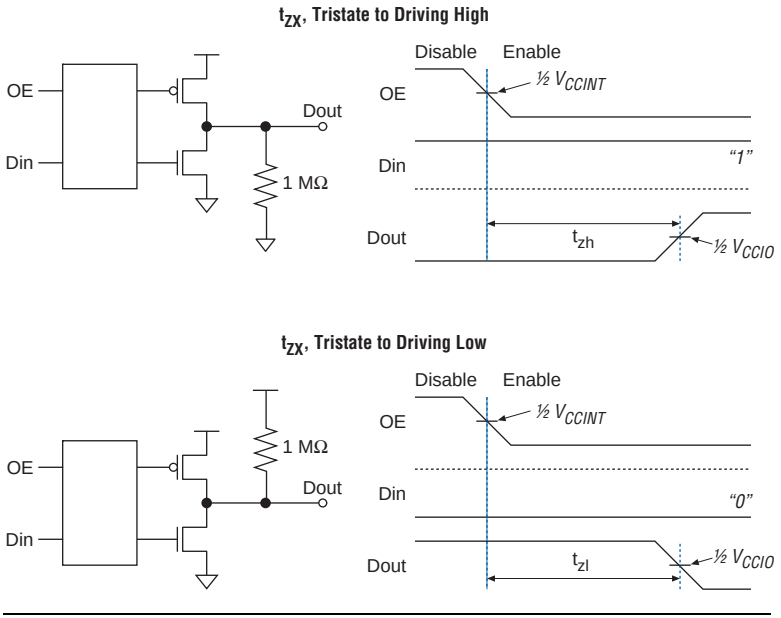


Table 4–54 specifies the input timing measurement setup.

Table 4–54. Timing Measurement Methodology for Input Pins (Part 1 of 2) *Notes (1), (2), (3), (4)*

I/O Standard	Measurement Conditions			Measurement Point
	V_{CCIO} (V)	V_{REF} (V)	Edge Rate (ns)	VMEAS (V)
LVTTL *(5)*	3.135		3.135	1.5675
LVCMOS *(5)*	3.135		3.135	1.5675
2.5 V *(5)*	2.375		2.375	1.1875
1.8 V *(5)*	1.710		1.710	0.855
1.5 V *(5)*	1.425		1.425	0.7125
PCI *(6)*	2.970		2.970	1.485
PCI-X *(6)*	2.970		2.970	1.485
SSTL-2 Class I	2.325	1.163	2.325	1.1625
SSTL-2 Class II	2.325	1.163	2.325	1.1625
SSTL-18 Class I	1.660	0.830	1.660	0.83
SSTL-18 Class II	1.660	0.830	1.660	0.83
1.8-V HSTL Class I	1.660	0.830	1.660	0.83

Table 4–55 shows the Stratix II GX performance for some common designs. All performance values were obtained with the Quartus II software compilation of LPM or MegaCore functions for FIR and FFT designs.

Table 4–55. Stratix II GX Performance Notes (Part 1 of 3) *Note (1)*

Applications		Resources Used			Performance				
		ALUTs	TriMatrix Memory Blocks	DSP Blocks	-3 Speed Grade (2)	-3 Speed Grade (3)	-4 Speed Grade	-5 Speed Grade	Units
LE	16-to-1 multiplexer (4)	21	0	0	657.03	620.73	589.62	477.09	MHz
	32-to-1 multiplexer (4)	38	0	0	534.75	517.33	472.81	369.27	MHz
	16-bit counter	16	0	0	568.18	539.66	507.61	422.47	MHz
	64-bit counter	64	0	0	242.54	231.0	217.77	180.31	MHz
TriMatrix Memory M512 block	Simple dual-port RAM 32 x 18bit	0	1	0	500.0	476.19	447.22	373.13	MHz
	FIFO 32 x 18 bit	22	1	0	500.00	476.19	460.82	373.13	MHz
TriMatrix Memory M4K block	Simple dual-port RAM 128 x 36bit	0	1	0	540.54	515.46	483.09	401.6	MHz
	True dual-port RAM 128 x 18bit	0	1	0	540.54	515.46	483.09	401.6	MHz
	FIFO 128 x 36 bit	22	1	0	524.10	500.25	466.41	381.38	MHz

Table 4–84. Stratix II GX I/O Input Delay for Column Pins (Part 3 of 3)							
I/O Standard	**Parameter**	**Fast Corner Industrial/ Commercial**	**-3 Speed Grade** *(2)*	**-3 Speed Grade** *(3)*	**-4 Speed Grade**	**-5 Speed Grade**	**Unit**
Differential SSTL-2 Class II *(1)*	t_{PI}	530	818	857	912	1094	ps
	t_{PCOUT}	251	382	400	426	511	ps
Differential SSTL-18 Class I *(1)*	t_{PI}	569	898	941	1001	1201	ps
	t_{PCOUT}	290	462	484	515	618	ps
Differential SSTL-18 Class II *(1)*	t_{PI}	569	898	941	1001	1201	ps
	t_{PCOUT}	290	462	484	515	618	ps
1.8-V differential HSTL Class I *(1)*	t_{PI}	569	898	941	1001	1201	ps
	t_{PCOUT}	290	462	484	515	618	ps
1.8-V differential HSTL Class II *(1)*	t_{PI}	569	898	941	1001	1201	ps
	t_{PCOUT}	290	462	484	515	618	ps
1.5-V differential HSTL Class I *(1)*	t_{PI}	587	993	1041	1107	1329	ps
	t_{PCOUT}	308	557	584	621	746	ps
1.5-V differential HSTL Class II *(1)*	t_{PI}	587	993	1041	1107	1329	ps
	t_{PCOUT}	308	557	584	621	746	ps

(1) These I/O standards are only supported on DQS pins.
(2) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
(3) This column refers to –3 speed grades for EP2SGX130 devices.

Table 4–85. Stratix II GX I/O Input Delay for Row Pins (Part 1 of 3)							
I/O Standard	**Parameter**	**Fast Corner Industrial/ Commercial**	**-3 Speed Grade** *(2)*	**-3 Speed Grade** *(3)*	**-4 Speed Grade**	**-5 Speed Grade**	**Unit**
LVTTL	t_{PI}	749	1287	1350	1435	1723	ps
	t_{PCOUT}	410	760	798	848	1018	ps
2.5 V	t_{PI}	761	1273	1335	1419	1704	ps
	t_{PCOUT}	422	746	783	832	999	ps
1.8 V	t_{PI}	827	1427	1497	1591	1911	ps
	t_{PCOUT}	488	900	945	1004	1206	ps
1.5 V	t_{PI}	830	1498	1571	1671	2006	ps
	t_{PCOUT}	491	971	1019	1084	1301	ps

Table 4–92. Stratix II GX Maximum Output Clock Rate for Row Pins (Part 2 of 2)					
I/O Standard	**Drive Strength**	**-3 Speed Grade**	**-4 Speed Grade**	**-5 Speed Grade**	**Unit**
Differential SSTL-2 Class I	8 mA	400	300	300	MHz
	12 mA	400	400	350	MHz
Differential SSTL-2 Class II	16 mA *(1)*	350	350	300	MHz
Differential SSTL-18 Class I	4 mA	200	150	150	MHz
	6 mA	350	250	200	MHz
	8 mA	450	300	300	MHz
	10 mA *(1)*	500	400	400	MHz
LVDS	-	717	717	640	MHz
HyperTransport	-	717	717	640	MHz

(1) This is the default setting in Quartus II software.

Table 4–93 shows the maximum output clock toggle rate for Stratix II GX device dedicated clock pins.

Table 4–93. Stratix II GX Maximum Output Clock Rate for Dedicated Clock Pins (Part 1 of 4)					
I/O Standard	**Drive Strength**	**-3 Speed Grade**	**-4 Speed Grade**	**-5 Speed Grade**	**Unit**
LVTTL	4 mA	270	225	210	MHz
	8 mA	435	355	325	MHz
	12 mA	580	475	420	MHz
	16 mA	720	594	520	MHz
	20 mA	875	700	610	MHz
	24 mA *(1)*	1030	794	670	MHz
LVCMOS	4 mA	290	250	230	MHz
	8 mA	565	480	440	MHz
	12 mA	790	710	670	MHz
	16 mA	1020	925	875	MHz
	20 mA	1066	985	935	MHz
	24 mA *(1)*	1100	1040	1000	MHz

Therefore, the DCD percentage for the output clock is from 48.4% to 51.6%.

Table 4–101. Maximum DCD for DDIO Output on Row I/O Pins Without PLL in the Clock Path for -4 and -5 Devices *Note (1)*

Maximum DCD (ps) for Row DDIO Output I/O Standard	Input I/O Standard (No PLL in the Clock Path)					Unit
	TTL/CMOS		SSTL-2	SSTL/HSTL	LVDS	
	3.3/2.5V	1.8/1.5V	2.5V	1.8/1.5V	3.3V	
3.3-V LVTTL	440	495	170	160	105	ps
3.3-V LVCMOS	390	450	120	110	75	ps
2.5 V	375	430	105	95	90	ps
1.8 V	325	385	90	100	135	ps
1.5-V LVCMOS	430	490	160	155	100	ps
SSTL-2 Class I	355	410	85	75	85	ps
SSTL-2 Class II	350	405	80	70	90	ps
SSTL-18 Class I	335	390	65	65	105	ps
1.8-V HSTL Class I	330	385	60	70	110	ps
1.5-V HSTL Class I	330	390	60	70	105	ps
LVDS	180	180	180	180	180	ps

(1) Table 4–101 assumes the input clock has zero DCD.

Table 4–102. Maximum DCD for DDIO Output on Column I/O Pins Without PLL in the Clock Path for -3 Devices (Part 1 of 2) *Note (1)*

Maximum DCD (ps) for DDIO Column Output I/O Standard	Input IO Standard (No PLL in the Clock Path)					Unit
	TTL/CMOS		SSTL-2	SSTL/HSTL	HSTL12	
	3.3/2.5V	1.8/1.5V	2.5V	1.8/1.5V	1.2V	
3.3-V LVTTL	260	380	145	145	145	ps
3.3-V LVCMOS	210	330	100	100	100	ps
2.5 V	195	315	85	85	85	ps
1.8 V	150	265	85	85	85	ps
1.5-V LVCMOS	255	370	140	140	140	ps
SSTL-2 Class I	175	295	65	65	65	ps
SSTL-2 Class II	170	290	60	60	60	ps
SSTL-18 Class I	155	275	55	50	50	ps

Table 4–104. Maximum DCD for DDIO Output on Row I/O Pins With PLL in the Clock Path

Maximum DCD (ps) for Row DDIO Output I/O Standard	Stratix II GX Devices (PLL Output Feeding DDIO)		Unit
	-3 Device	-4 and -5 Device	
3.3-V LVTTL	110	105	ps
3.3-V LVCMOS	65	75	ps
2.5V	75	90	ps
1.8V	85	100	ps
1.5-V LVCMOS	105	100	ps
SSTL-2 Class I	65	75	ps
SSTL-2 Class II	60	70	ps
SSTL-18 Class I	50	65	ps
1.8-V HSTL Class I	50	70	ps
1.5-V HSTL Class I	55	70	ps
LVDS	180	180	ps

Table 4–105. Maximum DCD for DDIO Output on Column I/O Pins With PLL in the Clock Path (Part 1 of 2)

Maximum DCD (ps) for Column DDIO Output I/O Standard	Stratix II GX Devices (PLL Output Feeding DDIO)		Unit
	-3 Device	-4 and -5 Device	
3.3-V LVTTL	145	160	ps
3.3-V LVCMOS	100	110	ps
2.5V	85	95	ps
1.8V	85	100	ps
1.5-V LVCMOS	140	155	ps
SSTL-2 Class I	65	75	ps
SSTL-2 Class II	60	70	ps
SSTL-18 Class I	50	65	ps
SSTL-18 Class II	70	80	ps
1.8-V HSTL Class I	60	70	ps
1.8-V HSTL Class II	60	70	ps
1.5-V HSTL Class I	55	70	ps
1.5-V HSTL Class II	85	100	ps

Table 4–110. Enhanced PLL Specifications (Part 2 of 2)					
Name	**Description**	**Min**	**Typ**	**Max**	**Unit**
f_{VCO}	PLL VCO operating range for –3 and –4 speed grade devices	300		1,040	MHz
	PLL VCO operating range for –5 speed grade devices	300		840	MHz
f_{SS}	Spread-spectrum modulation frequency	100		500	kHz
% spread	Percent down spread for a given clock frequency	0.4	0.5	0.6	%
t_{PLL_PSERR}	Accuracy of PLL phase shift			±30	ps
t_{ARESET}	Minimum pulse width on `areset` signal.	10			ns
$t_{ARESET\_RECONFIG}$	Minimum pulse width on the `areset` signal when using PLL reconfiguration. Reset the PLL after `scandone` goes high.	500			ns
$t_{RECONFIGWAIT}$	The time required for the wait after the reconfiguration is done and the areset is applied.			2	us

(1) This is limited by the I/O f_{MAX}. See Tables 4–91 through 4–95 for the maximum.
(2) If the counter cascading feature of the PLL is utilized, there is no minimum output clock frequency.

Table 4–111. Fast PLL Specifications (Part 1 of 2)					
Name	**Description**	**Min**	**Typ**	**Max**	**Unit**
f_{IN}	Input clock frequency (for -3 and -4 speed grade devices)	16		717	MHz
	Input clock frequency (for -5 speed grade devices)	16		640	MHz
f_{INPFD}	Input frequency to the PFD	16		500	MHz
f_{INDUTY}	Input clock duty cycle	40		60	%
$t_{INJITTER}$	Input clock jitter tolerance in terms of period jitter. Bandwidth ≤2 MHz		0.5		ns (p-p)
	Input clock jitter tolerance in terms of period jitter. Bandwidth > 0.2 MHz		1.0		ns (p-p)

Table 4–111. Fast PLL Specifications (Part 2 of 2)					
Name	**Description**	**Min**	**Typ**	**Max**	**Unit**
f_{VCO}	Upper VCO frequency range for –3 and –4 speed grades	300		1,040	MHz
	Upper VCO frequency range for –5 speed grades	300		840	MHz
	Lower VCO frequency range for –3 and –4 speed grades	150		520	MHz
	Lower VCO frequency range for –5 speed grades	150		420	MHz
f_{OUT}	PLL output frequency to GCLK or RCLK	4.6875		550	MHz
	PLL output frequency to LVDS or DPA clock	150		1,040	MHz
f_{OUT_EXT}	PLL clock output frequency to regular I/O	4.6875		*(1)*	MHz
$t_{CONFIGPLL}$	Time required to reconfigure scan chains for fast PLLs		$75/f_{SCANCLK}$		ns
f_{CLBW}	PLL closed-loop bandwidth	1.16	5	28	MHz
t_{LOCK}	Time required for the PLL to lock from the time it is enabled or the end of the device configuration		0.03	1	ms
t_{PLL_PSERR}	Accuracy of PLL phase shift			±30	ps
t_{ARESET}	Minimum pulse width on areset signal.	10			ns
$t_{ARESET\_RECONFIG}$	Minimum pulse width on the areset signal when using PLL reconfiguration. Reset the PLL after scandone goes high.	500			ns

(1) This is limited by the I/O f_{MAX}. See Tables 4–91 through 4–95 for the maximum.

External Memory Interface Specifications

Tables 4–112 through 4–116 contain Stratix II GX device specifications for the dedicated circuitry used for interfacing with external memory devices.

Table 4–112. DLL Frequency Range Specifications (Part 1 of 2)		
Frequency Mode	**Frequency Range (MHz)**	**Resolution (Degrees)**
0	100 to 175	30
1	150 to 230	22.5
2	200 to 350 (–3 speed grade)	30
	200 to 310 (–4 and –5 speed grade)	30

Table 4–112. DLL Frequency Range Specifications (Part 2 of 2)		
Frequency Mode	**Frequency Range (MHz)**	**Resolution (Degrees)**
3	240 to 400 (–3 speed grade)	36
	240 to 350 (–4 and –5 speed grade)	36

Table 4–113. DQS Jitter Specifications for DLL-Delayed Clock (t_{DQS_JITTER}) Note (1)		
Number of DQS Delay Buffer Stages *(2)*	**Commercial (ps)**	**Industrial (ps)**
1	80	110
2	110	130
3	130	180
4	160	210

(1) Peak-to-peak period jitter on the phase-shifted DQS clock. For example, jitter on two delay stages under commercial conditions is 200 ps peak-to-peak or 100 ps.
(2) Delay stages used for requested DQS phase shift are reported in a project's Compilation Report in the Quartus II software.

Table 4–114. DQS Phase-Shift Error Specifications for DLL-Delayed Clock (t_{DQS_PSERR})			
Number of DQS Delay Buffer Stages *(1)*	**–3 Speed Grade (ps)**	**–4 Speed Grade (ps)**	**–5 Speed Grade (ps)**
1	25	30	35
2	50	60	70
3	75	90	105
4	100	120	140

(1) Delay stages used for request DQS phase shift are reported in a project's Compilation Report in the Quartus II software. For example, phase-shift error on two delay stages under -3 conditions is 50 ps peak-to-peak or 25 ps.

Table 4–118. Document Revision History (Part 3 of 5)		
Date and Document Version	**Changes Made**	**Summary of Changes**
February 2007 v4.2	Added the “Document Revision History” section to this chapter.	Added support information for the Stratix II GX device.
	Updated Table 4–5: ● Removed last three lines ● Removed note 1 ● Added new note 4	
	Deleted table 6-6.	
	Replaced Table 4–6 with all new information.	
	Added Figures 4–1 and 4–2.	
	Added Tables 4–7 through 4–19.	
	Removed Figures 6-1 through 6-4.	
	Updated Table 4–22: ● Changed R_{CONF} information.	
	Updated Table 4–52 ● SSTL-18 Class I, column 1: changed 25 to 50.	
	Updated: ● Table 4–54 ● Table 4–87 ● Table 4–91 ● Table 4–94	
	Updated Tables 4–62 through 4–77	
	Updated Tables 4–79 and 4–80 ● Added “units” column	
	Updated Tables 4–83 through 4–86 ● Changed column title to “Fast Corner Industrial/Commercial”.	
	Updated Table 4–109. ● Added a new line to the bottom of the table.	
August 2006 v4.1	Update Table 6–75, Table 6–84, and Table 6–90.	