Intel - EP2SGX130GF1508C3N Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

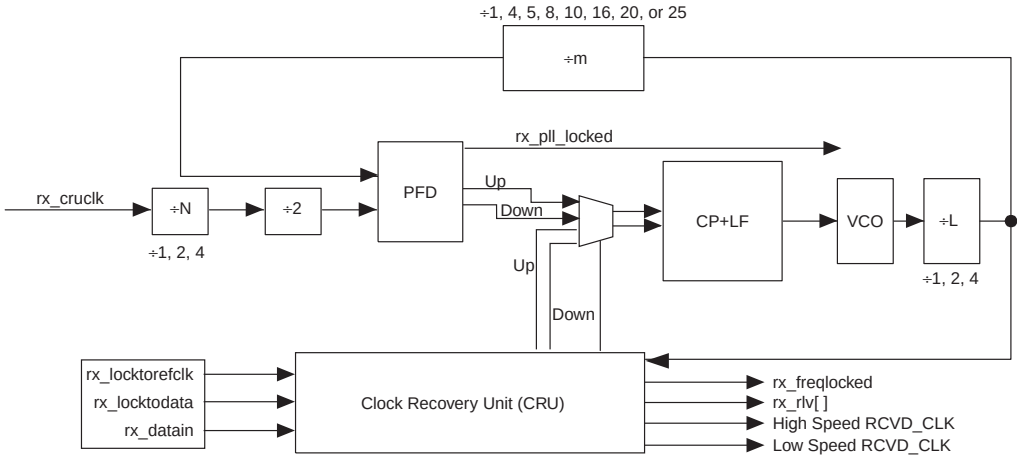
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	6627
Number of Logic Elements/Cells	132540
Total RAM Bits	6747840
Number of I/O	734
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1508-BBGA, FCBGA
Supplier Device Package	1508-FBGA, FC (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2sgx130gf1508c3n

Figure 2–16. Receiver PLL and CRU



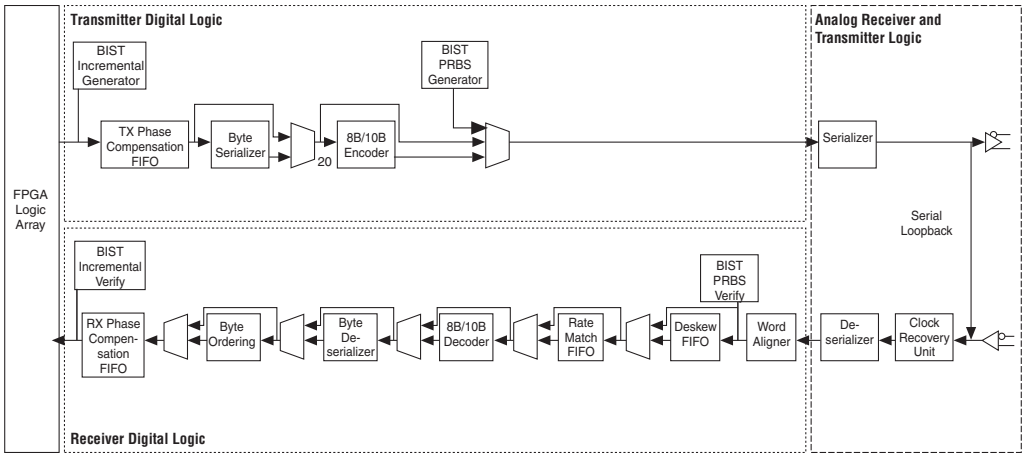
The receiver PLLs and CRUs can support frequencies up to 6.375 Gbps. The input clock frequency is limited to the full clock range of 50 to 622 MHz but only when using `REFCLK0` or `REFCLK1`. An optional `RX_PLL_LOCKED` port is available to indicate whether the PLL is locked to the reference clock. The receiver PLL has a programmable loop bandwidth which can be set to low, medium, or high. The Quartus II software can statically set the loop bandwidth parameter.

All the parameters listed are programmable in the Quartus II software. The receiver PLL has the following features:

- Operates from 600 Mbps to 6.375 Gbps.
- Uses a reference clock between 50 MHz and 622.08 MHz.
- Programmable bandwidth settings: low, medium, and high.
- Programmable `rx_locktorefclk` (forces the receiver PLL to lock to the reference clock) and `rx_locktodata` (forces the receiver PLL to lock to the data).
- The voltage-controlled oscillator (VCO) operates at half rate and has two modes. These modes are for low or high frequency operation and provide optimized phase-noise performance.
- Programmable frequency multiplication *W* of 1, 4, 5, 8, 10, 16, 20, and 25. Not all settings are supported for any particular frequency.
- Two lock indication signals are provided. They are found in PFD mode (lock-to-reference clock), and PD (lock-to-data).

Figure 2–24 shows the data path in serial loopback mode.

Figure 2–24. Stratix II GX Block in Serial Loopback Mode with BIST and PRBS

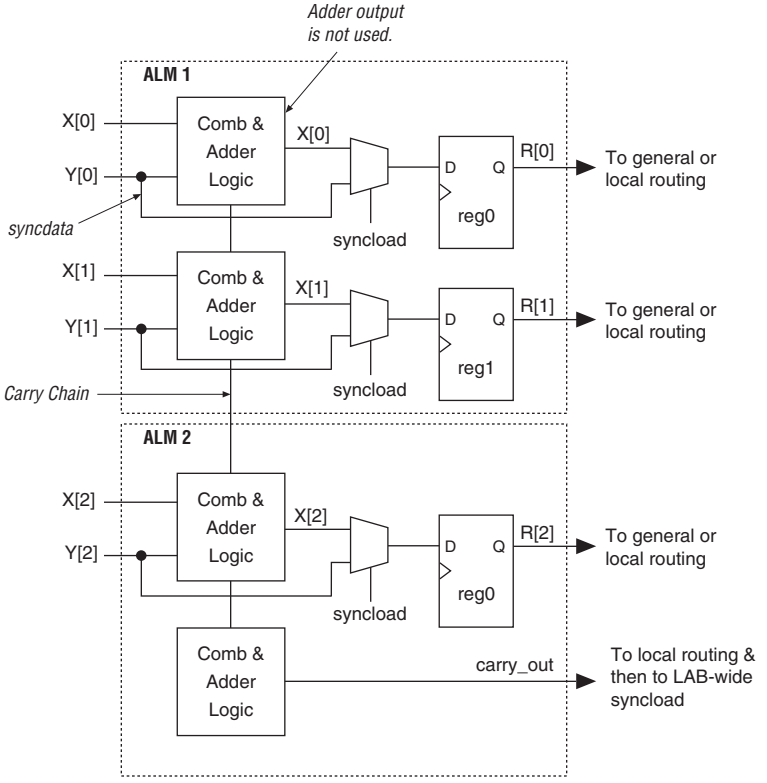


Parallel Loopback

The parallel loopback mode exercises the digital logic portion of the transceiver data path. The analog portions are not used in this loopback path, and the received high-speed serial data is not retimed. This protocol is available as one of the sub-protocols under Basic mode and can be used only for Basic double-width mode.

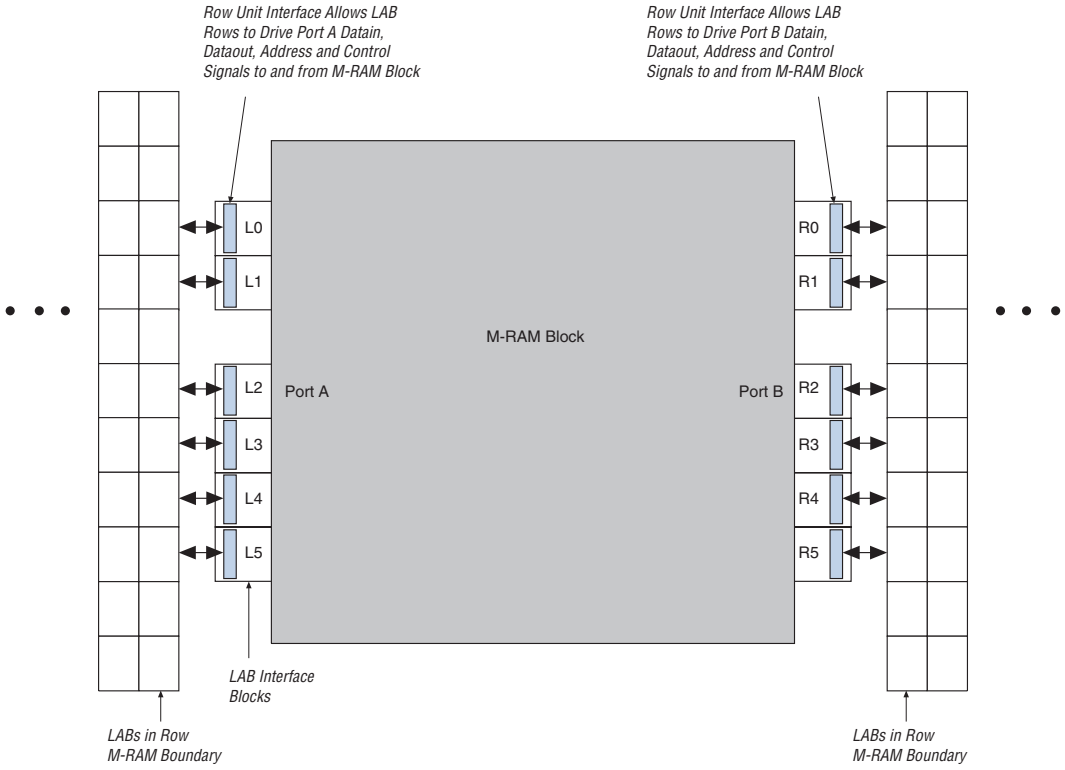
In this loopback mode, the data from the internally available BIST generator is transmitted. The data is looped back after the end of PCS and before the PMA. On the receive side, an internal BIST verifier checks for errors. This loopback enables you to verify the PCS block.

Figure 2–42. Conditional Operation Example



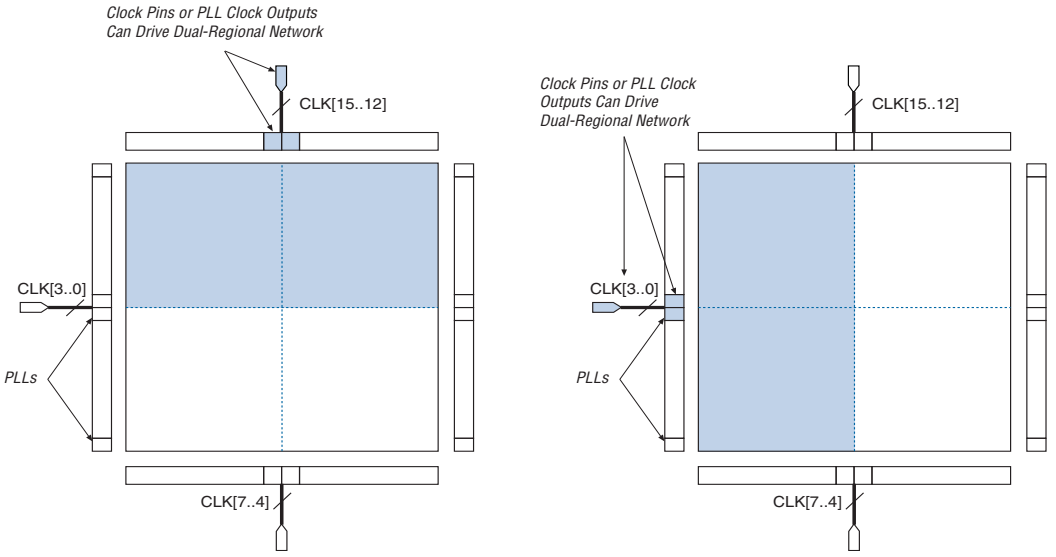
The arithmetic mode also offers clock enable, counter enable, synchronous up and down control, add and subtract control, synchronous clear, synchronous load. The LAB local interconnect data inputs generate the clock enable, counter enable, synchronous up and down and add and subtract control signals. These control signals may be used for the inputs that are shared between the four LUTs in the ALM. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. The Quartus II software automatically places any registers that are not used by the counter into other LABs.

Figure 2–55. M-RAM Block LAB Row Interface *Note (1)*



Note to Figure 2–55:
(1) Only R24 and C16 interconnects cross the M-RAM block boundaries.

Figure 2–63. Dual-Regional Clocks



Combined Resources

Within each quadrant, there are 24 distinct dedicated clocking resources consisting of 16 global clock lines and 8 regional clock lines. Multiplexers are used with these clocks to form buses to drive LAB row clocks, column IOE clocks, or row IOE clocks. Another multiplexer is used at the LAB level to select three of the six row clocks to feed the ALM registers in the LAB (see Figure 2–64).

Figure 2–64. Hierarchical Clock Networks per Quadrant

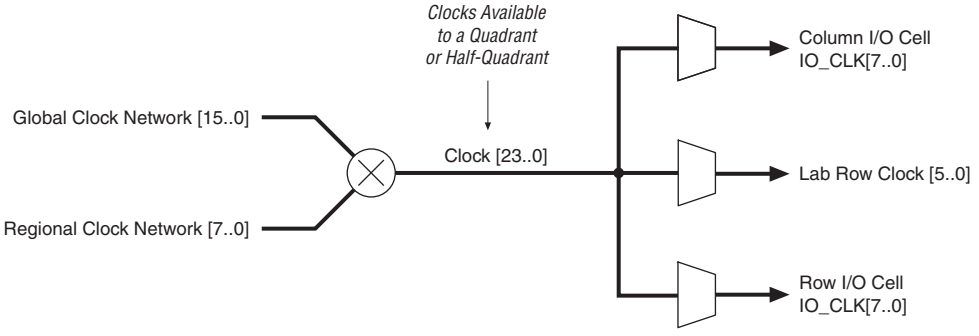
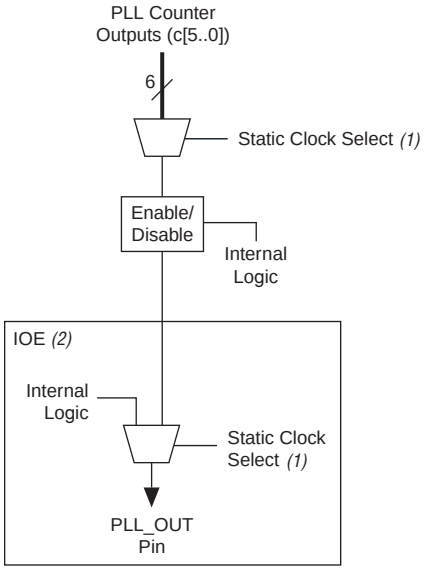


Figure 2–69. External PLL Output Clock Control Blocks



Notes to Figure 2–69:

(1) These clock select signals can only be set through a configuration file (**.sof** or **.pof**) and cannot be dynamically controlled during user mode operation.

(2) The clock control block feeds to a multiplexer within the PLL_OUT pin's IOE. The PLL_OUT pin is a dual-purpose pin. Therefore, this multiplexer selects either an internal signal or the output of the clock control block.

For the global clock control block, the clock source selection can be controlled either statically or dynamically. You have the option of statically selecting the clock source by using the Quartus II software to set specific configuration bits in the configuration file (**.sof** or **.pof**) or you can control the selection dynamically by using internal logic to drive the multiplexer select inputs. When selecting statically, the clock source can be set to any of the inputs to the select multiplexer. When selecting the clock source dynamically, you can either select between two PLL outputs (such as the C0 or C1 outputs from one PLL), between two PLLs (such as the C0/C1 clock output of one PLL or the C0/C1 clock output of the other PLL), between two clock pins (such as CLK0 or CLK1), or between a combination of clock pins or PLL outputs.

For the regional and PLL_OUT clock control block, the clock source selection can only be controlled statically using configuration bits. Any of the inputs to the clock select multiplexer can be set as the clock source.

Table 2–28. Global and Regional Clock Connections from Top Clock Pins and Enhanced PLL Outputs (Part 2 of 2)

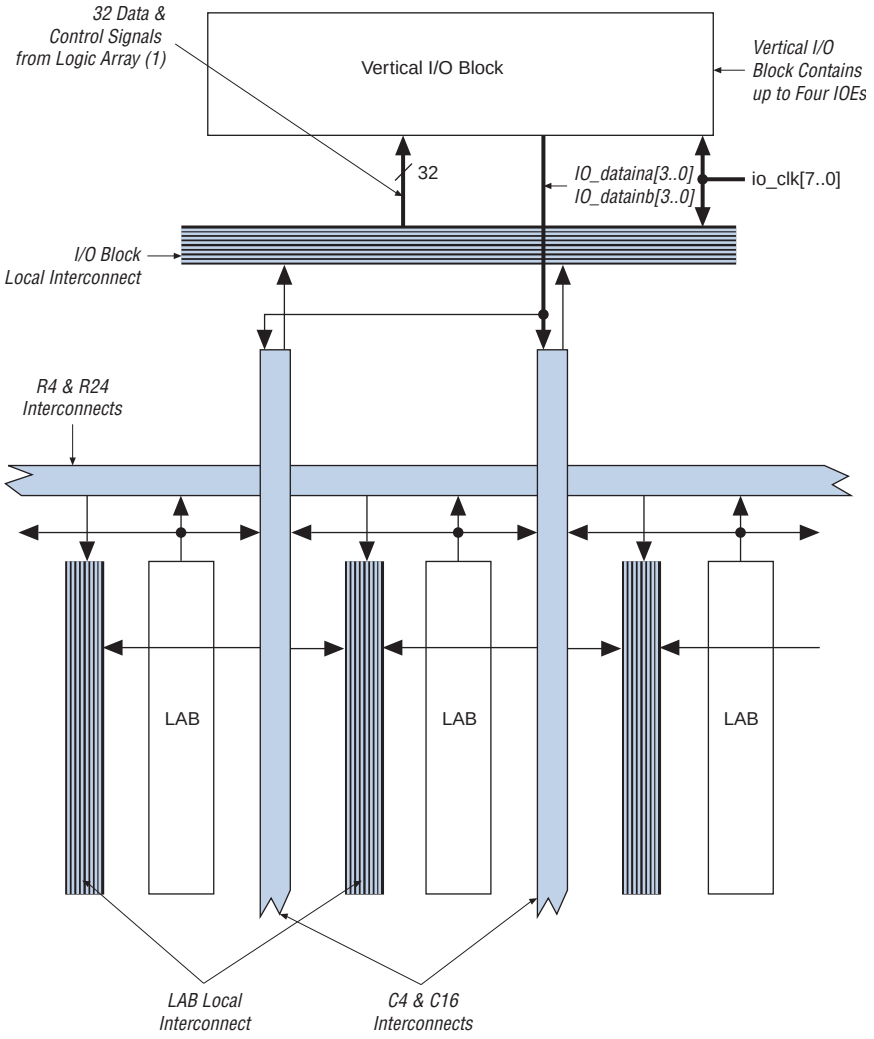
Top Side Global and Regional Clock Network Connectivity	DLLCLK	CLK12	CLK13	CLK14	CLK15	RCLK24	RCLK25	RCLK26	RCLK27	RCLK28	RCLK29	RCLK30	RCLK31
c2	✓			✓	✓			✓				✓	
c3	✓			✓	✓				✓				✓
c4	✓					✓		✓		✓		✓	
c5	✓						✓		✓		✓		✓
Enhanced PLL 11 outputs													
c0		✓	✓			✓				✓			
c1		✓	✓				✓				✓		
c2				✓	✓			✓				✓	
c3				✓	✓				✓				✓
c4						✓		✓		✓		✓	
c5							✓		✓		✓		✓

Table 2–29. Global and Regional Clock Connections from Bottom Clock Pins and Enhanced PLL Outputs (Part 1 of 2)

Bottom Side Global and Regional Clock Network Connectivity	DLLCLK	CLK4	CLK5	CLK6	CLK7	RCLK8	RCLK9	RCLK10	RCLK11	RCLK12	RCLK13	RCLK14	RCLK15
Clock pins													
CLK4p	✓	✓	✓			✓				✓			
CLK5p	✓	✓	✓				✓				✓		
CLK6p	✓			✓	✓			✓				✓	
CLK7p	✓			✓	✓				✓				✓
CLK4n		✓				✓				✓			
CLK5n			✓				✓				✓		
CLK6n				✓				✓				✓	
CLK7n					✓				✓				✓
Drivers from internal logic													
GCLKDRV0		✓											
GCLKDRV1			✓										

Figure 2–78 shows how a column I/O block connects to the logic array.

Figure 2–78. Column I/O Block Connection to the Interconnect



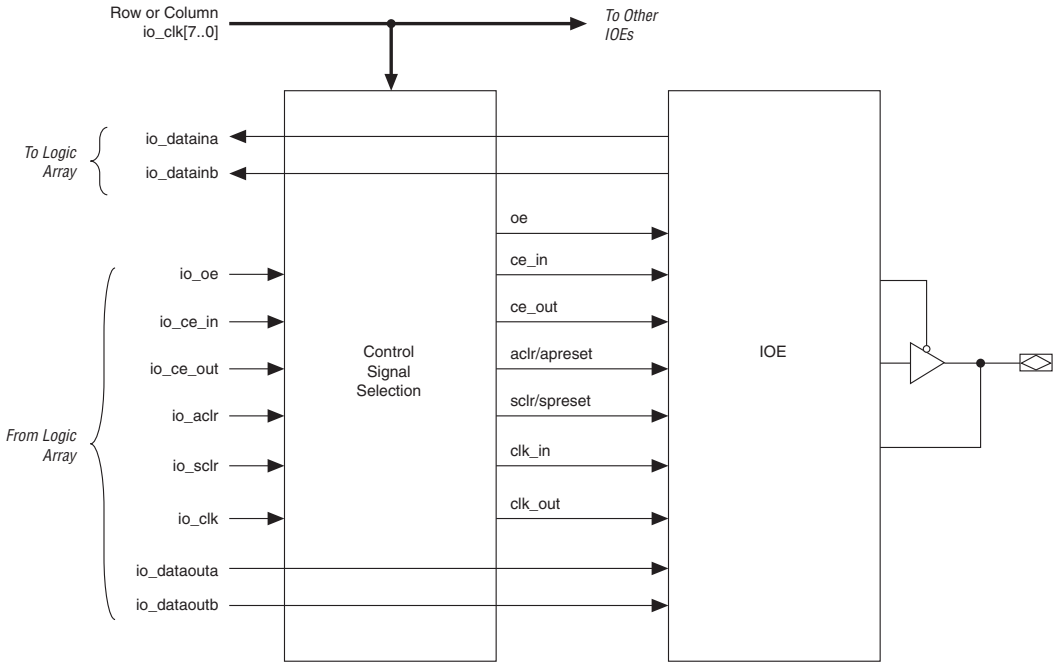
Note to Figure 2–78:

(1) The 32 data and control signals consist of eight data out lines: four lines each for DDR applications `io_dataouta[3..0]` and `io_dataoutb[3..0]`, four output enables `io_oe[3..0]`, four input clock enables `io_ce_in[3..0]`, four output clock enables `io_ce_out[3..0]`, four clocks `io_clk[3..0]`, four asynchronous clear and preset signals `io_aclr/apreset[3..0]`, and four synchronous clear and preset signals `io_sclr/spreset[3..0]`.

There are 32 control and data signals that feed each row or column I/O block. These control and data signals are driven from the logic array. The row or column IOE clocks, `io_clk[7..0]`, provide a dedicated routing resource for low-skew, high-speed clocks. I/O clocks are generated from global or regional clocks. Refer to "PLLs and Clock Networks" on page 2–89 for more information.

Figure 2–79 illustrates the signal paths through the I/O block.

Figure 2–79. Signal Path Through the I/O Block



Each IOE contains its own control signal selection for the following control signals: `oe`, `ce_in`, `ce_out`, `aclr/apreset`, `sclr/spreset`, `clk_in`, and `clk_out`. Figure 2–80 illustrates the control signal selection.

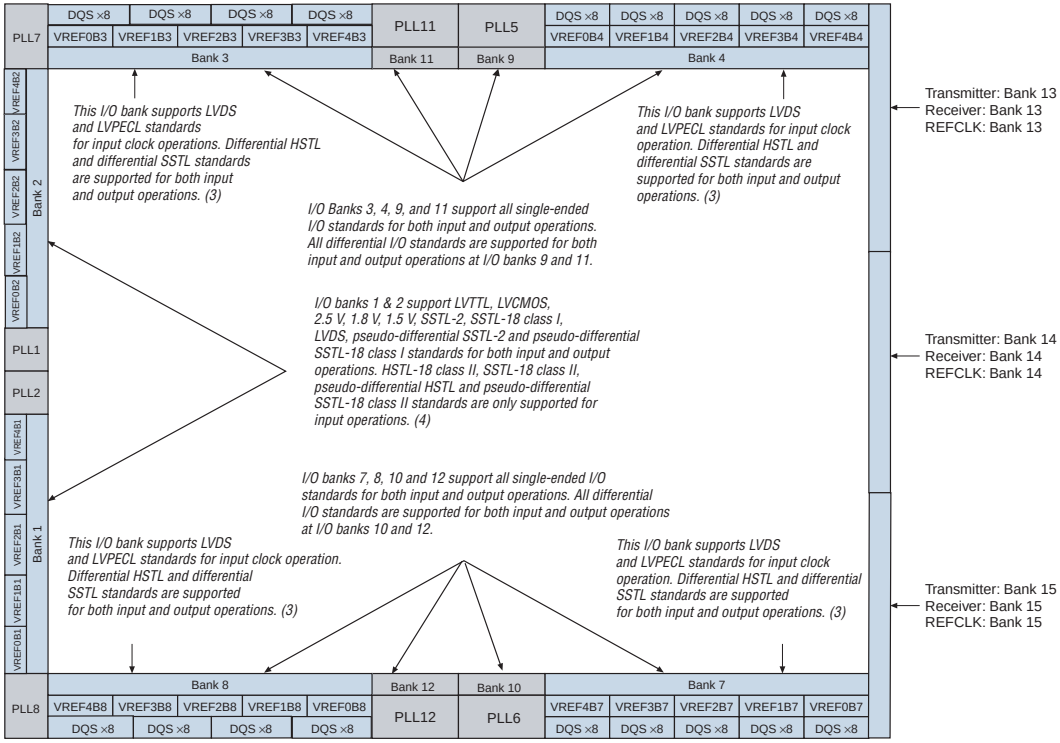
- Differential SSTL-2 class I and II
- 1.2-V HSTL class I and II
- 1.5-V HSTL class I and II
- 1.8-V HSTL class I and II
- SSTL-2 class I and II
- SSTL-18 class I and II

Table 2–33 describes the I/O standards supported by Stratix II GX devices.

Table 2–33. Stratix II GX Supported I/O Standards

I/O Standard	Type	Input Reference Voltage (V_{REF}) (V)	Output Supply Voltage (V_{CCIO}) (V)	Board Termination Voltage (V_{TT}) (V)
LVTTL	Single-ended	—	3.3	—
LVCMOS	Single-ended	—	3.3	—
2.5 V	Single-ended	—	2.5	—
1.8 V	Single-ended	—	1.8	—
1.5-V LVCMOS	Single-ended	—	1.5	—
3.3-V PCI	Single-ended	—	3.3	—
3.3-V PCI-X mode 1	Single-ended	—	3.3	—
LVDS	Differential	—	2.5 *(3)*	—
LVPECL *(1)*	Differential	—	3.3	—
HyperTransport technology	Differential	—	2.5 *(3)*	—
Differential 1.5-V HSTL class I and II *(2)*	Differential	0.75	1.5	0.75
Differential 1.8-V HSTL class I and II *(2)*	Differential	0.90	1.8	0.90
Differential SSTL-18 class I and II *(2)*	Differential	0.90	1.8	0.90
Differential SSTL-2 class I and II *(2)*	Differential	1.25	2.5	1.25
1.2-V HSTL*(4)*	Voltage-referenced	0.6	1.2	0.6
1.5-V HSTL class I and II	Voltage-referenced	0.75	1.5	0.75
1.8-V HSTL class I and II	Voltage-referenced	0.9	1.8	0.9
SSTL-18 class I and II	Voltage-referenced	0.90	1.8	0.90

Figure 2–87. Stratix II GX I/O Banks *Notes (1), (2)*



Notes to Figure 2–87:

(1) Figure 2–87 is a top view of the silicon die that corresponds to a reverse view for flip-chip packages. It is a graphical representation only.

(2) Depending on the size of the device, different device members have different numbers of V_{REF} groups. Refer to the pin list and the Quartus II software for exact locations.

(3) Banks 9 through 12 are enhanced PLL external clock output banks.

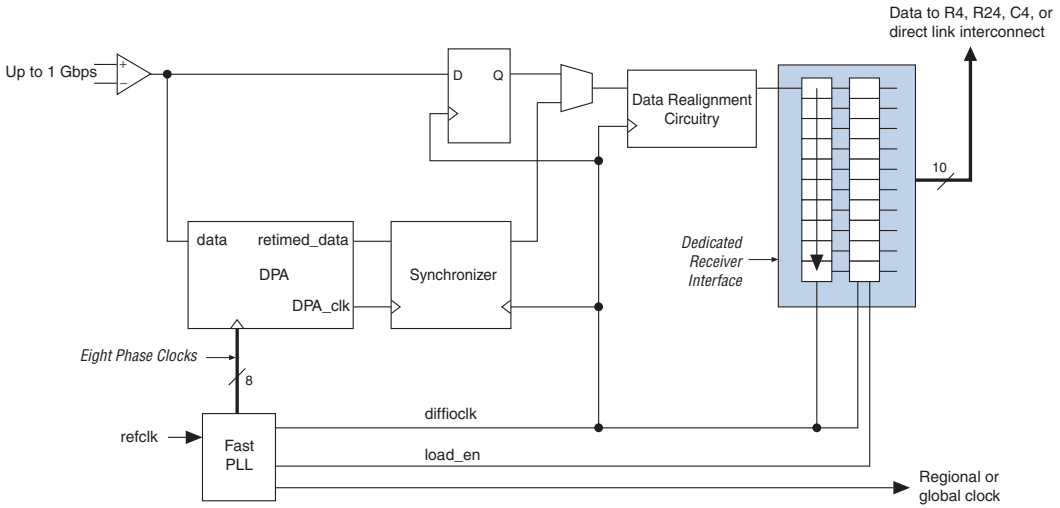
(4) Horizontal I/O banks feature SERDES and DPA circuitry for high-speed differential I/O standards. See the *High-Speed Differential I/O Interfaces with DPA in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook 2* for more information on differential I/O standards.

Each I/O bank has its own VCCIO pins. A single device can support 1.5-, 1.8-, 2.5-, and 3.3-V interfaces; each bank can support a different V_{CCIO} level independently. Each bank also has dedicated VREF pins to support the voltage-referenced standards (such as SSTL-2).

Each I/O bank can support multiple standards with the same V_{CCIO} for input and output pins. Each bank can support one V_{REF} voltage level. For example, when V_{CCIO} is 3.3 V, a bank can support LVTTL, LVCMOS, and 3.3-V PCI for inputs and outputs.

Figure 2–89 shows the block diagram of the Stratix II GX receiver channel.

Figure 2–89. Stratix II GX Receiver Channel



An external pin or global or regional clock can drive the fast PLLs, which can output up to three clocks: two multiplied high-speed clocks to drive the SERDES block and/or external pin, and a low-speed clock to drive the logic array. In addition, eight phase-shifted clocks from the VCO can feed to the DPA circuitry.

For more information on the fast PLL, see the *PLLs in Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Handbook*.

The eight phase-shifted clocks from the fast PLL feed to the DPA block. The DPA block selects the closest phase to the center of the serial data eye to sample the incoming data. This allows the source-synchronous circuitry to capture incoming data correctly regardless of the channel-to-channel or clock-to-channel skew. The DPA block locks to a phase closest to the serial data phase. The phase-aligned DPA clock is used to write the data into the synchronizer.

The synchronizer sits between the DPA block and the data realignment and SERDES circuitry. Since every channel utilizing the DPA block can have a different phase selected to sample the data, the synchronizer is needed to synchronize the data to the high-speed clock domain of the data realignment and the SERDES circuitry.

Table 3–1. Stratix II GX JTAG Instructions

JTAG Instruction	Instruction Code	Description
SAMPLE/PRELOAD	00 0000 0101	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation and permits an initial data pattern to be output at the device pins. Also used by the SignalTap II embedded logic analyzer.
EXTEST *(1)*	00 0000 1111	Allows the external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	11 1111 1111	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	00 0000 0111	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	00 0000 0110	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
HIGHZ *(1)*	00 0000 1011	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins.
CLAMP *(1)*	00 0000 1010	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding the I/O pins to a state defined by the data in the boundary-scan register.
ICR instructions		Used when configuring a Stratix II GX device via the JTAG port with a USB-Blaster™, MasterBlaster™, ByteBlasterMV™, or ByteBlaster II download cable, or when using a **.jam** or **.jbc** via an embedded processor or JRunner.
PULSE_NCONFIG	00 0000 0001	Emulates pulsing the nCONFIG pin low to trigger reconfiguration even though the physical pin is unaffected.
CONFIG_IO *(2)*	00 0000 1101	Allows configuration of I/O standards through the JTAG chain for JTAG testing. Can be executed before, during, or after configuration. Stops configuration if executed during configuration. Once issued, the CONFIG_IO instruction holds nSTATUS low to reset the configuration device. nSTATUS is held low until the IOE configuration register is loaded and the TAP controller state machine transitions to the UPDATE_DR state.
SignalTap II instructions		Monitors internal device operation with the SignalTap II embedded logic analyzer.

Notes to Table 3–1:

(1) Bus hold and weak pull-up resistor features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.

(2) For more information on using the CONFIG_IO instruction, refer to the *MorphIO: An I/O Reconfiguration Solution for Altera Devices White Paper.*

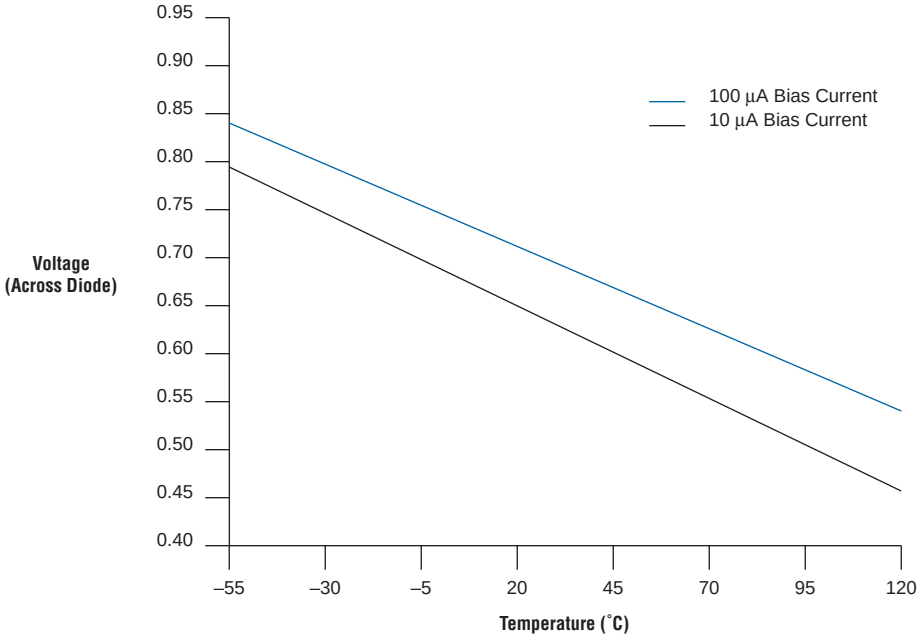
Table 3–5 shows the specifications for bias voltage and current of the Stratix II GX temperature sensing diode.

Table 3–5. Temperature-Sensing Diode Electrical Characteristics

Parameter	Minimum	Typical	Maximum	Unit
IBIAS high	80	100	120	µA
IBIAS low	8	10	12	µA
VBP - VBN	0.3		0.9	V
VBN		0.7		V
Series resistance			3	Ω

The temperature-sensing diode works for the entire operating range shown in Figure 3–2.

Figure 3–2. Temperature Versus Temperature-Sensing Diode Voltage



4. DC and Switching Characteristics

SIIGX51006-4.6

Operating Conditions

Stratix® II GX devices are offered in both commercial and industrial grades. Industrial devices are offered in -4 speed grade and commercial devices are offered in -3 (fastest), -4, and -5 speed grades.

Tables 4–1 through 4–51 provide information on absolute maximum ratings, recommended operating conditions, DC electrical characteristics, and other specifications for Stratix II GX devices.

Absolute Maximum Ratings

Table 4–1 contains the absolute maximum ratings for the Stratix II GX device family.

Table 4–1. Stratix II GX Device Absolute Maximum Ratings *Notes (1), (2), (3)*

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage	With respect to ground	–0.5	1.8	V
V_{CCIO}	Supply voltage	With respect to ground	–0.5	4.6	V
V_{CCPD}	Supply voltage	With respect to ground	–0.5	4.6	V
V_I	DC input voltage *(4)*		–0.5	4.6	V
I_{OUT}	DC output current, per pin		–25	40	mA
T_{STG}	Storage temperature	No bias	–65	150	C
T_J	Junction temperature	BGA packages under bias	–55	125	C

Notes to Table 4–1:

(1) See the *Operating Requirements for Altera Devices Data Sheet* for more information.

(2) Conditions beyond those listed in Table 4–1 may cause permanent damage to a device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse affects on the device.

(3) Supply voltage specifications apply to voltage readings taken at the device pins, not at the power supply.

(4) During transitions, the inputs may overshoot to the voltage shown in Table 4–2 based upon the input duty cycle. The DC case is equivalent to 100% duty cycle. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 12 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
CPRI Transmitter Jitter Generation *(15)*											
Deterministic Jitter (peak-to-peak)	Data Rate = 614.4 Mbps, 1.2288 Gbps, 2.4576 Gbps REFCLK = 61.44 MHz for 614.4 Mbps and 1.2288 Gbps REFCLK = 122.88 MHz for 2.4576 Gbps Pattern = CJPAT Vod = 1400 mV No Pre-emphasis			0.14			0.14			N/A	UI
Total Jitter (peak-to-peak)	Data Rate = 614.4 Mbps, 1.2288 Gbps, 2.4576 Gbps REFCLK = 61.44 MHz for 614.4 Mbps and 1.2288 Gbps REFCLK = 122.88 MHz for 2.4576 Gbps Pattern = CJPAT Vod = 1400 mV No Pre-emphasis			0.279			0.279			N/A	UI

Table 4–54. Timing Measurement Methodology for Input Pins (Part 2 of 2) *Notes (1), (2), (3), (4)*

I/O Standard	Measurement Conditions			Measurement Point
	V_{CCIO} (V)	V_{REF} (V)	Edge Rate (ns)	VMEAS (V)
1.8-V HSTL Class II	1.660	0.830	1.660	0.83
1.5-V HSTL Class I	1.375	0.688	1.375	0.6875
1.5-V HSTL Class II	1.375	0.688	1.375	0.6875
1.2-V HSTL with OCT	1.140	0.570	1.140	0.570
Differential SSTL-2 Class I	2.325	1.163	2.325	1.1625
Differential SSTL-2 Class II	2.325	1.163	2.325	1.1625
Differential SSTL-18 Class I	1.660	0.830	1.660	0.83
Differential SSTL-18 Class II	1.660	0.830	1.660	0.83
1.5-V differential HSTL Class I	1.375	0.688	1.375	0.6875
1.5-V differential HSTL Class II	1.375	0.688	1.375	0.6875
1.8-V differential HSTL Class I	1.660	0.830	1.660	0.83
1.8-V differential HSTL Class II	1.660	0.830	1.660	0.83
LVDS	2.325		0.100	1.1625
LVPECL	3.135		0.100	1.5675

Notes to Table 4–54:

(1) Input buffer sees no load at buffer input.
(2) Input measuring point at buffer input is 0.5 V_{CCIO}.
(3) Output measuring point is 0.5 V_{CC} at internal node.
(4) Input edge rate is 1 V/ns.
(5) Less than 50-mV ripple on V_{CCIO} and V_{CCPD}, V_{CCINT} = 1.15 V with less than 30-mV ripple.
(6) V_{CCPD} = 2.97 V, less than 50-mV ripple on V_{CCIO} and V_{CCPD}, V_{CCINT} = 1.15 V.

Table 4–68. EP2SGX60 Row Pins Global Clock Timing Parameters

Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.494	1.508	2.582	2.875	3.441	ns
t_{COUT}	1.499	1.513	2.578	2.871	3.436	ns
t_{PLLCIN}	-0.183	-0.168	0.116	0.122	0.135	ns
$t_{PLLCOUT}$	-0.178	-0.163	0.112	0.118	0.13	ns

Table 4–69. EP2SGX60 Column Pins Regional Clock Timing Parameters

Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.577	1.591	2.736	3.048	3.648	ns
t_{COUT}	1.412	1.426	2.740	3.052	3.653	ns
t_{PLLCIN}	0.065	0.08	0.334	0.361	0.423	ns
$t_{PLLCOUT}$	-0.1	-0.085	0.334	0.361	0.423	ns

Table 4–70. EP2SGX60 Row Pins Regional Clock Timing Parameters

Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.342	1.355	2.716	3.024	3.622	ns
t_{COUT}	1.347	1.360	2.716	3.024	3.622	ns
t_{PLLCIN}	-0.18	-0.166	0.326	0.352	0.412	ns
$t_{PLLCOUT}$	-0.175	-0.161	0.334	0.361	0.423	ns

Table 4–97. Maximum Output Clock Toggle Rate Derating Factors (Part 4 of 5)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate Derating Factors (ps/pF)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		-3	-4	-5	-3	-4	-5	-3	-4	-5
1.5-V HSTL Class II	16 mA	95	101	101	-	-	-	96	101	101
	18 mA	95	100	100	-	-	-	101	100	100
	20 mA	94	101	101	-	-	-	104	101	101
2.5-V differential SSTL Class II *(3)*	8 mA	364	680	680	-	-	-	350	680	680
	12 mA	163	207	207	-	-	-	188	207	207
	16 mA	118	147	147	-	-	-	94	147	147
	20 mA	99	122	122	-	-	-	87	122	122
	24 mA	91	116	116	-	-	-	85	116	116
1.8-V differential SSTL Class I *(3)*	4 mA	458	570	570	-	-	-	505	570	570
	6 mA	305	380	380	-	-	-	336	380	380
	8 mA	225	282	282	-	-	-	248	282	282
	10 mA	167	220	220	-	-	-	190	220	220
	12 mA	129	175	175	-	-	-	148	175	175
1.8-V differential SSTL Class II *(3)*	8 mA	173	206	206	-	-	-	155	206	206
	16 mA	150	160	160	-	-	-	140	160	160
	18 mA	120	130	130	-	-	-	110	130	130
	20 mA	109	127	127	-	-	-	94	127	127
1.8-V differential HSTL Class I *(3)*	4 mA	245	282	282	-	-	-	229	282	282
	6 mA	164	188	188	-	-	-	153	188	188
	8 mA	123	140	140	-	-	-	114	140	140
	10 mA	110	124	124	-	-	-	108	124	124
	12 mA	97	110	110	-	-	-	104	110	110
1.8-V differential HSTL Class II *(3)*	16 mA	101	104	104	-	-	-	99	104	104
	18 mA	98	102	102	-	-	-	93	102	102
	20 mA	93	99	99	-	-	-	88	99	99
1.5-V differential HSTL Class I *(3)*	4 mA	168	196	196	-	-	-	188	196	196
	6 mA	112	131	131	-	-	-	125	131	131
	8 mA	84	99	99	-	-	-	95	99	99
	10 mA	87	98	98	-	-	-	90	98	98
	12 mA	86	98	98	-	-	-	87	98	98

PLL Timing Specifications

Tables 4–110 and 4–111 describe the Stratix II GX PLL specifications when operating in both the commercial junction temperature range (0 to 85 C) and the industrial junction temperature range (–40 to 100 C), except for the clock switchover and phase-shift stepping features. These two features are only supported from the 0 to 100 C junction temperature range.

Table 4–110. Enhanced PLL Specifications (Part 1 of 2)

Name	Description	Min	Typ	Max	Unit
f_{IN}	Input clock frequency	4		500	MHz
f_{INPFD}	Input frequency to the PFD	4		420	MHz
f_{INDUTY}	Input clock duty cycle	40		60	%
f_{ENDUTY}	External feedback input clock duty cycle	40		60	%
$t_{INJITTER}$	Input or external feedback clock input jitter tolerance in terms of period jitter. Bandwidth ≤0.85 MHz		0.5		ns (peak-to-peak)
	Input or external feedback clock input jitter tolerance in terms of period jitter. Bandwidth > 0.85 MHz		1.0		ns (peak-to-peak)
$t_{OUTJITTER}$	Dedicated clock output period jitter			250 ps for ≥ 100 MHz outclk 25 mUI for < 100 MHz outclk	ps or mUI (p-p)
t_{FCOMP}	External feedback compensation time			10	ns
f_{OUT}	Output frequency for internal global or regional clock	1.5 *(2)*		550	MHz
$f_{OUTDUTY}$	Duty cycle for external clock output	45	50	55	%
$f_{SCANCLK}$	Scanclk frequency			100	MHz
$t_{CONFIGEPLL}$	Time required to reconfigure scan chains for EPLLs		$174/f_{SCANCLK}$		ns
f_{OUT_EXT}	PLL external clock output frequency	1.5 *(2)*		*(1)*	MHz
t_{LOCK}	Time required for the PLL to lock from the time it is enabled or the end of device configuration		0.03	1	ms
t_{DLOCK}	Time required for the PLL to lock dynamically after automatic clock switchover between two identical clock frequencies			1	ms
$f_{SWITCHOVER}$	Frequency range where the clock switchover performs properly	1.5	1	500	MHz
f_{CLBW}	PLL closed-loop bandwidth	0.13	1.2	16.9	MHz