# Intel - EP2SGX130GF1508C4N Datasheet


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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 6627 |
| Number of Logic Elements/Cells | 132540 |
| Total RAM Bits | 6747840 |
| Number of I/O | 734 |
| Number of Gates | - |
| Voltage - Supply | 1.15V ~ 1.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 1508-BBGA, FCBGA |
| Supplier Device Package | 1508-FBGA, FC (40x40) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep2sgx130gf1508c4n |

| Table 1–3. Stratix II GX FineLine BGA Package Sizes | | | |
|---|---|---|---|
| **Dimension** | **780 Pins** | **1,152 Pins** | **1,508 Pins** |
| Pitch (mm) | 1.00 | 1.00 | 1.00 |
| Area ($mm^2$) | 841 | 1,225 | 1,600 |
| Length width (mm × mm) | 29 × 29 | 35 × 35 | 40 × 40 |

## Referenced Document

This chapter references the following document:

- *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*

## Document Revision History

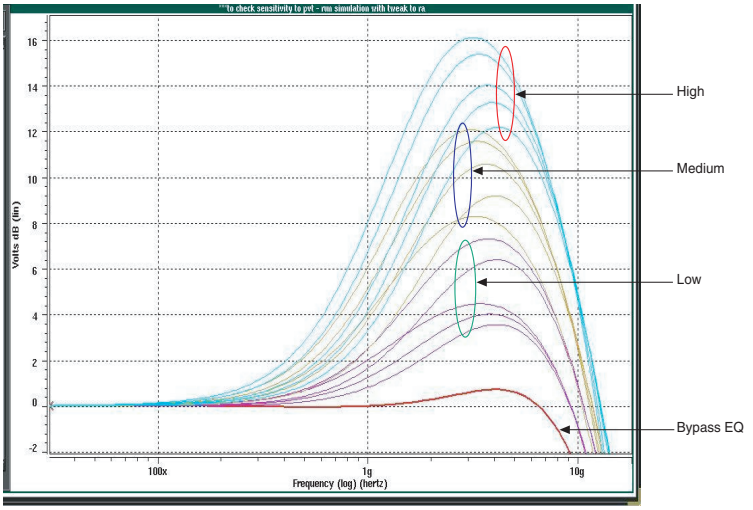
Table 1–4 shows the revision history for this chapter.

| Table 1–4. Document Revision History | | |
|---|---|---|
| **Date and Document Version** | **Changes Made** | **Summary of Changes** |
| October 2007, v1.6 | Updated "Features" section. | |
| | Minor text edits. | |
| August 2007, v1.5 | Added "Referenced Documents" section. | |
| | Minor text edits. | |
| February 2007, v1.4 | • Changed 622 Mbps to 600 Mbps on page 1-2 and Table 1–1.<br>• Deleted "DC coupling" from the Transceiver Block Features list.<br>• Changed 4 to 6 in the PLLs row (columns 3 and 4) of Table 1–1. | |
| | Added the "Document Revision History" section to this chapter. | Added support information for the Stratix II GX device. |
| June 2006, v1.3 | • Updated Table 1–2. | |
| April 2006, v1.2 | • Updated Table 1–1.<br>• Updated Table 1–2. | Updated numbers for receiver channels and user I/O pin counts in Table 1–2. |
| February 2006, v1.1 | • Updated Table 1–1. | |
| October 2005 v1.0 | Added chapter to the *Stratix II GX Device Handbook*. | |

The Stratix II GX receivers also have adaptive equalization capability that adjusts the equalization levels to compensate for changing link characteristics. The adaptive equalization can be powered down dynamically after it selects the appropriate equalization levels.

The receiver equalization circuit is comprised of a programmable amplifier. Each stage is a peaking equalizer with a different center frequency and programmable gain. This allows varying amounts of gain to be applied, depending on the overall frequency response of the channel loss. Channel loss is defined as the summation of all losses through the PCB traces, vias, connectors, and cables present in the physical link. Figure 2–15 shows the frequency response for the 16 programmable settings allowed by the Quartus II software for Stratix II GX devices.

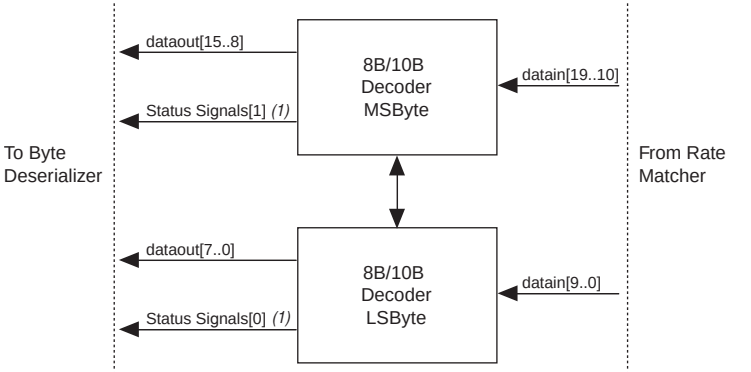
***Figure 2–15. Frequency Response***




## *Receiver PLL and CRU*

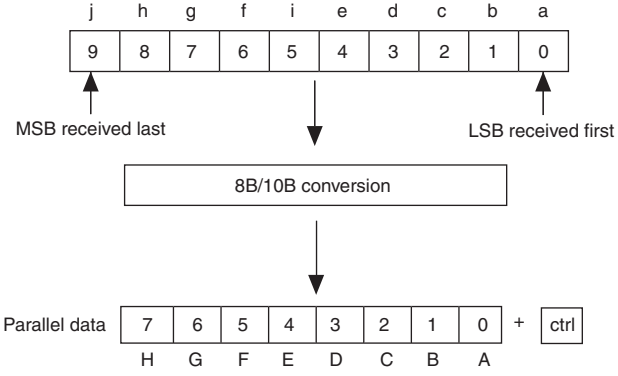
Each transceiver block has four receiver PLLs, lock detectors, signal detectors, run length checkers, and CRU units, each of which is dedicated to a receive channel. If the receive channel associated with a particular receiver PLL or CRU is not used, the receiver PLL and CRU are powered down for the channel. Figure 2–16 shows the receiver PLL and CRU circuits.

*Figure 2–21. 8B/10B Decoder*




The 8B/10B decoder in single-width mode translates the 10-bit encoded data into the 8-bit equivalent data or control code. The 10-bit code received must be from the supported Dx.y or Kx.y list with the proper disparity or error flags asserted. All 8B/10B control signals, such as disparity error or control detect, are pipelined with the data and edge-aligned with the data. Figure 2–22 shows how the 10-bit symbol is decoded in the 8-bit data + 1-bit control indicator.

*Figure 2–22. 8B/10B Decoder Conversion*

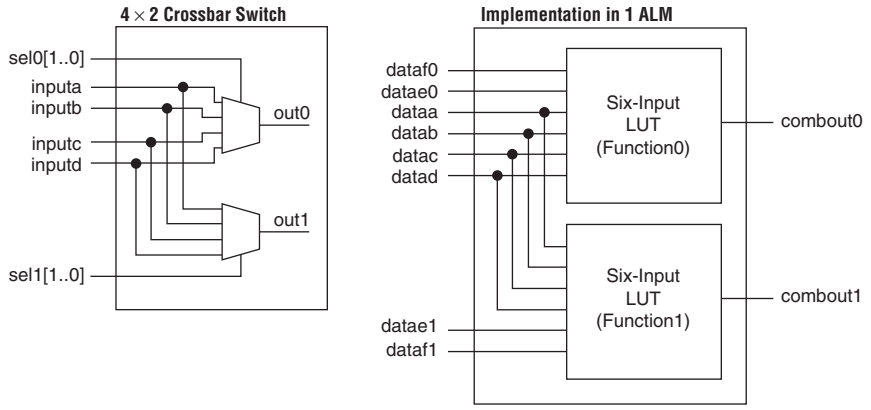



The 8B/10B decoder in double-width mode translates the 20-bit (2 × 10-bits) encoded code into the 16-bit (2 × 8-bits) equivalent data or control code. The 20-bit upper and lower symbols received must be from the supported Dx.y or Kx.y list with the proper disparity or error flags

To pack two five-input functions into one ALM, the functions must have at least two common inputs. The common inputs are dataa and datab. The combination of a four-input function with a five-input function requires one common input (either dataa or datab).

To implement two six-input functions in one ALM, four inputs must be shared and the combinational function must be the same. For example, a 4 × 2 crossbar switch (two 4-to-1 multiplexers with common inputs and unique select lines) can be implemented in one ALM, as shown in Figure 2–38. The shared inputs are dataa, datab, datac, and datad, while the unique select lines are datae0 and dataf0 for function0, and datae1 and dataf1 for function1. This crossbar switch consumes four LUTs in a four-input LUT-based architecture.

*Figure 2–38. 4 × 2 Crossbar Switch Example*




In a sparsely used device, functions that could be placed into one ALM can be implemented in separate ALMs. The Quartus II Compiler spreads a design out to achieve the best possible performance. As a device begins to fill up, the Quartus II software automatically utilizes the full potential of the Stratix II GX ALM. The Quartus II Compiler automatically searches for functions of common inputs or completely independent functions to be placed into one ALM and to make efficient use of the device resources. In addition, you can manually control resource usage by setting location assignments. Any six-input function can be implemented utilizing inputs dataa, datab, datac, datad, and either datae0 and dataf0 or datae1 and dataf1. If datae0 and dataf0 are utilized, the output is driven to register0, and/or register0 is bypassed and the data drives out to the interconnect using the top set of output drivers (see Figure 2–39). If datae1 and dataf1 are utilized, the output drives to register1 and/or bypasses register1 and drives to the interconnect

### *Carry Chain*

The carry chain provides a fast carry function between the dedicated adders in arithmetic or shared arithmetic mode. Carry chains can begin in either the first ALM or the fifth ALM in a LAB. The final carry-out signal is routed to an ALM, where it is fed to local, row, or column interconnects.

The Quartus II Compiler automatically creates carry chain logic during compilation, or you can create it manually during design entry. Parameterized functions, such as LPM functions, automatically take advantage of carry chains for the appropriate functions. The Quartus II Compiler creates carry chains longer than 16 (8 ALMs in arithmetic or shared arithmetic mode) by linking LABs together automatically. For enhanced fitting, a long carry chain runs vertically, allowing fast horizontal connections to TriMatrix memory and DSP blocks. A carry chain can continue as far as a full column. To avoid routing congestion in one small area of the device when a high fan-in arithmetic function is implemented, the LAB can support carry chains that only utilize either the top half or the bottom half of the LAB before connecting to the next LAB. The other half of the ALMs in the LAB is available for implementing narrower fan-in functions in normal mode. Carry chains that use the top four ALMs in the first LAB will carry into the top half of the ALMs in the next LAB within the column. Carry chains that use the bottom four ALMs in the first LAB will carry into the bottom half of the ALMs in the next LAB within the column. Every other column of the LABs are top-half bypassable, while the other LAB columns are bottom-half bypassable. Refer to "MultiTrack Interconnect" on page 2–63 for more information on carry chain interconnect.

## Shared Arithmetic Mode

In shared arithmetic mode, the ALM can implement a three-input add. In this mode, the ALM is configured with four 4-input LUTs. Each LUT either computes the sum of three inputs or the carry of three inputs. The output of the carry computation is fed to the next adder (either to `adder1` in the same ALM or to `adder0` of the next ALM in the LAB) using a dedicated connection called the shared arithmetic chain. This shared arithmetic chain can significantly improve the performance of an adder tree by reducing the number of summation stages required to implement an adder tree. Figure 2–43 shows the ALM in shared arithmetic mode.

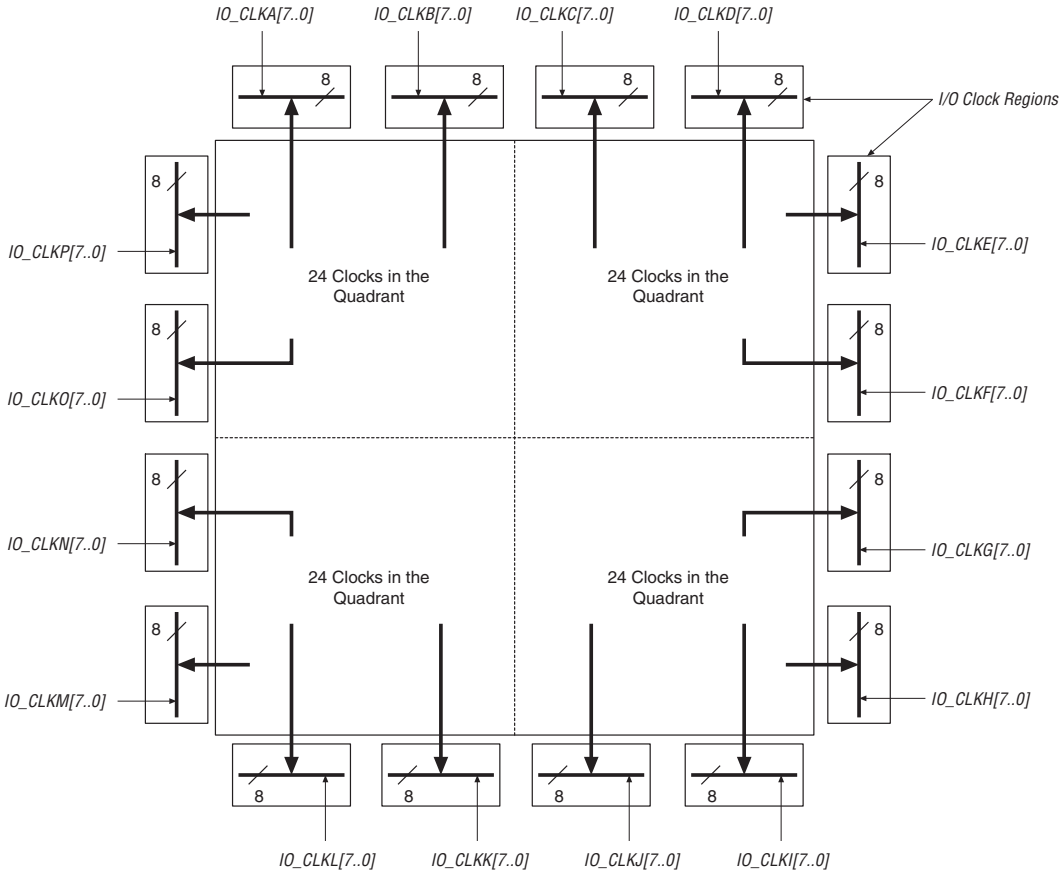
C16 column interconnects span a length of 16 LABs and provide the fastest resource for long column connections between LABs, TriMatrix memory blocks, DSP blocks, and IOEs. C16 interconnects can cross M-RAM blocks and also drive to row and column interconnects at every fourth LAB. C16 interconnects drive LAB local interconnects via C4 and R4 interconnects and do not drive LAB local interconnects directly. All embedded blocks communicate with the logic array similar to LAB-to-LAB interfaces. Each block (that is, TriMatrix memory and DSP blocks) connects to row and column interconnects and has local interconnect regions driven by row and column interconnects. These blocks also have direct link interconnects for fast connections to and from a neighboring LAB. All blocks are fed by the row LAB clocks, `labclk[5..0]`.

Table 2–18 shows the Stratix II GX device's routing scheme.

*Table 2–18. Stratix II GX Device Routing Scheme (Part 1 of 2)*

| Source | Destination | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Shared Arithmetic Chain | Carry Chain | Register Chain | Local Interconnect | Direct Link Interconnect | R4 Interconnect | R24 Interconnect | C4 Interconnect | C16 Interconnect | ALM | M512 RAM Block | M4K RAM Block | M-RAM Block | DSP Blocks | Column IOE | Row IOE |
| Shared arithmetic chain | | | | | | | | | | ✓ | | | | | | |
| Carry chain | | | | | | | | | | ✓ | | | | | | |
| Register chain | | | | | | | | | | ✓ | | | | | | |
| Local interconnect | | | | | | | | | | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Direct link interconnect | | | | ✓ | | | | | | | | | | | | |
| R4 interconnect | | | | ✓ | | ✓ | ✓ | ✓ | ✓ | | | | | | | |
| R24 interconnect | | | | | | ✓ | ✓ | ✓ | ✓ | | | | | | | |
| C4 interconnect | | | | ✓ | | ✓ | | ✓ | | | | | | | | |
| C16 interconnect | | | | | | ✓ | ✓ | ✓ | ✓ | | | | | | | |
| ALM | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | ✓ | | | | | | | | |
| M512 RAM block | | | | ✓ | ✓ | ✓ | | ✓ | | | | | | | | |
| M4K RAM block | | | | ✓ | ✓ | ✓ | | ✓ | | | | | | | | |
| M-RAM block | | | | | ✓ | ✓ | ✓ | ✓ | | | | | | | | |
| DSP blocks | | | | | ✓ | ✓ | | ✓ | | | | | | | | |

*Figure 2–66. EP2SGX60, EP2SGX90 and EP2SGX130 Device I/O Clock Groups*



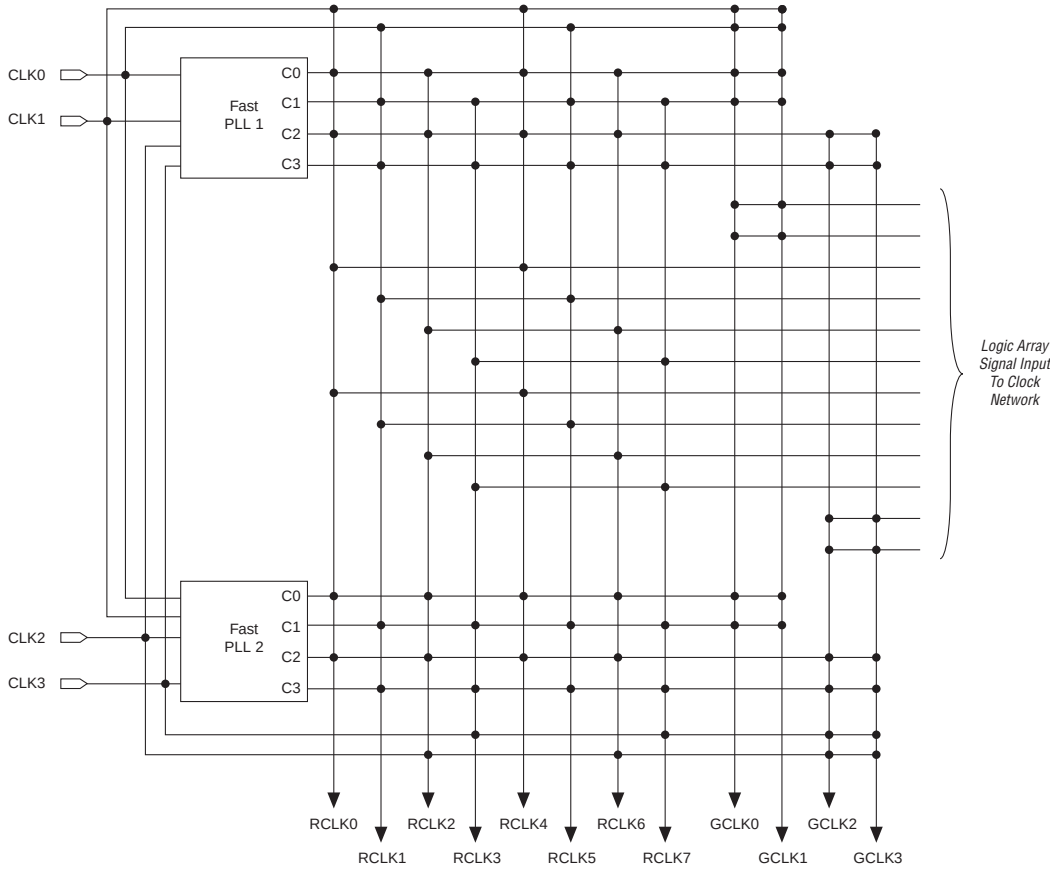

You can use the Quartus II software to control whether a clock input pin drives either a global, regional, or dual-regional clock network. The Quartus II software automatically selects the clocking resources if not specified.

### *Clock Control Block*

Each global clock, regional clock, and PLL external clock output has its own clock control block. The control block has two functions:

- Clock source selection (dynamic selection for global clocks)
- Clock power-down (dynamic clock enable or disable)

*Figure 2–71. Global and Regional Clock Connections from Center Clock Pins and Fast PLL Outputs Notes (1), (2)*




*Notes to Figure 2–71:*

(1) EP2SGX30C/D and P2SGX60C/D devices only have two fast PLLs (1 and 2) and two Enhanced PLLs (5 and 6), but the connectivity from these PLLs to the global and regional clock networks remains the same as shown.

(2) The global or regional clocks in a fast PLL's quadrant can drive the fast PLL input. A dedicated clock input pin or other PLL must drive the global or regional source. The source cannot be driven by internally generated logic before driving the fast PLL.

## On-Chip Termination

Stratix II GX devices provide differential (for the LVDS technology I/O standard) and series on-chip termination to reduce reflections and maintain signal integrity. On-chip termination simplifies board design by minimizing the number of external termination resistors required. Termination can be placed inside the package, eliminating small stubs that can still lead to reflections.

Stratix II GX devices provide four types of termination:

- Differential termination ($R_D$)
- Series termination ($R_S$) without calibration
- Series termination ($R_S$) with calibration
- Parallel termination ($R_T$) with calibration

Table 2–34 shows the Stratix II GX on-chip termination support per I/O bank.

*Table 2–34. On-Chip Termination Support by I/O Banks (Part 1 of 2)*

| On-Chip Termination Support | I/O Standard Support | Top and Bottom Banks (3, 4, 7, 8) | Left Bank (1, 2) |
|---|---|---|---|
| Series termination without calibration | 3.3-V LVTTL | ✓ | ✓ |
| | 3.3-V LVCMOS | ✓ | ✓ |
| | 2.5-V LVTTL | ✓ | ✓ |
| | 2.5-V LVCMOS | ✓ | ✓ |
| | 1.8-V LVTTL | ✓ | ✓ |
| | 1.8-V LVCMOS | ✓ | ✓ |
| | 1.5-V LVTTL | ✓ | ✓ |
| | 1.5-V LVCMOS | ✓ | ✓ |
| | SSTL-2 class I and II | ✓ | ✓ |
| | SSTL-18 class I | ✓ | ✓ |
| | SSTL-18 class II | ✓ | — |
| | 1.8-V HSTL class I | ✓ | ✓ |
| | 1.8-V HSTL class II | ✓ | — |
| | 1.5-V HSTL class I | ✓ | ✓ |
| | 1.2-V HSTL | ✓ | — |

### *On-Chip Parallel Termination with Calibration*

Stratix II GX devices support on-chip parallel termination with calibration for column I/O pins only. There is one calibration circuit for the top I/O banks and one circuit for the bottom I/O banks. Each on-chip parallel termination calibration circuit compares the total impedance of each I/O buffer to the external 50-Ω resistors connected to the RUP and RDN pins and dynamically enables or disables the transistors until they match. Calibration occurs at the end of device configuration. Once the calibration circuit finds the correct impedance, it powers down and stops changing the characteristics of the drivers.

On-chip parallel termination with calibration is only supported for input pins.

For more information about on-chip termination supported by Stratix II devices, refer to the *Selectable I/O Standards in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook*.

For more information about tolerance specifications for on-chip termination with calibration, refer to the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II GX Device Handbook.*

## MultiVolt I/O Interface

The Stratix II GX architecture supports the MultiVolt I/O interface feature that allows Stratix II GX devices in all packages to interface with systems of different supply voltages. The Stratix II GX VCCINT pins must always be connected to a 1.2-V power supply. With a 1.2-V $V_{CCINT}$ level, input pins are 1.2-, 1.5-, 1.8-, 2.5-, and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.2-, 1.5-, 1.8-, 2.5-, or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (for example, when VCCIO pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems). The Stratix II GX VCCPD power pins must be connected to a 3.3-V power supply. These power pins are used to supply the pre-driver power to the output buffers, which increases the performance of the output pins. The VCCPD pins also power configuration input pins and JTAG input pins.

*Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 5 of 19)*

| Symbol/ Description | Conditions | -3 Speed Commercial Speed Grade | | | -4 Speed Commercial and Industrial Speed Grade | | | -5 Speed Commercial Speed Grade | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Peak-to-peak jitter | Jitter frequency = 22.1 KHz | | > 8.5 | | | > 8.5 | | | > 8.5 | | UI |
| Peak-to-peak jitter | Jitter frequency = 1.875 MHz | | > 0.1 | | | > 0.1 | | | > 0.1 | | UI |
| Peak-to-peak jitter | Jitter frequency = 20 MHz | | > 0.1 | | | > 0.1 | | | > 0.1 | | UI |
| **PCI Express Transmit Jitter Generation** *(10)* | | | | | | | | | | | |
| Total jitter at 2.5 Gbps | Compliance pattern $V_{OD}$ = 800 mV Pre-emphasis (1st post-tap) = Setting 5 | - | - | 0.25 | - | - | 0.25 | - | - | 0.25 | UI |
| **PCI Express Receiver Jitter Tolerance** *(10)* | | | | | | | | | | | |
| Total jitter at 2.5 Gbps | Compliance pattern No Equalization DC gain = 3 dB | | > 0.6 | | | > 0.6 | | | > 0.6 | | UI |
| **Serial RapidIO Transmit Jitter Generation** *(11)* | | | | | | | | | | | |
| Deterministic Jitter (peak-to-peak) | Data Rate = 1.25, 2.5, 3.125 Gbps REFCLK = 125 MHz Pattern = CJPAT $V_{OD}$ = 800 mV No Pre-emphasis | - | - | 0.17 | - | - | 0.17 | - | - | 0.17 | UI |
| Total Jitter (peak-to-peak) | Data Rate = 1.25, 2.5, 3.125 Gbps REFCLK = 125 MHz Pattern = CJPAT $V_{OD}$ = 800 mV No Pre-emphasis | - | - | 0.35 | - | - | 0.35 | - | - | 0.35 | UI |

*Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 6 of 19)*

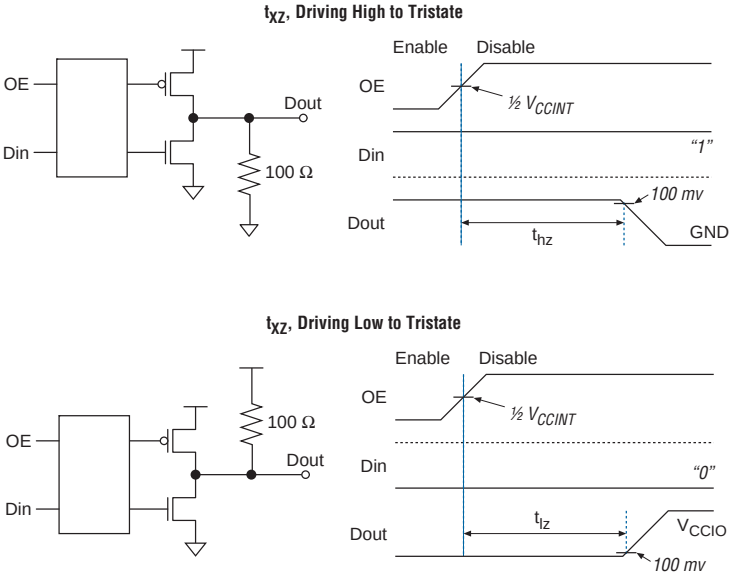
| Symbol/ Description | Conditions | -3 Speed Commercial Speed Grade | | | -4 Speed Commercial and Industrial Speed Grade | | | -5 Speed Commercial Speed Grade | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| **Serial RapidIO Receiver Jitter Tolerance** *(11)* | | | | | | | | | | | |
| Deterministic Jitter Tolerance (peak-to-peak) | Data Rate = 1.25, 2.5, 3.125 Gbps<br>REFCLK = 125 MHz<br>Pattern = CJPAT<br>Equalizer Setting = 0 for 1.25 Gbps<br>Equalizer Setting = 6 for 2.5 Gbps<br>Equalizer Setting = 6 for 3.125 Gbps | > 0.37 | | | > 0.37 | | | > 0.37 | | | UI |
| Combined Deterministic and Random Jitter Tolerance (peak-to-peak) | Data Rate = 1.25, 2.5, 3.125 Gbps<br>REFCLK = 125 MHz<br>Pattern = CJPAT<br>Equalizer Setting = 0 for 1.25 Gbps<br>Equalizer Setting = 6 for 2.5 Gbps<br>Equalizer Setting = 6 for 3.125 Gbps | > 0.55 | | | > 0.55 | | | > 0.55 | | | UI |

*Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 13 of 19)*

| Symbol/ Description | Conditions | -3 Speed Commercial Speed Grade | | | -4 Speed Commercial and Industrial Speed Grade | | | -5 Speed Commercial Speed Grade | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| **CPRI Receiver Jitter Tolerance** *(15)* | | | | | | | | | | | |
| Deterministic Jitter Tolerance (peak-to-peak) | Data Rate = 614.4 Mbps, 1.2288 Gbps, 2.4576 Gbps<br>REFCLK = 61.44 MHz for 614.4 Mbps<br>REFCLK = 122.88 MHz for 1.2288 Gbps and 2.4576 Gbps<br>Pattern = CJPAT<br>Equalizer Setting = 6<br>DC Gain = 0 dB | | > 0.4 | | | > 0.4 | | | N/A | | UI |
| Combined Deterministic and Random Jitter Tolerance (peak-to-peak) | Data Rate = 614.4 Mbps, 1.2288 Gbps, 2.4576 Gbps<br>REFCLK = 61.44 MHz for 614.4 Mbps<br>REFCLK = 122.88 MHz for 1.2288 Gbps and 2.4576 Gbps<br>Pattern = CJPAT<br>Equalizer Setting = 6<br>DC Gain = 0 dB | | > 0.66 | | | > 0.66 | | | N/A | | UI |

Figures 4–9 and 4–10 show the measurement setup for output disable and output enable timing.

***Figure 4–9. Measurement Setup for $t_{xz}$*** *Note (1)*




***Note to Figure 4–9:***

(1) $V_{CCINT}$ is 1.12 V for this measurement.

*Table 4–59. M512 Block Internal Timing Microparameters (Part 1 of 2)*

| Symbol | Parameter | -3 Speed Grade (2) | | -3 Speed Grade (3) | | -4 Speed Grade | | -5 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{M512RC}$ | Synchronous read cycle time | 2089 | 2318 | 2089 | 2433 | 2089 | 2587 | 2089 | 3104 | ps |
| $t_{M512WERESU}$ | Write or read enable setup time before clock | 22 | | 23 | | 24 | | 29 | | ps |
| $t_{M512WEREH}$ | Write or read enable hold time after clock | 203 | | 213 | | 226 | | 272 | | ps |
| $t_{M512DATASU}$ | Data setup time before clock | 22 | | 23 | | 24 | | 29 | | ps |
| $t_{M512DATAH}$ | Data hold time after clock | 203 | | 213 | | 226 | | 272 | | ps |
| $t_{M512WADDRSU}$ | Write address setup time before clock | 22 | | 23 | | 24 | | 29 | | ps |
| $t_{M512WADDRH}$ | Write address hold time after clock | 203 | | 213 | | 226 | | 272 | | ps |
| $t_{M512RADDRSU}$ | Read address setup time before clock | 22 | | 23 | | 24 | | 29 | | ps |
| $t_{M512RADDRH}$ | Read address hold time after clock | 203 | | 213 | | 226 | | 272 | | ps |
| $t_{M512DATACO1}$ | Clock-to-output delay when using output registers | 298 | 478 | 298 | 501 | 298 | 533 | 298 | 640 | ps |
| $t_{M512DATACO2}$ | Clock-to-output delay without output registers | 2102 | 2345 | 2102 | 2461 | 2102 | 2616 | 2102 | 3141 | ps |
| $t_{M512CLKL}$ | Minimum clock low time | 1315 | | 1380 | | 1468 | | 1762 | | ps |
| $t_{M512CLKH}$ | Minimum clock high time | 1315 | | 1380 | | 1468 | | 1762 | | ps |

| Table 4–86. Stratix II GX I/O Output Delay for Column Pins (Part 1 of 7) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| I/O Standard | Drive Strength | Parameter | Fast Corner Industrial/ Commercial | -3 Speed Grade *(3)* | -3 Speed Grade *(4)* | -4 Speed Grade | -5 Speed Grade | Unit |
| LVTTL | 4 mA | $t_{OP}$ | 1236 | 2351 | 2467 | 2624 | 2820 | ps |
| | | $t_{DIP}$ | 1258 | 2417 | 2537 | 2698 | 2910 | ps |
| | 8 mA | $t_{OP}$ | 1091 | 2036 | 2136 | 2272 | 2448 | ps |
| | | $t_{DIP}$ | 1113 | 2102 | 2206 | 2346 | 2538 | ps |
| | 12 mA | $t_{OP}$ | 1024 | 2036 | 2136 | 2272 | 2448 | ps |
| | | $t_{DIP}$ | 1046 | 2102 | 2206 | 2346 | 2538 | ps |
| | 16 mA | $t_{OP}$ | 998 | 1893 | 1986 | 2112 | 2279 | ps |
| | | $t_{DIP}$ | 1020 | 1959 | 2056 | 2186 | 2369 | ps |
| | 20 mA | $t_{OP}$ | 976 | 1787 | 1875 | 1994 | 2154 | ps |
| | | $t_{DIP}$ | 998 | 1853 | 1945 | 2068 | 2244 | ps |
| | 24 mA *(1)* | $t_{OP}$ | 969 | 1788 | 1876 | 1995 | 2156 | ps |
| | | $t_{DIP}$ | 991 | 1854 | 1946 | 2069 | 2246 | ps |
| LVCMOS | 4 mA | $t_{OP}$ | 1091 | 2036 | 2136 | 2272 | 2448 | ps |
| | | $t_{DIP}$ | 1113 | 2102 | 2206 | 2346 | 2538 | ps |
| | 8 mA | $t_{OP}$ | 999 | 1786 | 1874 | 1993 | 2153 | ps |
| | | $t_{DIP}$ | 1021 | 1852 | 1944 | 2067 | 2243 | ps |
| | 12 mA | $t_{OP}$ | 971 | 1720 | 1805 | 1919 | 2075 | ps |
| | | $t_{DIP}$ | 993 | 1786 | 1875 | 1993 | 2165 | ps |
| | 16 mA | $t_{OP}$ | 978 | 1693 | 1776 | 1889 | 2043 | ps |
| | | $t_{DIP}$ | 1000 | 1759 | 1846 | 1963 | 2133 | ps |
| | 20 mA | $t_{OP}$ | 965 | 1677 | 1759 | 1871 | 2025 | ps |
| | | $t_{DIP}$ | 987 | 1743 | 1829 | 1945 | 2115 | ps |
| | 24 mA *(1)* | $t_{OP}$ | 954 | 1659 | 1741 | 1851 | 2003 | ps |
| | | $t_{DIP}$ | 976 | 1725 | 1811 | 1925 | 2093 | ps |

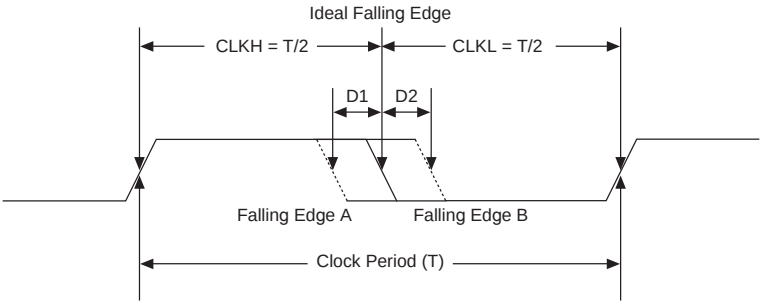
*Table 4–87. Stratix II GX I/O Output Delay for Row Pins (Part 3 of 4)*

| I/O Standard | Drive Strength | Parameter | Fast Corner Industrial/ Commercial | -3 Speed Grade *(3)* | -3 Speed Grade *(4)* | -4 Speed Grade | -5 Speed Grade | Unit |
|---|---|---|---|---|---|---|---|---|
| SSTL-18 Class I | 4 mA | $t_{OP}$ | 1038 | 1709 | 1793 | 1906 | 2046 | ps |
| | | $t_{DIP}$ | 995 | 1654 | 1736 | 1846 | 1973 | ps |
| | 6 mA | $t_{OP}$ | 1042 | 1648 | 1729 | 1838 | 1975 | ps |
| | | $t_{DIP}$ | 999 | 1593 | 1672 | 1778 | 1902 | ps |
| | 8 mA | $t_{OP}$ | 1018 | 1633 | 1713 | 1821 | 1958 | ps |
| | | $t_{DIP}$ | 975 | 1578 | 1656 | 1761 | 1885 | ps |
| | 10 mA *(1)* | $t_{OP}$ | 1021 | 1615 | 1694 | 1801 | 1937 | ps |
| | | $t_{DIP}$ | 978 | 1560 | 1637 | 1741 | 1864 | ps |
| 1.8-V HSTL Class I | 4 mA | $t_{OP}$ | 1019 | 1610 | 1689 | 1795 | 1956 | ps |
| | | $t_{DIP}$ | 976 | 1555 | 1632 | 1735 | 1883 | ps |
| | 6 mA | $t_{OP}$ | 1022 | 1580 | 1658 | 1762 | 1920 | ps |
| | | $t_{DIP}$ | 979 | 1525 | 1601 | 1702 | 1847 | ps |
| | 8 mA | $t_{OP}$ | 1004 | 1576 | 1653 | 1757 | 1916 | ps |
| | | $t_{DIP}$ | 961 | 1521 | 1596 | 1697 | 1843 | ps |
| | 10 mA | $t_{OP}$ | 1008 | 1567 | 1644 | 1747 | 1905 | ps |
| | | $t_{DIP}$ | 965 | 1512 | 1587 | 1687 | 1832 | ps |
| | 12 mA *(1)* | $t_{OP}$ | 999 | 1566 | 1643 | 1746 | 1904 | ps |
| | | $t_{DIP}$ | 956 | 1511 | 1586 | 1686 | 1831 | ps |
| 1.5-V HSTL Class I | 4 mA | $t_{OP}$ | 1018 | 1591 | 1669 | 1774 | 1933 | ps |
| | | $t_{DIP}$ | 975 | 1536 | 1612 | 1714 | 1860 | ps |
| | 6 mA | $t_{OP}$ | 1021 | 1579 | 1657 | 1761 | 1919 | ps |
| | | $t_{DIP}$ | 978 | 1524 | 1600 | 1701 | 1846 | ps |
| | 8 mA *(1)* | $t_{OP}$ | 1006 | 1572 | 1649 | 1753 | 1911 | ps |
| | | $t_{DIP}$ | 963 | 1517 | 1592 | 1693 | 1838 | ps |
| Differential SSTL-2 Class I | 8 mA | $t_{OP}$ | 1050 | 1759 | 1846 | 1962 | 2104 | ps |
| | | $t_{DIP}$ | 1007 | 1704 | 1789 | 1902 | 2031 | ps |
| | 12 mA | $t_{OP}$ | 1026 | 1694 | 1777 | 1889 | 2028 | ps |
| | | $t_{DIP}$ | 983 | 1639 | 1720 | 1829 | 1955 | ps |
| Differential SSTL-2 Class II | 16 mA | $t_{OP}$ | 992 | 1581 | 1659 | 1763 | 1897 | ps |
| | | $t_{DIP}$ | 949 | 1526 | 1602 | 1703 | 1824 | ps |

## Duty Cycle Distortion

Duty cycle distortion (DCD) describes how much the falling edge of a clock is off from its ideal position. The ideal position is when both the clock high time (CLKH) and the clock low time (CLKL) equal half of the clock period (T), as shown in Figure 4–11. DCD is the deviation of the non-ideal falling edge from the ideal falling edge, such as D1 for the falling edge A and D2 for the falling edge B (see Figure 4–11). The maximum DCD for a clock is the larger value of D1 and D2.

***Figure 4–11. Duty Cycle Distortion***




DCD expressed in absolution derivation, for example, D1 or D2 in Figure 4–11, is clock-period independent. DCD can also be expressed as a percentage, and the percentage number is clock-period dependent. DCD as a percentage is defined as:

(T/2 – D1) / T (the low percentage boundary)

(T/2 + D2) / T (the high percentage boundary)

### DCD Measurement Techniques

DCD is measured at an FPGA output pin driven by registers inside the corresponding I/O element (IOE) block. When the output is a single data rate signal (non-DDIO), only one edge of the register input clock (positive or negative) triggers output transitions (Figure 4–12). Therefore, any DCD present on the input clock signal or caused by the clock input buffer or different input I/O standard does not transfer to the output signal.

| Table 4–110. Enhanced PLL Specifications (Part 2 of 2) | | | | | |
|---|---|---|---|---|---|
| **Name** | **Description** | **Min** | **Typ** | **Max** | **Unit** |
| $f_{VCO}$ | PLL VCO operating range for –3 and –4 speed grade devices | 300 | | 1,040 | MHz |
| | PLL VCO operating range for –5 speed grade devices | 300 | | 840 | MHz |
| $f_{SS}$ | Spread-spectrum modulation frequency | 100 | | 500 | kHz |
| % spread | Percent down spread for a given clock frequency | 0.4 | 0.5 | 0.6 | % |
| $t_{PLL\_PSERR}$ | Accuracy of PLL phase shift | | | ±30 | ps |
| $t_{ARESET}$ | Minimum pulse width on `areset` signal. | 10 | | | ns |
| $t_{ARESET\_RECONFIG}$ | Minimum pulse width on the `areset` signal when using PLL reconfiguration. Reset the PLL after `scandone` goes high. | 500 | | | ns |
| $t_{RECONFIGWAIT}$ | The time required for the wait after the reconfiguration is done and the areset is applied. | | | 2 | us |

(1) This is limited by the I/O $f_{MAX}$. See Tables 4–91 through 4–95 for the maximum.
(2) If the counter cascading feature of the PLL is utilized, there is no minimum output clock frequency.

| Table 4–111. Fast PLL Specifications (Part 1 of 2) | | | | | |
|---|---|---|---|---|---|
| **Name** | **Description** | **Min** | **Typ** | **Max** | **Unit** |
| $f_{IN}$ | Input clock frequency (for -3 and -4 speed grade devices) | 16 | | 717 | MHz |
| | Input clock frequency (for -5 speed grade devices) | 16 | | 640 | MHz |
| $f_{INPFD}$ | Input frequency to the PFD | 16 | | 500 | MHz |
| $f_{INDUTY}$ | Input clock duty cycle | 40 | | 60 | % |
| $t_{INJITTER}$ | Input clock jitter tolerance in terms of period jitter. Bandwidth ≤2 MHz | | 0.5 | | ns (p-p) |
| | Input clock jitter tolerance in terms of period jitter. Bandwidth > 0.2 MHz | | 1.0 | | ns (p-p) |

*Table 4–118. Document Revision History (Part 4 of 5)*

| Date and Document Version | Changes Made | Summary of Changes |
|---|---|---|
| June 2006, v4.0 | • Updated Table 6–5.<br>• Updated Table 6–6.<br>• Updated all values in Table 6–7.<br>• Added Tables 6–8 and 6–9.<br>• Added Figures 6–1 through 6–4.<br>• Updated Table 6–18.<br>• Updated Tables 6–85 through 6–96.<br>• Added Table 6–80, Stratix II GX Maximum Output Clock Rate for Dedicated Clock Pins.<br>• Updated Table 6–100.<br>• In "I/O Timing Measurement Methodology" section, updated Table 6–42.<br>• In "Internal Timing Parameters" section, updated Tables 6–43 through 6–48.<br>• In "Stratix II GX Clock Timing Parameters" section, updated Tables 6–50 through 6–65.<br>• In "IOE Programmable Delay" section, updated Tables 6–67 and 6–68.<br>• In "I/O Delays" section, updated Tables 6–71 through 6–74.<br>• In "Maximum Input & Output Clock Toggle Rate" section, updated Tables 6–75 through 6–83.<br>• In "DCD Measurement Techniques" section, updated Tables 6–85 through 6–92.<br>• In "High-Speed I/O Specifications" section, updated Tables 6–94 through 6–96.<br>• In "External Memory Interface Specifications" section, updated Table 6–100. | • Removed rows for $V_{ID}$, $V_{OD}$, $V_{ICM}$, and $V_{OCM}$ from Table 6–5.<br>• Updated values for rx, tx, and `refclkb` in Table 6–6.<br>• Removed table containing 1.2-V PCML I/O information. That information is in Table 6–7.<br>• Added values to Table 6–100. |