# Intel - EP2SGX130GF1508I4N Datasheet


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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

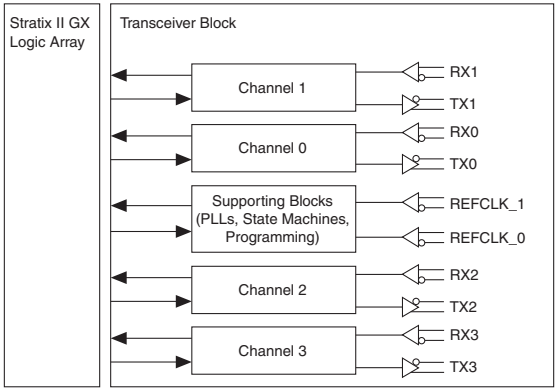
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 6627 |
| Number of Logic Elements/Cells | 132540 |
| Total RAM Bits | 6747840 |
| Number of I/O | 734 |
| Number of Gates | - |
| Voltage - Supply | 1.15V ~ 1.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 1508-BBGA, FCBGA |
| Supplier Device Package | 1508-FBGA, FC (40x40) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep2sgx130gf1508i4n |

*Figure 2–2. Elements of the Transceiver Block*




Each Stratix II GX transceiver channel consists of a transmitter and receiver. The transceivers are grouped in four and share PLL resources. Each transmitter has access to one of two PLLs. The transmitter contains the following:

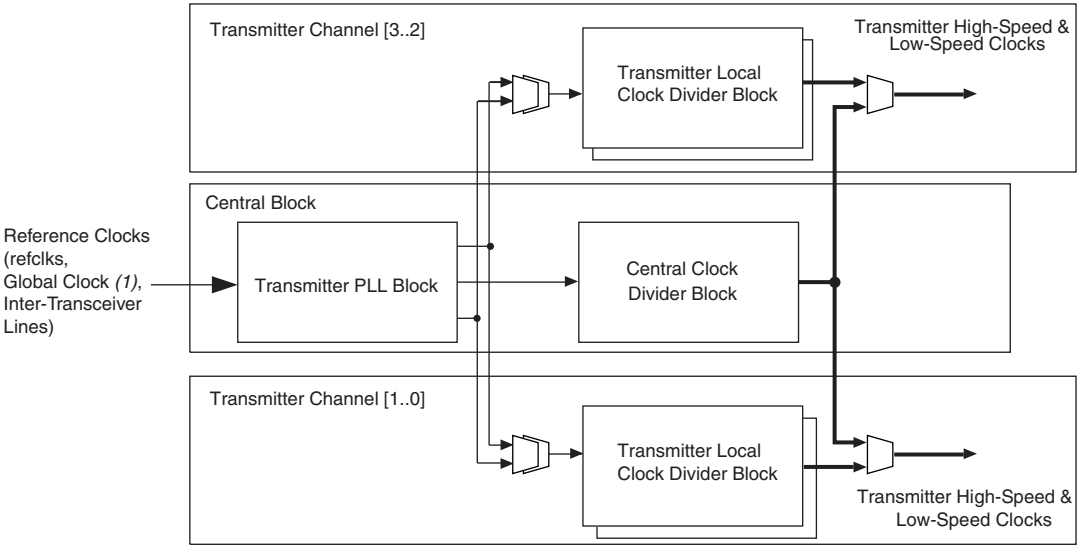
- Transmitter phase compensation first-in first-out (FIFO) buffer
- Byte serializer (optional)
- 8B/10B encoder (optional)
- Serializer (parallel-to-serial converter)
- Transmitter differential output buffer

The receiver contains the following:

- Receiver differential input buffer
- Receiver lock detector and run length checker
- Clock recovery unit (CRU)
- Deserializer
- Pattern detector
- Word aligner
- Lane deskew
- Rate matcher (optional)
- 8B/10B decoder (optional)
- Byte deserializer (optional)
- Byte ordering
- Receiver phase compensation FIFO buffer

Designers can preset Stratix II GX transceiver functions using the Quartus® II software. In addition, pre-emphasis, equalization, and differential output voltage ($V_{OD}$) are dynamically programmable. Each Stratix II GX transceiver channel supports various loopback modes and is

*Figure 2–3. Clock Distribution for the Transmitters Note (1)*




*Note to Figure 2–3:*
(1) The global clock line must be driven by an input pin.

The transmitter PLLs in each transceiver block clock the PMA and PCS circuitry in the transmit path. The Quartus II software automatically powers down the transmitter PLLs that are not used in the design. Figure 2–4 is a block diagram of the transmitter PLL.

The transmitter phase/frequency detector references the clock from one of the following sources:

- Reference clocks
- Reference clock from the adjacent transceiver block
- Inter-transceiver block clock lines
- Global clock line driven by input pin

Two reference clocks, `REFCLK0` and `REFCLK1`, are available per transceiver block. The inter-transceiver block bus allows multiple transceivers to use the same reference clocks. Each transceiver block has one outgoing reference clock which connects to one inter-transceiver block line. The incoming reference clock can be selected from five inter-transceiver block lines `IQ[4..0]` or from the global clock line that is driven by an input pin.

### *Transmit State Machine*

The transmit state machine operates in either PCI Express mode, XAUI mode, or GIGE mode, depending on the protocol used. The state machine is not utilized for certain protocols, such as SONET.

**GIGE Mode**

In GIGE mode, the transmit state machine converts all idle ordered sets (/K28.5/, /Dx.y/) to either /I1/ or /I2/ ordered sets. /I1/ consists of a negative-ending disparity /K28.5/ (denoted by /K28.5/-) followed by a neutral /D5.6/. /I2/ consists of a positive-ending disparity /K28.5/ (denoted by /K28.5/+) and a negative-ending disparity /D16.2/ (denoted by /D16.2/-). The transmit state machines do not convert any of the ordered sets to match /C1/ or /C2/, which are the configuration ordered sets. (/C1/ and /C2/ are defined by [/K28.5/, /D21.5/] and [/K28.5/, /D2.2/], respectively). Both the /I1/ and /I2/ ordered sets guarantee a negative-ending disparity after each ordered set.

**XAUI Mode**

The transmit state machine translates the XAUI XGMII code group to the XAUI PCS code group. Table 2–5 shows the code conversion.

*Table 2–5. Code Conversion*

| XGMII TXC | XGMII TXD | PCS Code-Group | Description |
|---|---|---|---|
| 0 | 00 through FF | Dxx.y | Normal data |
| 1 | 07 | K28.0 or K28.3 or K28.5 | Idle in ||**I**|| |
| 1 | 07 | K28.5 | Idle in ||**T**|| |
| 1 | 9C | K28.4 | Sequence |
| 1 | FB | K27.7 | Start |
| 1 | FD | K29.7 | Terminate |
| 1 | FE | K30.7 | Error |
| 1 | See IEEE 802.3 reserved code groups | See IEEE 802.3 reserved code groups | Reserved code groups |
| 1 | Other value | K30.7 | Invalid XGMII character |

The XAUI PCS idle code groups, /K28.0/ (/R/) and /K28.5/ (/K/), are automatically randomized based on a PRBS7 pattern with an $x^7 + x^6 + 1$ polynomial. The /K28.3/ (/A/) code group is automatically generated between 16 and 31 idle code groups. The idle randomization on the /A/, /K/, and /R/ code groups is done automatically by the transmit state machine.

When the FIFO pointers initialize, the receiver domain clock must remain phase locked to receiver FPGA clock.

After resetting the receiver FIFO buffer, writing to the receiver FIFO buffer begins and continues on each parallel clock. The phase compensation FIFO buffer is eight words deep for PIPE mode and four words deep for all other modes.

## Loopback Modes

The Stratix II GX transceiver has built-in loopback modes for debugging and testing. The loopback modes are configured in the Stratix II GX ALT2GXB megafunction in the Quartus II software. The available loopback modes are:

- Serial loopback
- Parallel loopback
- Reverse serial loopback
- Reverse serial loopback (pre-CDR)
- PCI Express PIPE reverse parallel loopback (available only in PIPE mode)

### *Serial Loopback*

The serial loopback mode exercises all the transceiver logic, except for the input buffer. Serial loopback is available for all non-PIPE modes. The loopback function is dynamically enabled through the `rx_seriallpbken` port on a channel-by-channel basis.

In serial loopback mode, the data on the transmit side is sent by the PLD. A separate mode is available in the ALT2GXB megafunction under Basic protocol mode, in which PRBS data is generated and verified internally in the transceiver. The PRBS patterns available in this mode are shown in Table 2–10.

Table 2–10 shows the BIST data output and verifier alignment pattern.

*Table 2–10. BIST Data Output and Verifier Alignment Pattern*

| Pattern | Polynomial | Parallel Data Width | | | |
|---|---|---|---|---|---|
| | | 8-Bit | 10-Bit | 16-Bit | 20-Bit |
| PRBS-7 | ×7 + ×6 + 1 | | | | ✓ |
| PRBS-10 | ×10 + ×7 + 1 | | ✓ | | |

allowing fast horizontal connections to TriMatrix memory and DSP blocks. A shared arithmetic chain can continue as far as a full column. Similar to the carry chains, the shared arithmetic chains are also top- or bottom-half bypassable. This capability allows the shared arithmetic chain to cascade through half of the ALMs in a LAB while leaving the other half available for narrower fan-in functionality. Every other LAB column is top-half bypassable, while the other LAB columns are bottom-half bypassable. Refer to "MultiTrack Interconnect" on page 2–63 for more information on shared arithmetic chain interconnect.

## Register Chain

In addition to the general routing outputs, the ALMs in a LAB have register chain outputs. The register chain routing allows registers in the same LAB to be cascaded together. The register chain interconnect allows a LAB to use LUTs for a single combinational function and the registers to be used for an unrelated shift register implementation. These resources speed up connections between ALMs while saving local interconnect resources (see Figure 2–45). The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. See "MultiTrack Interconnect" on page 2–63 for more information about register chain interconnect.

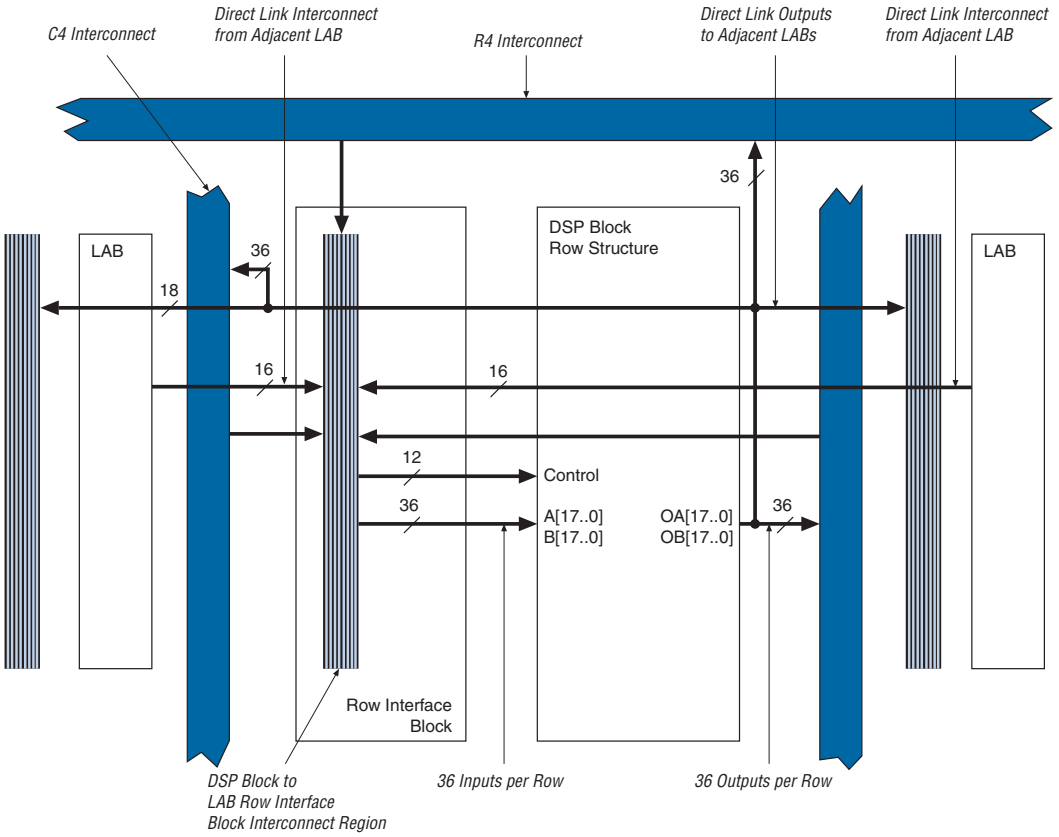
R24 row interconnects span 24 LABs and provide the fastest resource for long row connections between LABs, TriMatrix memory, DSP blocks, and Row IOEs. The R24 row interconnects can cross M-RAM blocks. R24 row interconnects drive to other row or column interconnects at every fourth LAB and do not drive directly to LAB local interconnects. R24 row interconnects drive LAB local interconnects via R4 and C4 interconnects. R24 interconnects can drive R24, R4, C16, and C4 interconnects. The column interconnect operates similarly to the row interconnect and vertically routes signals to and from LABs, TriMatrix memory, DSP blocks, and IOEs. Each column of LABs is served by a dedicated column interconnect.

These column resources include:

- Shared arithmetic chain interconnects in a LAB
- Carry chain interconnects in a LAB and from LAB to LAB
- Register chain interconnects in a LAB
- C4 interconnects traversing a distance of four blocks in an up and down direction
- C16 column interconnects for high-speed vertical routing through the device

Stratix II GX devices include an enhanced interconnect structure in LABs for routing shared arithmetic chains and carry chains for efficient arithmetic functions. The register chain connection allows the register output of one ALM to connect directly to the register input of the next ALM in the LAB for fast shift registers. These ALM-to-ALM connections bypass the local interconnect. The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. Figure 2–47 shows the shared arithmetic chain, carry chain, and register chain interconnects.

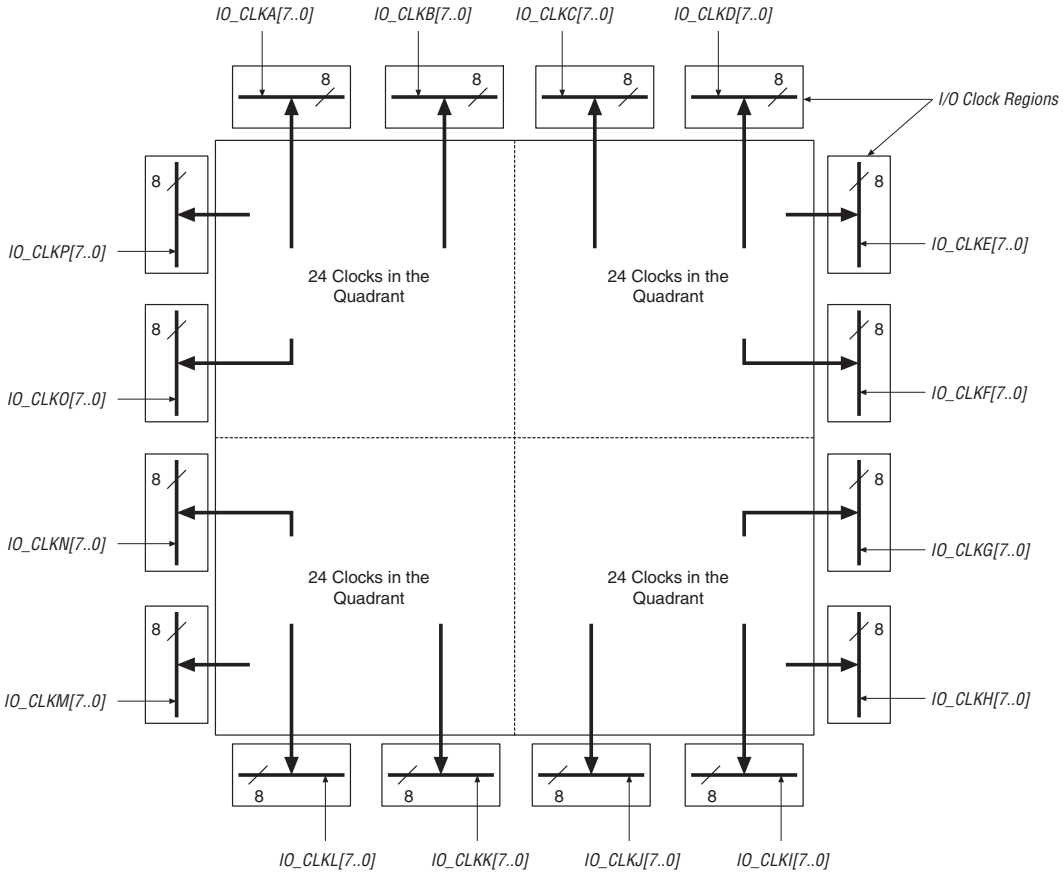
*Figure 2–60. DSP Block Interface to Interconnect*




A bus of 44 control signals feeds the entire DSP block. These signals include clocks, asynchronous clears, clock enables, signed and unsigned control signals, addition and subtraction control signals, rounding and saturation control signals, and accumulator synchronous loads. The clock signals are routed from LAB row clocks and are generated from specific LAB rows at the DSP block interface. The LAB row source for control signals, data inputs, and outputs is shown in Table 2–23.

Refer to the *DSP Blocks in Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook* for more information on DSP blocks.

*Figure 2–66. EP2SGX60, EP2SGX90 and EP2SGX130 Device I/O Clock Groups*




You can use the Quartus II software to control whether a clock input pin drives either a global, regional, or dual-regional clock network. The Quartus II software automatically selects the clocking resources if not specified.

### *Clock Control Block*

Each global clock, regional clock, and PLL external clock output has its own clock control block. The control block has two functions:

- Clock source selection (dynamic selection for global clocks)
- Clock power-down (dynamic clock enable or disable)

The Quartus II software enables the PLLs and their features without requiring any external devices. Table 2–25 shows the PLLs available for each Stratix II GX device and their type.

*Table 2–25. Stratix II GX Device PLL Availability* *Notes (1), (2)*

| Device | Fast PLLs | | | | | | | | Enhanced PLLs | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 *(3)* | 4 *(3)* | 7 | 8 | 9 *(3)* | 10 *(3)* | 5 | 6 | 11 | 12 |
| EP2SGX30 | ✓ | ✓ | | | | | | | ✓ | ✓ | | |
| EP2SGX60 | ✓ | ✓ | | | ✓ | ✓ | | | ✓ | ✓ | ✓ | ✓ |
| EP2SGX90 | ✓ | ✓ | | | ✓ | ✓ | | | ✓ | ✓ | ✓ | ✓ |
| EP2SGX130 | ✓ | ✓ | | | ✓ | ✓ | | | ✓ | ✓ | ✓ | ✓ |

*Notes to Table 2–25:*

(1) EP2SGX30C/D and EP2SGX60C/D devices only have two fast PLLs (1 and 2), but the connectivity from these two PLLs to the global and regional clock networks remains the same as shown. The EP2S60C/D devices only have two enhanced PLLs (5 and 6).

(2) The global or regional clocks in a fast PLL's quadrant can drive the fast PLL input. A dedicated clock input pin or other PLL must drive the global or regional source. The source cannot be driven by internally generated logic before driving the fast PLL.

(3) PLLs 3, 4, 9, and 10 are not available in Stratix II GX devices. However, these PLLs are listed in Table 2–25 because the Stratix II GX PLL numbering scheme is consistent with Stratix and Stratix II devices.

- Open-drain outputs
- DQ and DQS I/O pins
- Double data rate (DDR) registers

The IOE in Stratix II GX devices contains a bidirectional I/O buffer, six registers, and a latch for a complete embedded bidirectional single data rate or DDR transfer. Figure 2–76 shows the Stratix II GX IOE structure. The IOE contains two input registers (plus a latch), two output registers, and two output enable registers. You can use both input registers and the latch to capture DDR input and both output registers to drive DDR outputs. Additionally, you can use the output enable (OE) register for fast clock-to-output enable timing. The negative edge-clocked OE register is used for DDR SDRAM interfacing. The Quartus II software automatically duplicates a single OE register that controls multiple output or bidirectional pins.

generated by the Quartus II software. JRunner is targeted for embedded JTAG configuration. The source code is developed for the Windows NT operating system (OS), but can be customized to run on other platforms.

For more information on the JRunner software driver, refer to the *AN 414: An Embedded Solution for PLD JTAG Configuration* and the source files on the Altera web site (www.altera.com).

## Programming Serial Configuration Devices with SRunner

A serial configuration device can be programmed in-system by an external microprocessor using SRunner. SRunner is a software driver developed for embedded serial configuration device programming that can be easily customized to fit into different embedded systems. SRunner reads a Raw Programming Data file (**.rpd**) and writes to serial configuration devices. The serial configuration device programming time using SRunner is comparable to the programming time when using the Quartus II software.

For more information about SRunner, refer to the *AN 418 SRunner: An Embedded Solution for Serial Configuration Device Programming* and the source code on the Altera web site.

For more information on programming serial configuration devices, refer to the *Serial Configuration Devices (EPCS1, EPCS4, EPCS64, and EPCS128) Data Sheet* in the *Configuration Handbook*.

## Configuring Stratix II FPGAs with the MicroBlaster Driver

The MicroBlaster software driver supports an RBF programming input file and is ideal for embedded FPP or PS configuration. The source code is developed for the Windows NT operating system, although it can be customized to run on other operating systems.

For more information on the MicroBlaster software driver, refer to the *Configuring the MicroBlaster Fast Passive Parallel Software Driver White Paper* or the *Configuring the MicroBlaster Passive Serial Software Driver White Paper* on the Altera web site.

## PLL Reconfiguration

The phase-locked loops (PLLs) in the Stratix II GX device family support reconfiguration of their multiply, divide, VCO-phase selection, and bandwidth selection settings without reconfiguring the entire device. You can use either serial data from the logic array or regular I/O pins to program the PLL's counter settings in a serial chain. This option provides

The temperature sensing diode is a very sensitive circuit which can be influenced by noise coupled from other traces on the board, and possibly within the device package itself, depending on device usage. The interfacing device registers temperature based on millivolts of difference as seen at the TSD. Switching I/O near the TSD pins can affect the temperature reading. Altera recommends you take temperature readings during periods of no activity in the device (for example, standby mode where no clocks are toggling in the device), such as when the nearby I/Os are at a DC state, and disable clock networks in the device.

## Automated Single Event Upset (SEU) Detection

Stratix II GX devices offer on-chip circuitry for automated checking of single event upset (SEU) detection. Some applications that require the device to operate error free at high elevations or in close proximity to Earth's North or South Pole will require periodic checks to ensure continued data integrity. The error detection cyclic redundancy check (CRC) feature controlled by the **Device & Pin Options** dialog box in the Quartus II software uses a 32-bit CRC circuit to ensure data reliability and is one of the best options for mitigating SEU.

You can implement the error detection CRC feature with existing circuitry in Stratix II GX devices, eliminating the need for external logic. Stratix II GX devices compute CRC during configuration and checks the computed-CRC against an automatically computed CRC during normal operation. The `CRC_ERROR` pin reports a soft error when configuration SRAM data is corrupted, triggering device reconfiguration.

### Custom-Built Circuitry

Dedicated circuitry is built into Stratix II GX devices to automatically perform error detection. This circuitry constantly checks for errors in the configuration SRAM cells while the device is in user mode. You can monitor one external pin for the error and use it to trigger a reconfiguration cycle. You can select the desired time between checks by adjusting a built-in clock divider.

### Software Interface

Beginning with version 4.1 of the Quartus II software, you can turn on the automated error detection CRC feature in the **Device & Pin Options** dialog box. This dialog box allows you to enable the feature and set the internal frequency of the CRC between 400 kHz to 50 MHz. This controls the rate that the CRC circuitry verifies the internal configuration SRAM bits in the Stratix II GX FPGA.

For more information on CRC, refer to *AN 357: Error Detection Using CRC in Altera FPGA Devices*.

*Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 3 of 19)*

| Symbol/ Description | Conditions | -3 Speed Commercial Speed Grade | | | -4 Speed Commercial and Industrial Speed Grade | | | -5 Speed Commercial Speed Grade | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| **Fibre Channel Transmit Jitter Generation** *(8), (17)* | | | | | | | | | | | |
| Total jitter FC-1 | REFCLK = 106.25 MHz Pattern = CRPAT $V_{OD}$ = 800 mV No Pre-emphasis | - | - | 0.23 | - | - | 0.23 | - | - | 0.23 | UI |
| Deterministic jitter FC-1 | REFCLK = 106.25 MHz Pattern = CRPAT $V_{OD}$ = 800 mV No Pre-emphasis | - | - | 0.11 | - | - | 0.11 | - | - | 0.11 | UI |
| Total jitter FC-2 | REFCLK = 106.25 MHz Pattern = CRPAT $V_{OD}$ = 800 mV No Pre-emphasis | - | - | 0.33 | - | - | 0.33 | - | - | 0.33 | UI |
| Deterministic jitter FC-2 | REFCLK = 106.25 MHz Pattern = CRPAT $V_{OD}$ = 800 mV No Pre-emphasis | - | - | 0.2 | - | - | 0.2 | - | - | 0.2 | UI |
| Total jitter FC-4 | REFCLK = 106.25 MHz Pattern = CRPAT $V_{OD}$ = 800 mV No Pre-emphasis | - | - | 0.52 | - | - | 0.52 | - | - | 0.52 | UI |
| Deterministic jitter FC-4 | REFCLK = 106.25 MHz Pattern = CRPAT $V_{OD}$ = 800 mV No Pre-emphasis | - | - | 0.33 | - | - | 0.33 | - | - | 0.33 | UI |
| **Fibre Channel Receiver Jitter Tolerance** *(8), (18)* | | | | | | | | | | | |
| Deterministic jitter FC-1 | Pattern = CJTPAT No Equalization DC Gain = 0 dB | > 0.37 | | | > 0.37 | | | > 0.37 | | | UI |
| Random jitter FC-1 | Pattern = CJTPAT No Equalization DC Gain = 0 dB | > 0.31 | | | > 0.31 | | | > 0.31 | | | UI |

*Table 4–31. PCML Specifications* *Note (1)*

| Symbol | Parameter | References |
|---|---|---|
| **Reference Clock** | | |
| 3.3-V PCML<br>1.5-V PCML<br>1.2-V PCML | Reference clock supported PCML standards | |
| $V_{ID}$ | Peak-to-peak differential input voltage | The specifications are located in the Reference Clock section of Table 4–6 on page 4–4.<br><br>The specifications listed in Table 4–6 are applicable to PCML input standards. |
| $V_{ICM}$ | Input common mode voltage | |
| R | On-chip termination resistors | |
| **Receiver** | | |
| 3.3-V PCML<br>1.5-V PCML<br>1.2-V PCML | Receiver supported PCML standards | |
| $V_{ID}$ | Peak-to-peak differential input voltage | The specifications are located in the Receiver section of Table 4–6 on page 4–4.<br><br>The specifications listed in Table 4–6 are applicable to PCML input standards. |
| $V_{ICM}$ | Input common mode voltage | |
| R | On-chip termination resistors | |
| **Transmitter** | | |
| 1.5-V PCML<br>1.2-V PCML | Transmitter supported PCML standards | |
| $V_{CCH}$ | Output buffer supply voltage | The specifications are located in Table 4–5 on page 4–4. |
| $V_{OD}$ | Peak-to-peak differential output voltage | The specifications are located in Tables 4–7, 4–8, 4–9, 4–10, 4–11, and 4–12.<br><br>The specifications listed in these tables are applicable to PCML output standards. |
| $V_{OCM}$ | Output common mode voltage | The specifications are located in the Transmitter section of Table 4–6 on page 4–4.<br><br>The specifications listed in Table 4–6 are applicable to PCML output standards. |
| R | On-chip termination resistors | |

*Note to Table 4–31:*

(1) Stratix II GX devices support PCML input and output on GXB banks 13, 14, 15, 16, and 17. This table references Stratix II GX PCML specifications that are located in other sections of the *Stratix II GX Device Handbook*.

*Table 4–49. On-Chip Termination Specification for Top and Bottom I/O Banks (Part 2 of 2)* *Notes (1), (2)*

| Symbol | Description | Conditions | Resistance Tolerance | | |
|---|---|---|---|---|---|
| | | | Commercial Max | Industrial Max | Unit |
| 50-Ω $R_T$ 2.5 | Internal parallel termination with calibration (50-Ω setting) | $V_{CCIO}$ = 1.8 V | ±30 | ± 30 | % |
| 25-Ω $R_S$ 1.8 | Internal series termination with calibration (25-Ω setting) | $V_{CCIO}$ = 1.8 V | ±5 | ±10 | % |
| | Internal series termination without calibration (25-Ω setting) | $V_{CCIO}$ = 1.8 V | ±30 | ±30 | % |
| 50-Ω $R_S$ 1.8 | Internal series termination with calibration (50-Ω setting) | $V_{CCIO}$ = 1.8 V | ±5 | ±10 | % |
| | Internal series termination without calibration (50-Ω setting) | $V_{CCIO}$ = 1.8 V | ±30 | ±30 | % |
| 50-Ω $R_T$ 1.8 | Internal parallel termination with calibration (50-Ω setting) | $V_{CCIO}$ = 1.8 V | ±10 | ±15 | % |
| 50-Ω $R_S$ 1.5 | Internal series termination with calibration (50-Ω setting) | $V_{CCIO}$ = 1.5 V | ±8 | ±10 | % |
| | Internal series termination without calibration (50-Ω setting) | $V_{CCIO}$ = 1.5 V | ±36 | ±36 | % |
| 50-Ω $R_T$ 1.5 | Internal parallel termination with calibration (50-Ω setting) | $V_{CCIO}$ = 1.5 V | ±10 | ±15 | % |
| 50-Ω $R_S$ 1.2 | Internal series termination with calibration (50-Ω setting) | $V_{CCIO}$ = 1.2 V | ±8 | ±10 | % |
| | Internal series termination without calibration (50-Ω setting) | $V_{CCIO}$ = 1.2 V | ±50 | ±50 | % |
| 50-Ω $R_T$ 1.2 | Internal parallel termination with calibration (50-Ω setting) | $V_{CCIO}$ = 1.2 V | ±10 | ±15 | % |

*Note for Table 4–49:*

(1) The resistance tolerance for calibrated SOCT is for the moment of calibration. If the temperature or voltage changes over time, the tolerance may also change.

(2) On-chip parallel termination with calibration is only supported for input pins.

*Table 4–84. Stratix II GX I/O Input Delay for Column Pins (Part 2 of 3)*

| I/O Standard | Parameter | Fast Corner Industrial/ Commercial | -3 Speed Grade *(2)* | -3 Speed Grade *(3)* | -4 Speed Grade | -5 Speed Grade | Unit |
|---|---|---|---|---|---|---|---|
| 2.5 V | $t_{PI}$ | 717 | 1210 | 1269 | 1349 | 1619 | ps |
| | $t_{PCOUT}$ | 438 | 774 | 812 | 863 | 1036 | ps |
| 1.8 V | $t_{PI}$ | 783 | 1366 | 1433 | 1523 | 1829 | ps |
| | $t_{PCOUT}$ | 504 | 930 | 976 | 1037 | 1246 | ps |
| 1.5 V | $t_{PI}$ | 786 | 1436 | 1506 | 1602 | 1922 | ps |
| | $t_{PCOUT}$ | 507 | 1000 | 1049 | 1116 | 1339 | ps |
| LVCMOS | $t_{PI}$ | 707 | 1223 | 1282 | 1364 | 1637 | ps |
| | $t_{PCOUT}$ | 428 | 787 | 825 | 878 | 1054 | ps |
| SSTL-2 Class I | $t_{PI}$ | 530 | 818 | 857 | 912 | 1094 | ps |
| | $t_{PCOUT}$ | 251 | 382 | 400 | 426 | 511 | ps |
| SSTL-2 Class II | $t_{PI}$ | 530 | 818 | 857 | 912 | 1094 | ps |
| | $t_{PCOUT}$ | 251 | 382 | 400 | 426 | 511 | ps |
| SSTL-18 Class I | $t_{PI}$ | 569 | 898 | 941 | 1001 | 1201 | ps |
| | $t_{PCOUT}$ | 290 | 462 | 484 | 515 | 618 | ps |
| SSTL-18 Class II | $t_{PI}$ | 569 | 898 | 941 | 1001 | 1201 | ps |
| | $t_{PCOUT}$ | 290 | 462 | 484 | 515 | 618 | ps |
| 1.5-V HSTL Class I | $t_{PI}$ | 587 | 993 | 1041 | 1107 | 1329 | ps |
| | $t_{PCOUT}$ | 308 | 557 | 584 | 621 | 746 | ps |
| 1.5-V HSTL Class II | $t_{PI}$ | 587 | 993 | 1041 | 1107 | 1329 | ps |
| | $t_{PCOUT}$ | 308 | 557 | 584 | 621 | 746 | ps |
| 1.8-V HSTL Class I | $t_{PI}$ | 569 | 898 | 941 | 1001 | 1201 | ps |
| | $t_{PCOUT}$ | 290 | 462 | 484 | 515 | 618 | ps |
| 1.8-V HSTL Class II | $t_{PI}$ | 569 | 898 | 941 | 1001 | 1201 | ps |
| | $t_{PCOUT}$ | 290 | 462 | 484 | 515 | 618 | ps |
| PCI | $t_{PI}$ | 712 | 1214 | 1273 | 1354 | 1625 | ps |
| | $t_{PCOUT}$ | 433 | 778 | 816 | 868 | 1042 | ps |
| PCI-X | $t_{PI}$ | 712 | 1214 | 1273 | 1354 | 1625 | ps |
| | $t_{PCOUT}$ | 433 | 778 | 816 | 868 | 1042 | ps |
| Differential SSTL-2 Class I *(1)* | $t_{PI}$ | 530 | 818 | 857 | 912 | 1094 | ps |
| | $t_{PCOUT}$ | 251 | 382 | 400 | 426 | 511 | ps |

| Table 4–84. Stratix II GX I/O Input Delay for Column Pins (Part 3 of 3) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **I/O Standard** | **Parameter** | **Fast Corner Industrial/ Commercial** | **-3 Speed Grade** *(2)* | **-3 Speed Grade** *(3)* | **-4 Speed Grade** | **-5 Speed Grade** | **Unit** |
| Differential SSTL-2 Class II *(1)* | $t_{PI}$ | 530 | 818 | 857 | 912 | 1094 | ps |
| | $t_{PCOUT}$ | 251 | 382 | 400 | 426 | 511 | ps |
| Differential SSTL-18 Class I *(1)* | $t_{PI}$ | 569 | 898 | 941 | 1001 | 1201 | ps |
| | $t_{PCOUT}$ | 290 | 462 | 484 | 515 | 618 | ps |
| Differential SSTL-18 Class II *(1)* | $t_{PI}$ | 569 | 898 | 941 | 1001 | 1201 | ps |
| | $t_{PCOUT}$ | 290 | 462 | 484 | 515 | 618 | ps |
| 1.8-V differential HSTL Class I *(1)* | $t_{PI}$ | 569 | 898 | 941 | 1001 | 1201 | ps |
| | $t_{PCOUT}$ | 290 | 462 | 484 | 515 | 618 | ps |
| 1.8-V differential HSTL Class II *(1)* | $t_{PI}$ | 569 | 898 | 941 | 1001 | 1201 | ps |
| | $t_{PCOUT}$ | 290 | 462 | 484 | 515 | 618 | ps |
| 1.5-V differential HSTL Class I *(1)* | $t_{PI}$ | 587 | 993 | 1041 | 1107 | 1329 | ps |
| | $t_{PCOUT}$ | 308 | 557 | 584 | 621 | 746 | ps |
| 1.5-V differential HSTL Class II *(1)* | $t_{PI}$ | 587 | 993 | 1041 | 1107 | 1329 | ps |
| | $t_{PCOUT}$ | 308 | 557 | 584 | 621 | 746 | ps |

(1) These I/O standards are only supported on DQS pins.
(2) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
(3) This column refers to –3 speed grades for EP2SGX130 devices.

| Table 4–85. Stratix II GX I/O Input Delay for Row Pins (Part 1 of 3) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **I/O Standard** | **Parameter** | **Fast Corner Industrial/ Commercial** | **-3 Speed Grade** *(2)* | **-3 Speed Grade** *(3)* | **-4 Speed Grade** | **-5 Speed Grade** | **Unit** |
| LVTTL | $t_{PI}$ | 749 | 1287 | 1350 | 1435 | 1723 | ps |
| | $t_{PCOUT}$ | 410 | 760 | 798 | 848 | 1018 | ps |
| 2.5 V | $t_{PI}$ | 761 | 1273 | 1335 | 1419 | 1704 | ps |
| | $t_{PCOUT}$ | 422 | 746 | 783 | 832 | 999 | ps |
| 1.8 V | $t_{PI}$ | 827 | 1427 | 1497 | 1591 | 1911 | ps |
| | $t_{PCOUT}$ | 488 | 900 | 945 | 1004 | 1206 | ps |
| 1.5 V | $t_{PI}$ | 830 | 1498 | 1571 | 1671 | 2006 | ps |
| | $t_{PCOUT}$ | 491 | 971 | 1019 | 1084 | 1301 | ps |

| Table 4–86. Stratix II GX I/O Output Delay for Column Pins (Part 3 of 7) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| I/O Standard | Drive Strength | Parameter | Fast Corner Industrial/ Commercial | -3 Speed Grade *(3)* | -3 Speed Grade *(4)* | -4 Speed Grade | -5 Speed Grade | Unit |
| SSTL-2 Class I | 8 mA | $t_{OP}$ | 957 | 1715 | 1799 | 1913 | 2041 | ps |
| | | $t_{DIP}$ | 979 | 1781 | 1869 | 1987 | 2131 | ps |
| | 12 mA *(1)* | $t_{OP}$ | 940 | 1672 | 1754 | 1865 | 1991 | ps |
| | | $t_{DIP}$ | 962 | 1738 | 1824 | 1939 | 2081 | ps |
| SSTL-2 Class II | 16 mA | $t_{OP}$ | 918 | 1609 | 1688 | 1795 | 1918 | ps |
| | | $t_{DIP}$ | 940 | 1675 | 1758 | 1869 | 2008 | ps |
| | 20 mA | $t_{OP}$ | 919 | 1598 | 1676 | 1783 | 1905 | ps |
| | | $t_{DIP}$ | 941 | 1664 | 1746 | 1857 | 1995 | ps |
| | 24 mA *(1)* | $t_{OP}$ | 915 | 1596 | 1674 | 1781 | 1903 | ps |
| | | $t_{DIP}$ | 937 | 1662 | 1744 | 1855 | 1993 | ps |
| SSTL-18 Class I | 4 mA | $t_{OP}$ | 953 | 1690 | 1773 | 1886 | 2012 | ps |
| | | $t_{DIP}$ | 975 | 1756 | 1843 | 1960 | 2102 | ps |
| | 6 mA | $t_{OP}$ | 958 | 1656 | 1737 | 1848 | 1973 | ps |
| | | $t_{DIP}$ | 980 | 1722 | 1807 | 1922 | 2063 | ps |
| | 8 mA | $t_{OP}$ | 937 | 1640 | 1721 | 1830 | 1954 | ps |
| | | $t_{DIP}$ | 959 | 1706 | 1791 | 1904 | 2044 | ps |
| | 10 mA | $t_{OP}$ | 942 | 1638 | 1718 | 1827 | 1952 | ps |
| | | $t_{DIP}$ | 964 | 1704 | 1788 | 1901 | 2042 | ps |
| | 12 mA *(1)* | $t_{OP}$ | 936 | 1626 | 1706 | 1814 | 1938 | ps |
| | | $t_{DIP}$ | 958 | 1692 | 1776 | 1888 | 2028 | ps |
| SSTL-18 Class II | 8 mA | $t_{OP}$ | 925 | 1597 | 1675 | 1782 | 1904 | ps |
| | | $t_{DIP}$ | 947 | 1663 | 1745 | 1856 | 1994 | ps |
| | 16 mA | $t_{OP}$ | 937 | 1578 | 1655 | 1761 | 1882 | ps |
| | | $t_{DIP}$ | 959 | 1644 | 1725 | 1835 | 1972 | ps |
| | 18 mA | $t_{OP}$ | 933 | 1585 | 1663 | 1768 | 1890 | ps |
| | | $t_{DIP}$ | 955 | 1651 | 1733 | 1842 | 1980 | ps |
| | 20 mA *(1)* | $t_{OP}$ | 933 | 1583 | 1661 | 1766 | 1888 | ps |
| | | $t_{DIP}$ | 955 | 1649 | 1731 | 1840 | 1978 | ps |

| Table 4–91. Stratix II GX Maximum Output Clock Rate for Column Pins (Part 3 of 3) | | | | | |
|---|---|---|---|---|---|
| **I/O Standard** | **Drive Strength** | **-3 Speed Grade** | **-4 Speed Grade** | **-5 Speed Grade** | **Unit** |
| Differential SSTL-18 Class I | 4 mA | 200 | 150 | 150 | MHz |
| | 6 mA | 350 | 250 | 200 | MHz |
| | 8 mA | 450 | 300 | 300 | MHz |
| | 10 mA | 500 | 400 | 400 | MHz |
| | 12 mA | 700 | 550 | 400 | MHz |
| Differential SSTL-18 Class II | 8 mA | 200 | 200 | 150 | MHz |
| | 16 mA | 400 | 350 | 350 | MHz |
| | 18 mA | 450 | 400 | 400 | MHz |
| | 20 mA | 550 | 500 | 450 | MHz |
| 1.8-V HSTL differential Class I | 4 mA | 300 | 300 | 300 | MHz |
| | 6 mA | 500 | 450 | 450 | MHz |
| | 8 mA | 650 | 600 | 600 | MHz |
| | 10 mA | 700 | 650 | 600 | MHz |
| | 12 mA | 700 | 700 | 650 | MHz |
| 1.8-V HSTL differential Class II | 16 mA | 500 | 500 | 450 | MHz |
| | 18 mA | 550 | 500 | 500 | MHz |
| | 20 mA | 650 | 550 | 550 | MHz |
| 1.5-V HSTL differential Class I | 4 mA | 350 | 300 | 300 | MHz |
| | 6 mA | 500 | 500 | 450 | MHz |
| | 8 mA | 700 | 650 | 600 | MHz |
| | 10 mA | 700 | 700 | 650 | MHz |
| | 12 mA | 700 | 700 | 700 | MHz |
| 1.5-V HSTL differential Class II | 16 mA | 600 | 600 | 550 | MHz |
| | 18 mA | 650 | 600 | 600 | MHz |
| | 20 mA | 700 | 650 | 600 | MHz |

(1) This is the default setting in the Quartus II software.

*Table 4–100. Maximum DCD for DDIO Output on Row I/O Pins Without PLL in the Clock Path for -3 Devices* *Note (1)*

| Maximum DCD (ps) for Row DDIO Output I/O Standard | Input I/O Standard (No PLL in Clock Path) | | | | | Unit |
|---|---|---|---|---|---|---|
| | TTL/CMOS | | SSTL-2 | SSTL/HSTL | LVDS | |
| | 3.3 and 2.5 V | 1.8 and 1.5 V | 2.5 V | 1.8 and 1.5 V | 3.3 V | |
| 3.3-V LVTTL | 260 | 380 | 145 | 145 | 110 | ps |
| 3.3-V LVCMOS | 210 | 330 | 100 | 100 | 65 | ps |
| 2.5 V | 195 | 315 | 85 | 85 | 75 | ps |
| 1.8 V | 150 | 265 | 85 | 85 | 120 | ps |
| 1.5-V LVCMOS | 255 | 370 | 140 | 140 | 105 | ps |
| SSTL-2 Class I | 175 | 295 | 65 | 65 | 70 | ps |
| SSTL-2 Class II | 170 | 290 | 60 | 60 | 75 | ps |
| SSTL-18 Class I | 155 | 275 | 55 | 50 | 90 | ps |
| 1.8-V HSTL Class I | 150 | 270 | 60 | 60 | 95 | ps |
| 1.5-V HSTL Class I | 150 | 270 | 55 | 55 | 90 | ps |
| LVDS | 180 | 180 | 180 | 180 | 180 | ps |

(1) The information in Table 4–100 assumes the input clock has zero DCD.

Here is an example for calculating the DCD in percentage for a DDIO output on a row I/O on a -3 device:

If the input I/O standard is 2.5-V SSTL-2 and the DDIO output I/O standard is SSTL-2 Class= II, the maximum DCD is 60 ps (see Table 4–100). If the clock frequency is 267 MHz, the clock period T is:

T = 1/ f = 1 / 267 MHz = 3.745 ns = 3,745 ps

Calculate the DCD as a percentage:

(T/2 – DCD) / T = (3,745 ps/2 – 60 ps) / 3745 ps = 48.4% (for low boundary)

(T/2 + DCD) / T = (3,745 ps/2 + 60 ps) / 3745 ps = 51.6% (for high boundary)