Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

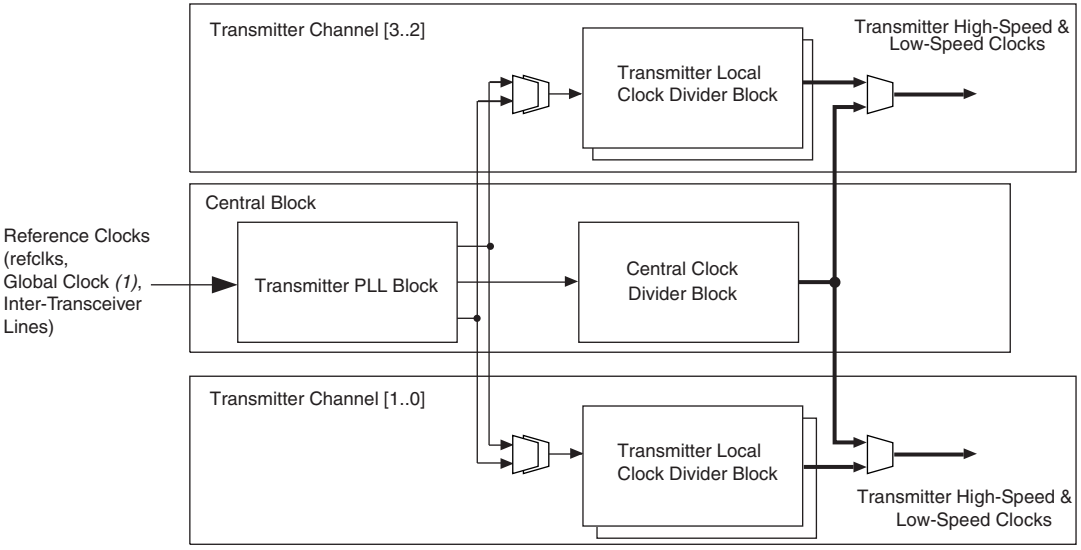
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	6627
Number of Logic Elements/Cells	132540
Total RAM Bits	6747840
Number of I/O	734
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1508-BBGA, FCBGA
Supplier Device Package	1508-FBGA, FC (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2sgx130gf40c4nes

Figure 2–3. Clock Distribution for the Transmitters Note (1)



Note to Figure 2–3:
(1) The global clock line must be driven by an input pin.

The transmitter PLLs in each transceiver block clock the PMA and PCS circuitry in the transmit path. The Quartus II software automatically powers down the transmitter PLLs that are not used in the design. Figure 2–4 is a block diagram of the transmitter PLL.

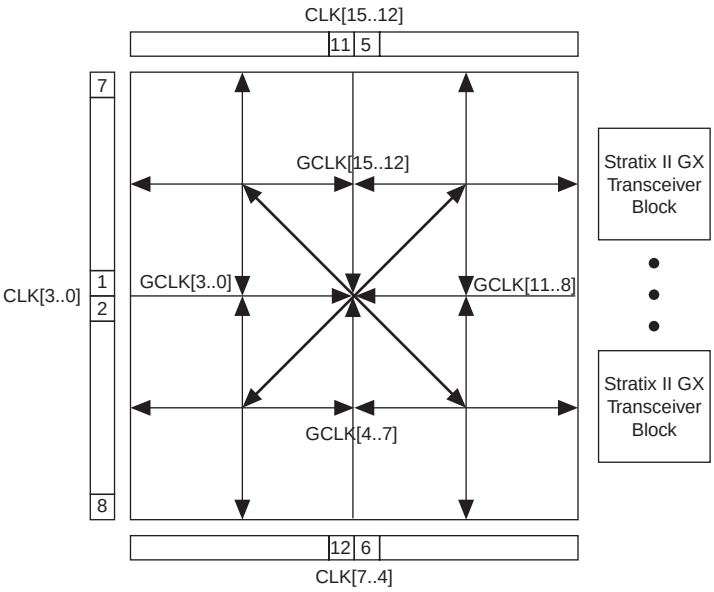
The transmitter phase/frequency detector references the clock from one of the following sources:

- Reference clocks
- Reference clock from the adjacent transceiver block
- Inter-transceiver block clock lines
- Global clock line driven by input pin

Two reference clocks, `REFCLK0` and `REFCLK1`, are available per transceiver block. The inter-transceiver block bus allows multiple transceivers to use the same reference clocks. Each transceiver block has one outgoing reference clock which connects to one inter-transceiver block line. The incoming reference clock can be selected from five inter-transceiver block lines `IQ[4..0]` or from the global clock line that is driven by an input pin.

The receiver PLL can also drive the regional clocks and regional routing adjacent to the associated transceiver block. Figure 2–30 shows which global clock resource can be used by the recovered clock. Figure 2–31 shows which regional clock resource can be used by the recovered clock.

Figure 2–30. Stratix II GX Receiver PLL Recovered Clock to Global Clock Connection *Notes (1), (2)*



Notes to Figure 2–30:

(1) CLK# pins are clock pins and their associated number. These are pins for global and regional clocks.

(2) GCLK# pins are global clock pins.

Table 2–13. Available Clocking Connections for Transceivers in 2SGX60E

Region	Clock Resource		Transceiver		
	Global Clock	Regional Clock	Bank 13 8 Clock I/O	Bank 14 8 Clock I/O	Bank 15 8 Clock I/O
Region0 8 LRIO clock	✓	RCLK 20-27	✓		
Region1 8 LRIO clock	✓	RCLK 20-27	✓	✓	
Region2 8 LRIO clock	✓	RCLK 12-19		✓	✓
Region3 8 LRIO clock	✓	RCLK 12-19			✓

Table 2–14. Available Clocking Connections for Transceivers in 2SGX90F

Region	Clock Resource		Transceiver			
	Global Clock	Regional Clock	Bank 13 8 Clock I/O	Bank 14 8 Clock I/O	Bank 15 8 clock I/O	Bank 16 8 Clock I/O
Region0 8 LRIO clock	✓	RCLK 20-27	✓			
Region1 8 LRIO clock	✓	RCLK 20-27		✓		
Region2 8 LRIO clock	✓	RCLK 12-19			✓	
Region3 8 LRIO clock	✓	RCLK 12-19				✓

.

Table 2–15. Available Clocking Connections for Transceivers in 2SGX130G

Region	Clock Resource		Transceiver				
	Global Clock	Regional Clock	Bank 13 8 Clock I/O	Bank 14 8 Clock I/O	Bank 15 8 clock I/O	Bank 16 8 Clock I/O	Bank 17 8 Clock I/O
Region0 8 LRIO clock	✓	RCLK 20-27	✓				
Region1 8 LRIO clock	✓	RCLK 20-27		✓			
Region2 8 LRIO clock	✓	RCLK 12-19			✓	✓	
Region3 8 LRIO clock	✓	RCLK 12-19				✓	✓

Other Transceiver Features

Other important features of the Stratix II GX transceivers are the power down and reset capabilities, external voltage reference and bias circuitry, and hot swapping.

Calibration Block

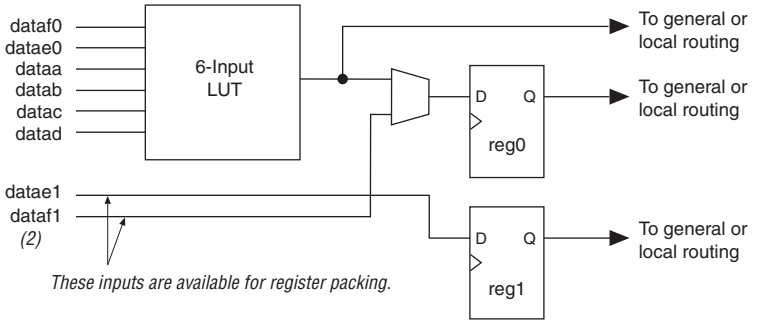
The Stratix II GX device uses the calibration block to calibrate the on-chip termination for the PLLs and their associated output buffers and the terminating resistors on the transceivers. The calibration block counters the effects of process, voltage, and temperature (PVT). The calibration block references a derived voltage across an external reference resistor to calibrate the on-chip termination resistors on the Stratix II GX device. The calibration block can be powered down. However, powering down the calibration block during operations may yield transmit and receive data errors.

Dynamic Reconfiguration

This feature allows you to dynamically reconfigure the PMA portion and the channel parameters, such as data rate and functional mode, of the Stratix II GX transceiver. The PMA reconfiguration allows you to quickly optimize the settings for the transceiver's PMA to achieve the intended bit error rate (BER).

using the bottom set of output drivers. The Quartus II Compiler automatically selects the inputs to the LUT. Asynchronous load data for the register comes from the `datae` or `dataf` input of the ALM. ALMs in normal mode support register packing.

Figure 2–39. 6-Input Function in Normal Mode *Notes (1), (2)*



Notes to Figure 2–39:

(1) If `datae1` and `dataf1` are used as inputs to the six-input function, `datae0` and `dataf0` are available for register packing.

(2) The `dataf1` input is available for register packing only if the six-input function is un-registered.

Extended LUT Mode

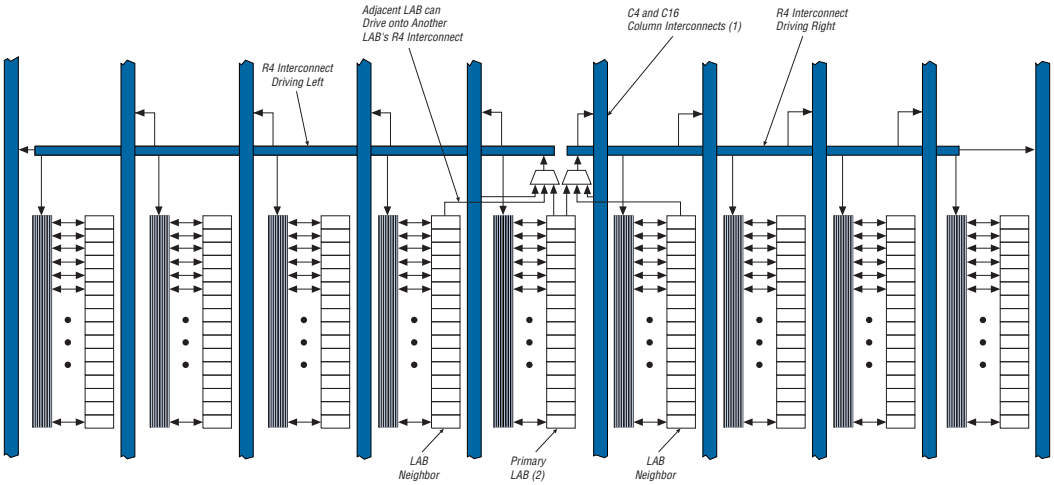
The extended LUT mode is used to implement a specific set of seven-input functions. The set must be a 2-to-1 multiplexer fed by two arbitrary five-input functions sharing four inputs. Figure 2–40 shows the template of supported seven-input functions utilizing extended LUT mode. In this mode, if the seven-input function is unregistered, the unused eighth input is available for register packing. Functions that fit into the template shown in Figure 2–40 occur naturally in designs. These functions often appear in designs as "if-else" statements in Verilog HDL or VHDL code.

The direct link interconnect allows a LAB, DSP block, or TriMatrix memory block to drive into the local interconnect of its left and right neighbors and then back into itself, providing fast communication between adjacent LABs and/or blocks without using row interconnect resources.

The R4 interconnects span four LABs, three LABs and one M512 RAM block, two LABs and one M4K RAM block, or two LABs and one DSP block to the right or left of a source LAB. These resources are used for fast row connections in a four-LAB region. Every LAB has its own set of R4 interconnects to drive either left or right. Figure 2–46 shows R4 interconnect connections from a LAB.

R4 interconnects can drive and be driven by DSP blocks and RAM blocks and row IOEs. For LAB interfacing, a primary LAB or LAB neighbor can drive a given R4 interconnect. For R4 interconnects that drive to the right, the primary LAB and right neighbor can drive onto the interconnect. For R4 interconnects that drive to the left, the primary LAB and its left neighbor can drive onto the interconnect. R4 interconnects can drive other R4 interconnects to extend the range of LABs they can drive. R4 interconnects can also drive C4 and C16 interconnects for connections from one row to another. Additionally, R4 interconnects can drive R24 interconnects.

Figure 2–46. R4 Interconnect Connections *Notes (1), (2), (3)*



Notes to Figure 2–46:

(1) C4 and C16 interconnects can drive R4 interconnects.
(2) This pattern is repeated for every LAB in the LAB row.
(3) The LABs in Figure 2–46 show the 16 possible logical outputs per LAB.

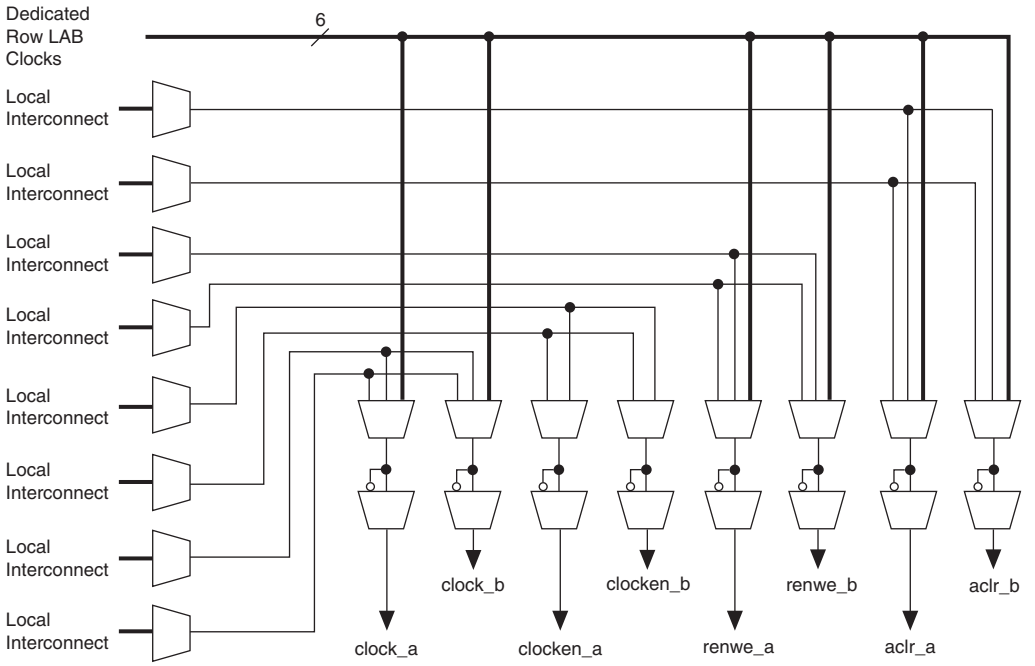
C16 column interconnects span a length of 16 LABs and provide the fastest resource for long column connections between LABs, TriMatrix memory blocks, DSP blocks, and IOEs. C16 interconnects can cross M-RAM blocks and also drive to row and column interconnects at every fourth LAB. C16 interconnects drive LAB local interconnects via C4 and R4 interconnects and do not drive LAB local interconnects directly. All embedded blocks communicate with the logic array similar to LAB-to-LAB interfaces. Each block (that is, TriMatrix memory and DSP blocks) connects to row and column interconnects and has local interconnect regions driven by row and column interconnects. These blocks also have direct link interconnects for fast connections to and from a neighboring LAB. All blocks are fed by the row LAB clocks, `labclk[5..0]`.

Table 2–18 shows the Stratix II GX device's routing scheme.

Table 2–18. Stratix II GX Device Routing Scheme (Part 1 of 2)

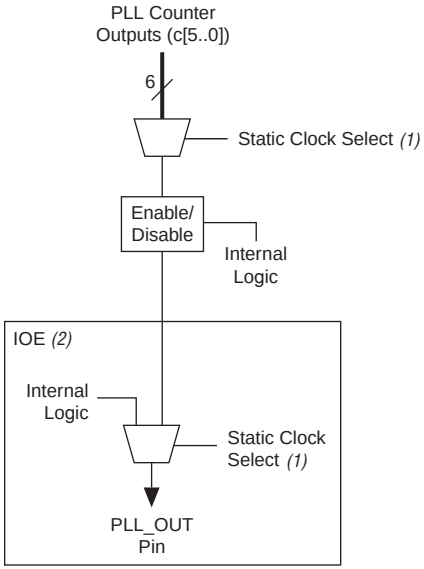
Source	Destination															
	Shared Arithmetic Chain	Carry Chain	Register Chain	Local Interconnect	Direct Link Interconnect	R4 Interconnect	R24 Interconnect	C4 Interconnect	C16 Interconnect	ALM	M512 RAM Block	M4K RAM Block	M-RAM Block	DSP Blocks	Column IOE	Row IOE
Shared arithmetic chain										✓						
Carry chain										✓						
Register chain										✓						
Local interconnect										✓	✓	✓	✓	✓	✓	✓
Direct link interconnect				✓												
R4 interconnect				✓		✓	✓	✓	✓							
R24 interconnect						✓	✓	✓	✓							
C4 interconnect				✓		✓		✓								
C16 interconnect						✓	✓	✓	✓							
ALM	✓	✓	✓	✓	✓	✓		✓								
M512 RAM block				✓	✓	✓		✓								
M4K RAM block				✓	✓	✓		✓								
M-RAM block					✓	✓	✓	✓								
DSP blocks					✓	✓		✓								

Figure 2–51. M4K RAM Block Control Signals



The R4, C4, and direct link interconnects from adjacent LABs drive the M4K RAM block local interconnect. The M4K RAM blocks can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 16 direct link input connections to the M4K RAM block are possible from the left adjacent LABs and another 16 possible from the right adjacent LAB. M4K RAM block outputs can also connect to left and right LABs through direct link interconnect. Figure 2–52 shows the M4K RAM block to logic array interface.

Figure 2–69. External PLL Output Clock Control Blocks



Notes to Figure 2–69:

(1) These clock select signals can only be set through a configuration file (**.sof** or **.pof**) and cannot be dynamically controlled during user mode operation.

(2) The clock control block feeds to a multiplexer within the PLL_OUT pin's IOE. The PLL_OUT pin is a dual-purpose pin. Therefore, this multiplexer selects either an internal signal or the output of the clock control block.

For the global clock control block, the clock source selection can be controlled either statically or dynamically. You have the option of statically selecting the clock source by using the Quartus II software to set specific configuration bits in the configuration file (**.sof** or **.pof**) or you can control the selection dynamically by using internal logic to drive the multiplexer select inputs. When selecting statically, the clock source can be set to any of the inputs to the select multiplexer. When selecting the clock source dynamically, you can either select between two PLL outputs (such as the C0 or C1 outputs from one PLL), between two PLLs (such as the C0/C1 clock output of one PLL or the C0/C1 clock output of the other PLL), between two clock pins (such as CLK0 or CLK1), or between a combination of clock pins or PLL outputs.

For the regional and PLL_OUT clock control block, the clock source selection can only be controlled statically using configuration bits. Any of the inputs to the clock select multiplexer can be set as the clock source.

These dedicated circuits combined, with enhanced PLL clocking and phase-shift ability, provide a complete hardware solution for interfacing to high-speed memory.

For more information on external memory interfaces, refer to the *External Memory Interfaces in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook*.

Programmable Drive Strength

The output buffer for each Stratix II GX device I/O pin has a programmable drive strength control for certain I/O standards. The LVTTL, LVCMOS, SSTL, and HSTL standards have several levels of drive strength that you can control. The default setting used in the Quartus II software is the maximum current strength setting that is used to achieve maximum I/O performance. For all I/O standards, the minimum setting is the lowest drive strength that guarantees the I_{OH}/I_{OL} of the standard. Using minimum settings provides signal slew rate control to reduce system noise and signal overshoot.

Table 2–41. EP2SGX130 Device Differential Channels *Note (1)*

Package	Transmitter/Receiver	Total Channels	Center Fast PLLs		Corner Fast PLLs	
			PLL1	PLL2	PLL7	PLL8
1508-pin FineLine BGA	Transmitter	71	37	41	37	41
	Receiver	73	37	41	37	41

Note to Tables 2–38 through 2–41:
(1) The total number of receiver channels includes the four non-dedicated clock channels that can be optionally used as data channels.

Therefore, the total number of channels is not the addition of the number of channels accessible by PLLs 1 and 2 with the number of channels accessible by PLLs 7 and 8.

Dedicated Circuitry with DPA Support

Stratix II GX devices support source-synchronous interfacing with LVDS signaling at up to 1 Gbps. Stratix II GX devices can transmit or receive serial channels along with a low-speed or high-speed clock.

The receiving device PLL multiplies the clock by an integer factor W = 1 through 32. The SERDES factor J determines the parallel data width to deserialize from receivers or to serialize for transmitters. The SERDES factor J can be set to 4, 5, 6, 7, 8, 9, or 10 and does not have to equal the PLL clock-multiplication W value. A design using the dynamic phase aligner also supports all of these J factor values. For a J factor of 1, the Stratix II GX device bypasses the SERDES block. For a J factor of 2, the Stratix II GX device bypasses the SERDES block, and the DDR input and output registers are used in the IOE. Figure 2–88 shows the block diagram of the Stratix II GX transmitter channel.

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 6 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Serial RapidIO Receiver Jitter Tolerance *(11)*											
Deterministic Jitter Tolerance (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps REFCLK = 125 MHz Pattern = CJPAT Equalizer Setting = 0 for 1.25 Gbps Equalizer Setting = 6 for 2.5 Gbps Equalizer Setting = 6 for 3.125 Gbps	> 0.37			> 0.37			> 0.37			UI
Combined Deterministic and Random Jitter Tolerance (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps REFCLK = 125 MHz Pattern = CJPAT Equalizer Setting = 0 for 1.25 Gbps Equalizer Setting = 6 for 2.5 Gbps Equalizer Setting = 6 for 3.125 Gbps	> 0.55			> 0.55			> 0.55			UI

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 19 of 19)											
Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	

Notes to Table 4–19:

(1) Dedicated REFCLK pins were used to drive the input reference clocks.
(2) Jitter numbers specified are valid for the stated conditions only.
(3) Refer to the protocol characterization documents for detailed information.
(4) HiGig configuration is available in a -3 speed grade only. For more information, refer to the *Stratix II GX Transceiver Architecture Overview* chapter in volume 2 of the *Stratix II GX Device Handbook*.
(5) Stratix II GX transceivers meet CEI jitter generation specification of 0.3 UI for a V_{OD} range of 400 mV to 1000 mV.
(6) The Sinusoidal Jitter Tolerance Mask is defined only for low voltage (LV) variant of CPRI.
(7) The jitter numbers for SONET/SDH are compliant to the GR-253-CORE Issue 3 Specification.
(8) The jitter numbers for Fibre Channel are compliant to the FC-PI-4 Specification revision 6.10.
(9) The jitter numbers for XAUI are compliant to the IEEE802.3ae-2002 Specification.
(10) The jitter numbers for PCI Express are compliant to the PCIe Base Specification 2.0.
(11) The jitter numbers for Serial RapidIO are compliant to the RapidIO Specification 1.3.
(12) The jitter numbers for GIGE are compliant to the IEEE802.3-2002 Specification.
(13) The jitter numbers for HiGig are compliant to the IEEE802.3ae-2002 Specification.
(14) The jitter numbers for (OIF) CEI are compliant to the OIF-CEI-02.0 Specification.
(15) The jitter numbers for CPRI are compliant to the CPRI Specification V2.1.
(16) The HD-SDI and 3G-SDI jitter numbers are compliant to the SMPTE292M and SMPTE424M Specifications.
(17) The Fibre Channel transmitter jitter generation numbers are compliant to the specification at β_T interoperability point.
(18) The Fibre Channel receiver jitter tolerance numbers are compliant to the specification at β_R interoperability point.

Table 4–20 provides information on recommended input clock jitter for each mode.

Table 4–20. Recommended Input Clock Jitter (Part 1 of 2)						
Mode	Reference Clock (MHz)	Vectron LVPECL XO Type/Model	Frequency Range (MHz)	RMS Jitter (12 kHz to 20 MHz) (ps)	Period Jitter (Peak to Peak) (ps)	Phase Noise at 1 MHz (dB c/Hz)
PCI-E	100	VCC6-Q/R	10 to 270	0.3	23	-149.9957
(OIF) CEI PHY	156.25	VCC6-Q/R	10 to 270	0.3	23	-146.2169
	622.08	VCC6-Q	270 to 800	2	30	Not available
GIGE	62.5	VCC6-Q/R	10 to 270	0.3	23	-149.9957
	125	VCC6-Q/R	10 to 270	0.3	23	-146.9957
XAUI	156.25	VCC6-Q/R	10 to 270	0.3	23	-146.2169

Figures 4–6 and 4–7 show receiver input and transmitter output waveforms, respectively, for all differential I/O standards (LVDS and LVPECL).

Figure 4–6. Receiver Input Waveforms for Differential I/O Standards

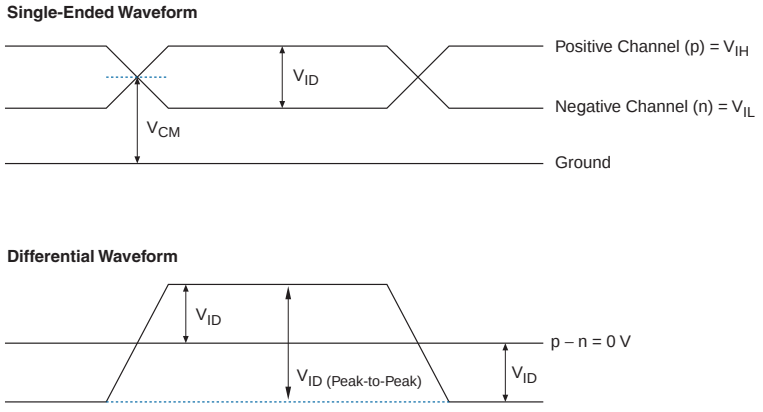


Figure 4–7. Transmitter Output Waveforms for Differential I/O Standards

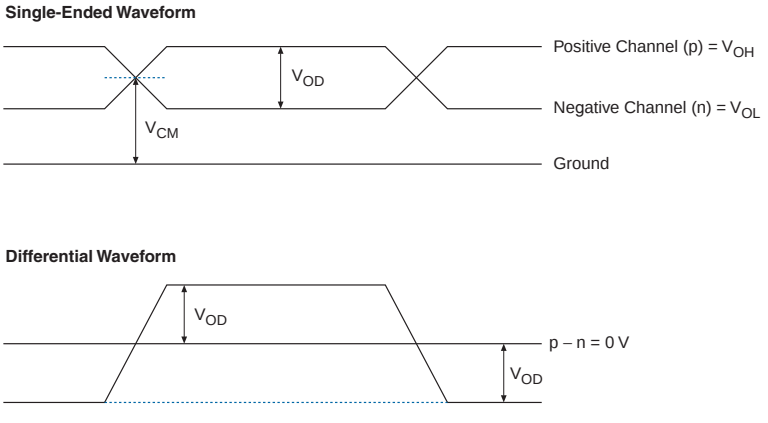


Table 4–46. 1.8-V HSTL Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.71	1.80	1.89	V
V_{REF}	Input reference voltage		0.85	0.90	0.95	V
V_{TT}	Termination voltage		0.85	0.90	0.95	V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 16 mA *(1)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OH} = –16 mA *(1)*			0.4	V

Note to Table 4–46:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Table 4–47. 1.8-V HSTL Class I and II Differential Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage		1.71	1.80	1.89	V
V_{DIF} (DC)	DC input differential voltage		0.2			V
V_{CM} (DC)	DC common mode input voltage		0.78		1.12	V
V_{DIF} (AC)	AC differential input voltage		0.4			V
V_{OX} (AC)	AC differential cross point voltage		0.68		0.9	V

Table 4–55. Stratix II GX Performance Notes (Part 3 of 3) *Note (1)*

Applications		Resources Used			Performance				
		ALUTs	TriMatrix Memory Blocks	DSP Blocks	-3 Speed Grade *(2)*	-3 Speed Grade *(3)*	-4 Speed Grade	-5 Speed Grade	Units
TriMatrix Memory MegaRAM block (cont.)	Single port RAM 64K x 9 bit	0	1	0	364.96	347.22	325.73	271.73	MHz
	Simple dual-port RAM 64K x 9 bit	0	1	0	420.16	400.0	375.93	313.47	MHz
	True dual-port RAM 64K x 9 bit	0	1	0	359.71	342.46	322.58	268.09	MHz
DSP block	9 x 9-bit multiplier *(5)*	0	0	1	430.29	409.16	385.2	320.1	MHz
	18 x 18-bit multiplier *(5)*	0	0	1	410.17	390.01	367.1	305.06	MHz
	18 x 18-bit multiplier *(7)*	0	0	1	450.04	428.08	403.22	335.12	MHz
	36 x 36-bit multiplier *(5)*	0	0	1	250.0	238.15	224.01	186.6	MHz
	36 x 36-bit multiplier *(6)*	0	0	1	410.17	390.01	367.1	305.06	MHz
	18-bit, 4-tap FIR filter	0	0	1	410.17	390.01	367.1	305.06	MHz

Notes to Table 4–55:

(1) These design performance numbers were obtained using the Quartus II software.
(2) This column refers to -3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
(3) This column refers to -3 speed grades for EP2SGX130 devices.
(4) This application uses registered inputs and outputs.
(5) This application uses registered multiplier input and output stages within the DSP block.
(6) This application uses registered multiplier input, pipeline, and output stages within the DSP block.
(7) This application uses registered multiplier inputs with outputs of the multiplier stage feeding the accumulator or subtractor within the DSP block.

Table 4–61. M-RAM Block Internal Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	-3 Speed Grade *(2)*		-3 Speed Grade *(3)*		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{MEGABESU}$	Byte enable setup time before clock	-9		-10		-11		-13		ps
$t_{MEGABEH}$	Byte enable hold time after clock	39		40		43		52		ps
$t_{MEGADATAASU}$	A port data setup time before clock	50		52		55		67		ps
$t_{MEGADATAAH}$	A port data hold time after clock	243		255		271		325		ps
$t_{MEGAADDRASU}$	A port address setup time before clock	589		618		657		789		ps
$t_{MEGAADDRAH}$	A port address hold time after clock	-347		-365		-388		-465		ps
$t_{MEGADATABSU}$	B port setup time before clock	50		52		55		67		ps
$t_{MEGADATABH}$	B port hold time after clock	243		255		271		325		ps
$t_{MEGAADDRBSU}$	B port address setup time before clock	589		618		657		789		ps
$t_{MEGAADDRBH}$	B port address hold time after clock	-347		-365		-388		-465		ps
$t_{MEGADATACO1}$	Clock-to-output delay when using output registers	480	715	480	749	480	797	480	957	ps
$t_{MEGADATACO2}$	Clock-to-output delay without output registers	1950	2899	1950	3042	1950	3235	1950	3884	ps
$t_{MEGACLKL}$	Minimum clock low time	1250		1312		1395		1675		ps
$t_{MEGACLKH}$	Minimum clock high time	1250		1312		1395		1675		ps
$t_{MEGACLR}$	Minimum clear pulse width	144		151		160		192		ps

(1) The M512 block f_{MAX} obtained using the Quartus II software does not necessarily equal to 1/TMEGARC.
(2) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
(3) This column refers to –3 speed grades for EP2SGX130 devices.

Table 4–86. Stratix II GX I/O Output Delay for Column Pins (Part 1 of 7)								
I/O Standard	Drive Strength	Parameter	Fast Corner Industrial/ Commercial	-3 Speed Grade *(3)*	-3 Speed Grade *(4)*	-4 Speed Grade	-5 Speed Grade	Unit
LVTTL	4 mA	t_{OP}	1236	2351	2467	2624	2820	ps
		t_{DIP}	1258	2417	2537	2698	2910	ps
	8 mA	t_{OP}	1091	2036	2136	2272	2448	ps
		t_{DIP}	1113	2102	2206	2346	2538	ps
	12 mA	t_{OP}	1024	2036	2136	2272	2448	ps
		t_{DIP}	1046	2102	2206	2346	2538	ps
	16 mA	t_{OP}	998	1893	1986	2112	2279	ps
		t_{DIP}	1020	1959	2056	2186	2369	ps
	20 mA	t_{OP}	976	1787	1875	1994	2154	ps
		t_{DIP}	998	1853	1945	2068	2244	ps
	24 mA *(1)*	t_{OP}	969	1788	1876	1995	2156	ps
		t_{DIP}	991	1854	1946	2069	2246	ps
LVCMOS	4 mA	t_{OP}	1091	2036	2136	2272	2448	ps
		t_{DIP}	1113	2102	2206	2346	2538	ps
	8 mA	t_{OP}	999	1786	1874	1993	2153	ps
		t_{DIP}	1021	1852	1944	2067	2243	ps
	12 mA	t_{OP}	971	1720	1805	1919	2075	ps
		t_{DIP}	993	1786	1875	1993	2165	ps
	16 mA	t_{OP}	978	1693	1776	1889	2043	ps
		t_{DIP}	1000	1759	1846	1963	2133	ps
	20 mA	t_{OP}	965	1677	1759	1871	2025	ps
		t_{DIP}	987	1743	1829	1945	2115	ps
	24 mA *(1)*	t_{OP}	954	1659	1741	1851	2003	ps
		t_{DIP}	976	1725	1811	1925	2093	ps

Table 4–105. Maximum DCD for DDIO Output on Column I/O Pins With PLL in the Clock Path (Part 2 of 2)			
Maximum DCD (ps) for Column DDIO Output I/O Standard	Stratix II GX Devices (PLL Output Feeding DDIO)		Unit
	-3 Device	-4 and -5 Device	
1.2-V HSTL	155	155	ps
LVPECL	180	180	ps

High-Speed I/O Specifications

Table 4–106 provides high-speed timing specifications definitions.

Table 4–106. High-Speed Timing Specifications and Definitions	
High-Speed Timing Specifications	Definitions
t_C	High-speed receiver/transmitter input and output clock period.
f_{HSCLK}	High-speed receiver/transmitter input and output clock frequency.
J	Deserialization factor (width of parallel data bus).
W	PLL multiplication factor.
t_{RISE}	Low-to-high transmission time.
t_{FALL}	High-to-low transmission time.
Timing unit interval (TUI)	The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency × Multiplication Factor) = t_C/w).
f_{IN}	Fast PLL input clock frequency
f_{HSDR}	Maximum/minimum LVDS data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
$f_{HSDRDPA}$	Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.
Channel-to-channel skew (TCCS)	The timing difference between the fastest and the slowest output edges including t_{CO} variation and clock skew across channels driven by the same fast PLL. The clock is included in the TCCS measurement.
Sampling window (SW)	The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window.
Input jitter	Peak-to-peak input jitter on high-speed PLLs.
Output jitter	Peak-to-peak output jitter on high-speed PLLs.
t_{DUTY}	Duty cycle on high-speed transmitter output clock.
t_{LOCK}	Lock time for high-speed transmitter and receiver PLLs.