Intel - EP2SGX130GF40C5NES Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

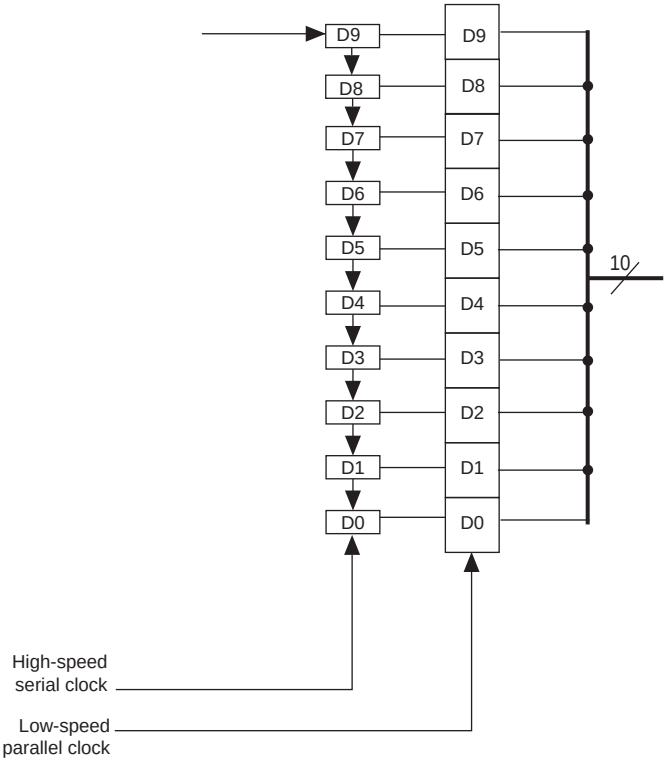
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	6627
Number of Logic Elements/Cells	132540
Total RAM Bits	6747840
Number of I/O	734
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1508-BBGA, FCBGA
Supplier Device Package	1508-FBGA, FC (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2sgx130gf40c5nes

Stratix II GX devices are available in space-saving FineLine BGA packages (refer to Table 1–2). All Stratix II GX devices support vertical migration within the same package. Vertical migration means that you

Figure 2–17. Deserializer Note (1)

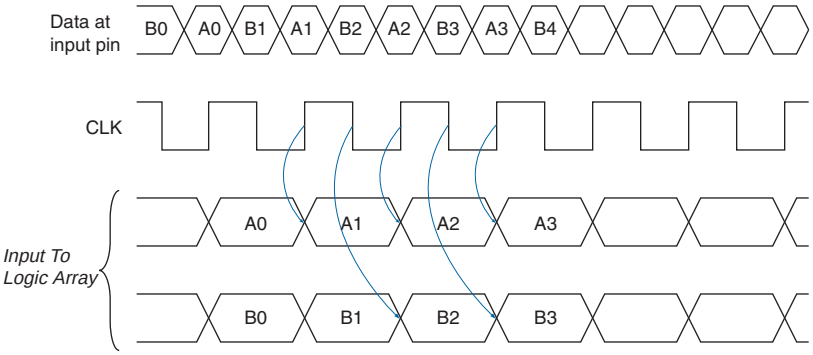


Note to Figure 2–17:
(1) This is a 10-bit deserializer. The deserializer can also convert 8, 16, or 20 bits of data.

Word Aligner

The deserializer block creates 8-, 10-, 16-, or 20-bit parallel data. The deserializer ignores protocol symbol boundaries when converting this data. Therefore, the boundaries of the transferred words are arbitrary. The word aligner aligns the incoming data based on specific byte or word boundaries. The word alignment module is clocked by the local receiver recovered clock during normal operation. All the data and programmed patterns are defined as big-endian (most significant word followed by least significant word). Most-significant-bit-first protocols such as SONET/SDH should reverse the bit order of word align patterns programmed.

Figure 2–83. Input Timing Diagram in DDR Mode



When using the IOE for DDR outputs, the two output registers are configured to clock two data paths from ALMs on rising clock edges. These output registers are multiplexed by the clock to drive the output pin at a ×2 rate. One output register clocks the first bit out on the clock high time, while the other output register clocks the second bit out on the clock low time. Figure 2–84 shows the IOE configured for DDR output. Figure 2–85 shows the DDR output timing diagram.

The bus-hold circuitry also pulls undriven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. You can select this feature individually for each I/O pin. The bus-hold output drives no higher than V_{CCIO} to prevent overdriving signals. If the bus-hold feature is enabled, the programmable pull-up option cannot be used. Disable the bus-hold feature when the I/O pin has been configured for differential signals.

The bus-hold circuitry uses a resistor with a nominal resistance (RBH) of approximately 7 k to pull the signal level to the last-driven state.

f Refer to the DC & Switching Characteristics chapter in volume 1 of the Stratix II GX Device Handbook for the specific sustaining current driven through this resistor and overdrive current used to identify the next-driven input level. This information is provided for each V_{CCIO} voltage level.

The bus-hold circuitry is active only after configuration. When going into user mode, the bus-hold circuit captures the value on the pin present at the end of configuration.

Programmable Pull-Up Resistor

Each Stratix II GX device I/O pin provides an optional programmable pull-up resistor during user mode. If you enable this feature for an I/O pin, the pull-up resistor (typically 25 k) holds the output to the V_{CCIO} level of the output pin's bank.

Programmable pull-up resistors are only supported on user I/O pins and are not supported on dedicated configuration pins, JTAG pins, or dedicated clock pins.

Advanced I/O Standard Support

The Stratix II GX device IOEs support the following I/O standards:

- 3.3-V LVTTL/LVCMOS
- 2.5-V LVTTL/LVCMOS
- 1.8-V LVTTL/LVCMOS
- 1.5-V LVCMOS
- 3.3-V PCI
- 3.3-V PCI-X mode 1
- LVDS
- LVPECL (on input and output clocks only)
- Differential 1.5-V HSTL class I and II
- Differential 1.8-V HSTL class I and II
- Differential SSTL-18 class I and II

Table 4–21. PCS Latency (Part 2 of 2) Note (1)

Functional Mode	Configuration	Transmitter PCS Latency					
		TX PIPE	TX Phase Comp FIFO	Byte Serializer	TX State Machine	8B/10B Encoder	Sum (2)
Serial RapidIO	1.25 Gbps, 2.5 Gbps, 3.125 Gbps	-	2-3	1	-	0.5	4-5
SDI	HD 10-bit channel width	-	2-3	1	-	1	4-5
	HD, 3G 20-bit channel width	-	2-3	1	-	0.5	4-5
BASIC Single Width	8-bit/10-bit channel width	-	2-3	1	-	1	4-5
	16-bit/20-bit channel width	-	2-3	1	-	0.5	4-5
BASIC Double Width	16-bit/20-bit channel width	-	2-3	1	-	1	4-5
	32-bit/40-bit channel width	-	2-3	1	-	0.5	4-5
	Parallel Loopback/ BIST	-	2-3	1	-	1	4-5

Notes to Table 4–21:

(1) The latency numbers are with respect to the PLD-transceiver interface clock cycles.

(2) The total latency number is rounded off in the Sum column.

(3) For CPRI 614 Mbps and 1.228 Gbps data rates, the Quartus II software customizes the PLD-transceiver interface clocking to achieve zero clock cycle uncertainty in the transmitter phase compensation FIFO latency. For more details, refer to the *CPRI Mode* section in the *Stratix II GX Transceiver Architecture Overview* chapter in volume 2 of the *Stratix II GX Device Handbook*.

Table 4–102. Maximum DCD for DDIO Output on Column I/O Pins Without PLL in the Clock Path for -3 Devices (Part 2 of 2) Note 1

Maximum DCD (ps) for DDIO Column Output I/O Standard	Input IO Standard (No PLL in the Clock Path)					Unit
	TTL/CMOS		SSTL-2	SSTL/HSTL	HSTL12	
	3.3/2.5V	1.8/1.5V	2.5V	1.8/1.5V	1.2V	
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(1) Table 4–102assumes the input clock has zero DCD.

Table 4–103. Maximum DCD for DDIO Output on Column I/O Pins Without PLL in the Clock Path for -4 and -5 Devices Note 1

Maximum DCD (ps) for DDIO Column Output I/O Standard	Input IO Standard (No PLL in the Clock Path)				Unit
	TTL/CMOS		SSTL-2	SSTL/HSTL	
	3.3/2.5V	1.8/1.5V	2.5V	1.8/1.5V	
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(1) Table 4–103assumes the input clock has zero DCD.