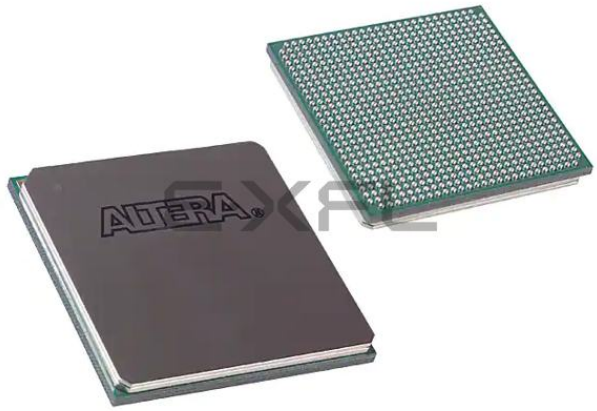

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1694
Number of Logic Elements/Cells	33880
Total RAM Bits	1369728
Number of I/O	361
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	780-BBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2sgx30cf780c3n

Control and Status Signals

The rx_enapatternalign signal is the FPGA control signal that enables word alignment in non-automatic modes. The rx_enapatternalign signal is not used in automatic modes (PCI Express, XAUI, GIGE, CPRI, and Serial RapidIO).

In manual alignment mode, after the rx_enapatternalign signal is activated, the rx_syncstatus signal goes high for one parallel clock cycle to indicate that the alignment pattern has been detected and the word boundary has been locked. If the rx_enapatternalign is deactivated, the rx_syncstatus signal acts as a re-synchronization signal to signify that the alignment pattern has been detected but not locked on a different word boundary.

When using the synchronization state machine, the rx_syncstatus signal indicates the link status. If the rx_syncstatus signal is high, link synchronization is achieved. If the rx_syncstatus signal is low, synchronization has not yet been achieved, or there were enough code group errors to lose synchronization.

In some modes, the rx_enapatternalign signal can be configured to operate as a rising edge signal.

For more information on manual alignment modes, refer to the *Stratix II GX Device Handbook*, volume 2.

When the rx_enapatternalign signal is sensitive to the rising edge, each rising edge triggers a new boundary alignment search, clearing the rx_syncstatus signal.

The rx_patterndetect signal pulses high during a new alignment, and also whenever the alignment pattern occurs on the current word boundary.

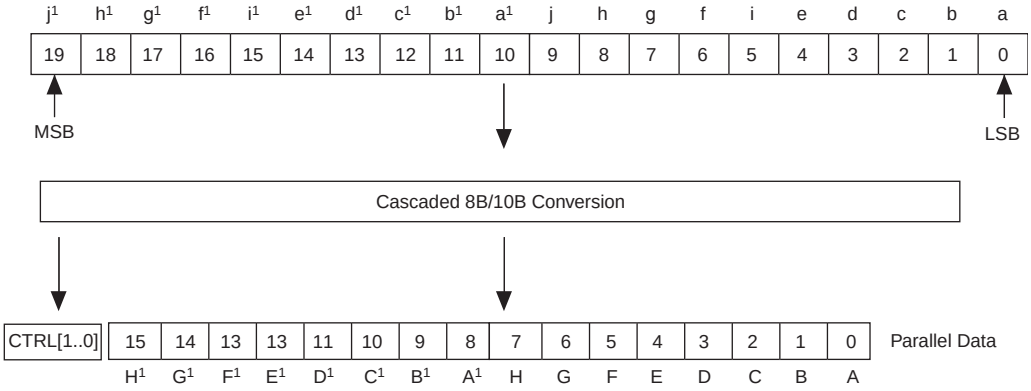
SONET/SDH

In all the SONET/SDH modes, you can configure the word aligner to either align to A1A2 or A1A1A2A2 patterns. Once the pattern is found, the word boundary is aligned and the word aligner asserts the rx_patterndetect signal for one clock cycle.

asserted. All 8B/10B control signals, such as disparity error or control detect, are pipelined with the data in the Stratix II GX receiver block and are edge aligned with the data.

Figure 2–23 shows how the 20-bit code is decoded to the 16-bit data + 2-bit control indicator.

Figure 2–23. 20-Bit to 16-Bit Decoding Process



There are two optional error status ports available in the 8B/10B decoder, `rx_errdetect` and `rx_disperr`. These status signals are aligned with the code group in which the error occurred.

Receiver State Machine

The receiver state machine operates in Basic, GIGE, PCI Express, and XAUI modes. In GIGE mode, the receiver state machine replaces invalid code groups with K30.7. In XAUI mode, the receiver state machine translates the XAUI PCS code group to the XAUI XGMII code group.

Byte Deserializer

The byte deserializer widens the transceiver data path before the FPGA interface. This reduces the rate at which the received data needs to be clocked at in the FPGA logic. The byte deserializer block is available in both single- and double-width modes.

The byte deserializer converts the one- or two-byte interface into a two- or four-byte-wide data path from the transceiver to the FPGA logic (see Table 2–9). The FPGA interface has a limit of 250 MHz, so the byte deserializer is needed to widen the bus width at the FPGA interface and

Table 2–16. Reset Signal Map to Stratix II GX Blocks

Reset Signal	Transmitter Phase Compensation FIFO Module/ Byte Serializer	Transmitter 8B/10B Encoder	Transmitter Serializer	Transmitter Analog Circuits	Transmitter PLL	Transmitter XAUI State Machine	BIST Generators	Receiver Deserializer	Receiver Word Aligner	Receiver Deskew FIFO Module	Receiver Rate Matcher	Receiver 8B/10B Decoder	Receiver Phase Comp FIFO Module/ Byte Deserializer	Receiver PLL / CRU	Receiver XAUI State Machine	BIST Verifiers	Receiver Analog Circuits
rx_digitalreset									✓	✓	✓	✓	✓		✓	✓	
rx_analogreset								✓						✓			✓
tx_digitalreset	✓	✓				✓	✓										
gxb_powerdown	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
gxb_enable	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Voltage Reference Capabilities

Stratix II GX transceivers provide voltage reference and bias circuitry. To set up internal bias for controlling the transmitter output driver voltage swings, as well as to provide voltage and current biasing for other analog circuitry, the device uses an internal bandgap voltage reference of 0.7 V. An external 2-KΩ resistor connected to ground generates a constant bias current (independent of power supply drift, process changes, or temperature variation). An on-chip resistor generates a tracking current that tracks on-chip resistor variation. These currents are mirrored and distributed to the analog circuitry in each channel.

For more information, refer to the *DC and Switching Characteristics* chapter in volume 1 of the *Stratix II GX Handbook*.

M4K RAM Blocks

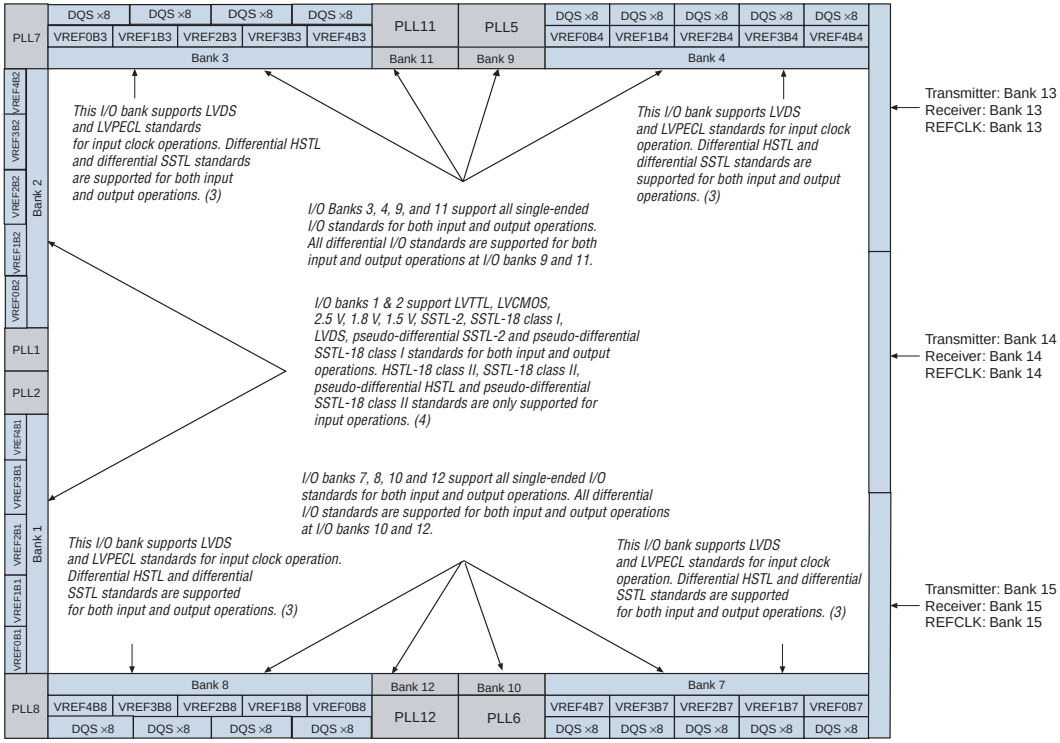
The M4K RAM block includes support for true dual-port RAM. The M4K RAM block is used to implement buffers for a wide variety of applications such as storing processor code, implementing lookup schemes, and implementing larger memory applications. Each block contains 4,608 RAM bits (including parity bits). M4K RAM blocks can be configured in the following modes:

- True dual-port RAM
- Simple dual-port RAM
- Single-port RAM
- FIFO
- ROM
- Shift register

When configured as RAM or ROM, you can use an initialization file to pre-load the memory contents.

The M4K RAM blocks allow for different clocks on their inputs and outputs. Either of the two clocks feeding the block can clock M4K RAM block registers (`renwe`, `address`, `byte enable`, `datain`, and `output` registers). Only the `output` register can be bypassed. The six `labclk` signals or local interconnects can drive the control signals for the A and B ports of the M4K RAM block. ALMs can also control the `clock_a`, `clock_b`, `renwe_a`, `renwe_b`, `clr_a`, `clr_b`, `clocken_a`, and `clocken_b` signals, as shown in Figure 2–51.

Figure 2–87. Stratix II GX I/O Banks *Notes (1), (2)*



Notes to Figure 2–87:

(1) Figure 2–87 is a top view of the silicon die that corresponds to a reverse view for flip-chip packages. It is a graphical representation only.

(2) Depending on the size of the device, different device members have different numbers of V_{REF} groups. Refer to the pin list and the Quartus II software for exact locations.

(3) Banks 9 through 12 are enhanced PLL external clock output banks.

(4) Horizontal I/O banks feature SERDES and DPA circuitry for high-speed differential I/O standards. See the *High-Speed Differential I/O Interfaces with DPA in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook 2* for more information on differential I/O standards.

Each I/O bank has its own VCCIO pins. A single device can support 1.5-, 1.8-, 2.5-, and 3.3-V interfaces; each bank can support a different V_{CCIO} level independently. Each bank also has dedicated VREF pins to support the voltage-referenced standards (such as SSTL-2).

Each I/O bank can support multiple standards with the same V_{CCIO} for input and output pins. Each bank can support one V_{REF} voltage level. For example, when V_{CCIO} is 3.3 V, a bank can support LVTTL, LVCMOS, and 3.3-V PCI for inputs and outputs.

For more information on tolerance specifications for differential on-chip termination, refer to the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II GX Device Handbook*.

On-Chip Series Termination without Calibration

Stratix II GX devices support driver impedance matching to provide the I/O driver with controlled output impedance that closely matches the impedance of the transmission line. As a result, reflections can be significantly reduced. Stratix II GX devices support on-chip series termination for single-ended I/O standards with typical R_S values of 25 and 50 Ω. Once matching impedance is selected, current drive strength is no longer selectable. Table 2–34 shows the list of output standards that support on-chip series termination without calibration.

For more information about series on-chip termination supported by Stratix II GX devices, refer to the *Selectable I/O Standards in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook*.

For more information about tolerance specifications for on-chip termination without calibration, refer to the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II GX Device Handbook*.

On-Chip Series Termination with Calibration

Stratix II GX devices support on-chip series termination with calibration in column I/O pins in top and bottom banks. There is one calibration circuit for the top I/O banks and one circuit for the bottom I/O banks. Each on-chip series termination calibration circuit compares the total impedance of each I/O buffer to the external 25-Ω or 50-Ω resistors connected to the `RUP` and `RDN` pins, and dynamically enables or disables the transistors until they match. Calibration occurs at the end of device configuration. Once the calibration circuit finds the correct impedance, it powers down and stops changing the characteristics of the drivers.

For more information about series on-chip termination supported by Stratix II GX devices, refer to the *Selectable I/O Standards in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook*.

For more information about tolerance specifications for on-chip termination with calibration, refer to the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Table 2–42. Document Revision History (Part 4 of 6)

Date and Document Version	Changes Made	Summary of Changes
	Updated: ● "Transmitter PLLs" ● "Transmitter Phase Compensation FIFO Buffer" ● "8B/10B Encoder" ● "Byte Serializer" ● "Programmable Output Driver" ● "Receiver PLL & CRU" ● "Programmable Pre-Emphasis" ● "Receiver Input Buffer" ● "Control and Status Signals" ● "Programmable Run Length Violation" ● "Channel Aligner" ● "Basic Mode" ● "Byte Ordering Block" ● "Receiver Phase Compensation FIFO Buffer" ● "Loopback Modes" ● "Serial Loopback" ● "Parallel Loopback" ● "Regional Clock Network" ● "MultiVolt I/O Interface" ● "High-Speed Differential I/O with DPA Support"	
	Updated bulleted lists at the beginning of the "Transceivers" section.	
	Added reference to the "Transmit Buffer" section.	
	Deleted the Programmable V_{OD} table from the "Programmable Output Driver" section.	
	Changed "PLD Interface" heading to "Parallel Data Width" heading in Table 2–14.	
	Deleted "Global & Regional Clock Connections from Right Side Clock Pins & Fast PLL Outputs" table.	
	Updated notes to Tables 2–29 and 2–37.	
	Updated notes to Figures 2–72, 2–73 and 2–74.	
	Updated bulleted list in the "Advanced I/O Standard Support" section.	

The Stratix II GX device instruction register length is 10 bits and the USERCODE register length is 32 bits. Tables 3–2 and 3–3 show the boundary-scan register length and device IDCODE information for Stratix II GX devices.

Table 3–2. Stratix II GX Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EP2SGX30	1,320
EP2SGX60	1,506
EP2SGX90	2,016
EP2SGX130	2,454

Table 3–3. 32-Bit Stratix II GX Device IDCODE

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	LSB (1 Bit)
EP2SGX30	0000	0010 0000 1110 0001	000 0110 1110	1
EP2SGX60	0000	0010 0000 1110 0010	000 0110 1110	1
EP2SGX90	0000	0010 0000 1110 0011	000 0110 1110	1
EP2SGX130	0000	0010 0000 1110 0100	000 0110 1110	1

SignalTap II Embedded Logic Analyzer

Stratix II GX devices feature the SignalTap II embedded logic analyzer, which monitors design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry. You can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages, such as FineLine BGA packages, because it can be difficult to add a connection to a pin during the debugging process after a board is designed and manufactured.

Configuration

The logic, circuitry, and interconnects in the Stratix II GX architecture are configured with CMOS SRAM elements. Altera® FPGAs are reconfigurable and every device is tested with a high coverage production test program so you do not have to perform fault testing and can instead focus on simulation and design verification.

Stratix II GX devices are configured at system power-up with data stored in an Altera configuration device or provided by an external controller (for example, a MAX® II device or microprocessor). You can configure Stratix II GX devices using the fast passive parallel (FPP), active serial

Referenced Documents

This chapter references the following documents:

- *AN 357: Error Detection Using CRC in Altera FPGA Devices*
- *AN 414: An Embedded Solution for PLD JTAG Configuration*
- *AN 418 SRunner: An Embedded Solution for Serial Configuration Device Programming*
- *Configuring Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook*
- *Configuring the MicroBlaster Fast Passive Parallel Software Driver White Paper*
- *Configuring the MicroBlaster Passive Serial Software Driver White Paper*
- *MorphIO: An I/O Reconfiguration Solution for Altera Devices White Paper*
- *PLLs in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook*
- *Remote System Upgrades with Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook*
- *Serial Configuration Devices (EPCS1, EPCS4, EPCS64, and EPCS128) Data Sheet* in the *Configuration Handbook*
- *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Document Revision History

Table 3–6 shows the revision history for this chapter.

Table 3–6. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
October 2007 v1.4	Minor text edits.	—
August 2007 v1.3	Updated the note in the "IEEE Std. 1149.1 JTAG Boundary-Scan Support"	—
	Updated Table 3–3.	—
	Added the "Referenced Documents" section.	—
May 2007 v1.2	Updated the "Temperature Sensing Diode (TSD)" section.	—
February 2007 v1.1	Added the "Document Revision History" section to this chapter.	Added support information for the Stratix II GX device.
October 2005 v1.0	Added chapter to the *Stratix II GX Device Handbook*.	—

Table 4–6. Stratix II GX Transceiver Block AC Specification (Part 4 of 6)

Symbol / Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Bandwidth at 3.125 Gbps	BW = Low	-	30	-	-	30	-	-	30	-	MHz
	BW = Med	-	40	-	-	40	-	-	40	-	MHz
	BW = High	-	50	-	-	50	-	-	50	-	MHz
Bandwidth at 2.5 Gbps	BW = Low	-	35	-	-	35	-	-	35	-	MHz
	BW = Med	-	50	-	-	50	-	-	50	-	MHz
	BW = High	-	60	-	-	60	-	-	60	-	MHz
Return loss differential mode		100 MHz to 2.5 GHz (XAUI): -10 dB 50 MHz to 1.25 GHz (PCI-E): -10 dB 100 MHz to 4.875 GHz (OIF/CEI): -8dB 4.875 GHz to 10 GHz (OIF/CEI): 16.6 dB/decade slope									
Return loss common mode		100 MHz to 2.5 GHz (XAUI): -6 dB 50 MHz to 1.25 GHz (PCI-E): -6 dB 100 MHz to 4.875 GHz (OIF/CEI): -6dB 4.875 GHz to 10 GHz (OIF/CEI): 16.6 dB/decade slope									
Programmable PPM detector *(2)*		±62.5, 100, 125, 200, 250, 300, 500, 1000			±62.5, 100, 125, 200, 250, 300, 500, 1000			±62.5, 100, 125, 200, 250, 300, 500, 1000			ppm
Run length *(3)*, *(9)*		80			80			80			UI
Programmable equalization		-	-	16	-	-	16	-	-	16	dB
Signal detect/loss threshold *(4)*		65	-	175	65	-	175	65	-	175	mV
CDR LTR TIme *(5)*, *(9)*		-	-	75	-	-	75	-	-	75	us
CDR Minimum T1b *(6)*, *(9)*		15	-	-	15	-	-	15	-	-	us
LTD lock time *(7)*, *(9)*		0	100	4000	0	100	4000	0	100	4000	ns
Data lock time from `rx_freqlocked` *(8)*, *(9)*		-	-	4	-	-	4	-	-	4	us
Programmable DC gain		0, 3, 6			0, 3, 6			0, 3, 6			dB
Transmitter											

Figure 4–4. Transmitter Output Waveform

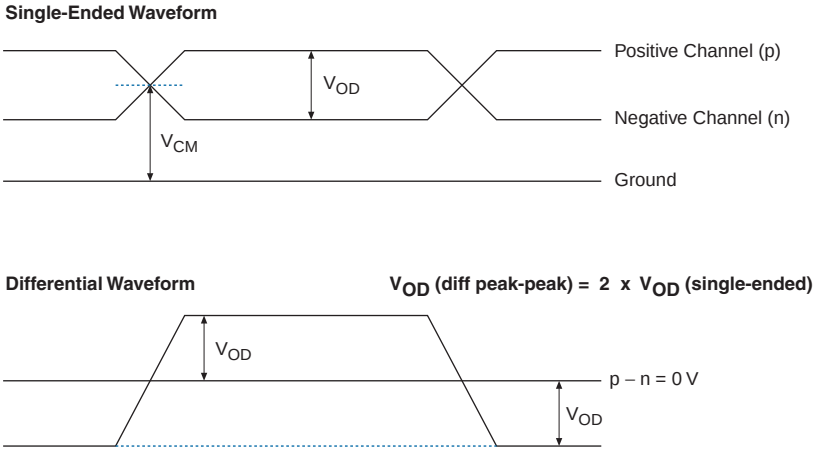
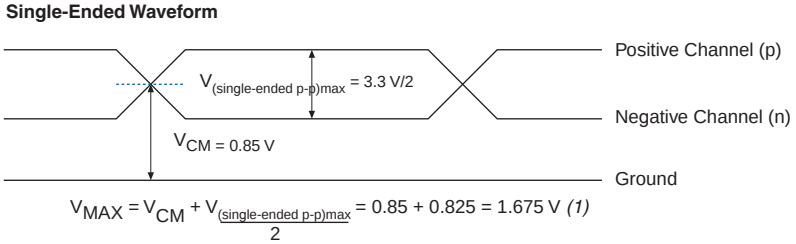


Figure 4–5. Maximum Receiver Input Pin Voltage



Note to Figure 4–5:
(1) The absolute V_{MAX} that the receiver input pins can tolerate is 2 V.

Tables 4–7 through 4–12 show the typical V_{OD} for data rates from 600 Mbps to 6.375 Gbps. The specification is for measurement at the package ball.

Table 4–7. Typical V_{OD} Setting, TX Term = 100 Ω Note (1)

V_{CCH} TX = 1.5 V	V_{OD} Setting (mV)						
	200	400	600	800	1000	1200	1400
V_{OD} Typical (mV)	220	430	625	830	1020	1200	1350

Note to Table 4–7:
(1) Applicable to data rates from 600 Mbps to 6.375 Gbps. Specification is for measurement at the package ball.

Table 4–19 shows the Stratix II GX transceiver block AC specifications.

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 1 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SONET/SDH Transmit Jitter Generation *(7)*											
Peak-to-peak jitter at 622.08 Mbps	REFCLK = 77.76 MHz Pattern = PRBS23 V_{OD} = 800 mV No Pre-emphasis	-	-	0.1	-	-	0.1	-	-	0.1	UI
RMS jitter at 622.08 Mbps	REFCLK = 77.76 MHz Pattern = PRBS23 V_{OD} = 800 mV No Pre-emphasis	-	-	0.01	-	-	0.01	-	-	0.01	UI
Peak-to-peak jitter at 2488.32 Mbps	REFCLK = 155.52 MHz Pattern = PRBS23 V_{OD} = 800 mV No Pre-emphasis	-	-	0.1	-	-	0.1	-	-	0.1	UI
RMS jitter at 2488.32 Mbps	REFCLK = 155.52 MHz Pattern = PRBS23 V_{OD} = 800 mV No Pre-emphasis	-	-	0.01	-	-	0.01	-	-	0.01	UI

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 5 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Peak-to-peak jitter	Jitter frequency = 22.1 KHz		> 8.5			> 8.5			> 8.5		UI
Peak-to-peak jitter	Jitter frequency = 1.875 MHz		> 0.1			> 0.1			> 0.1		UI
Peak-to-peak jitter	Jitter frequency = 20 MHz		> 0.1			> 0.1			> 0.1		UI
PCI Express Transmit Jitter Generation *(10)*											
Total jitter at 2.5 Gbps	Compliance pattern V_{OD} = 800 mV Pre-emphasis (1st post-tap) = Setting 5	-	-	0.25	-	-	0.25	-	-	0.25	UI
PCI Express Receiver Jitter Tolerance *(10)*											
Total jitter at 2.5 Gbps	Compliance pattern No Equalization DC gain = 3 dB		> 0.6			> 0.6			> 0.6		UI
Serial RapidIO Transmit Jitter Generation *(11)*											
Deterministic Jitter (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps REFCLK = 125 MHz Pattern = CJPAT V_{OD} = 800 mV No Pre-emphasis	-	-	0.17	-	-	0.17	-	-	0.17	UI
Total Jitter (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps REFCLK = 125 MHz Pattern = CJPAT V_{OD} = 800 mV No Pre-emphasis	-	-	0.35	-	-	0.35	-	-	0.35	UI

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 10 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Sinusoidal Jitter Tolerance (peak-to-peak)	Jitter Frequency = 1.875 MHz Data Rate = 3.75 Gbps REFCLK = 187.5 MHz Pattern = CJPAT No Equalization DC Gain = 3 dB	> 0.1			-			-			UI
	Jitter Frequency = 20 MHz Data Rate = 3.75 Gbps REFCLK = 187.5 MHz Pattern = CJPAT No Equalization DC Gain = 3 dB	> 0.1			-			-			UI
(OIF) CEI Transmitter Jitter Generation *(14)*											
Total Jitter (peak-to-peak)	Data Rate = 6.375 Gbps REFCLK = 318.75 MHz Pattern = PRBS15 Vod=1000 mV *(5)* No Pre-emphasis BER = 10^{-12}			0.3			N/A			N/A	UI
(OIF) CEI Receiver Jitter Tolerance *(14)*											
Deterministic Jitter Tolerance (peak-to-peak)	Data Rate = 6.375 Gbps Pattern = PRBS31 Equalizer Setting = 15 DC Gain = 0 dB BER = 10^{-12}	> 0.675			N/A			N/A			UI

Table 4–54. Timing Measurement Methodology for Input Pins (Part 2 of 2) *Notes (1), (2), (3), (4)*

I/O Standard	Measurement Conditions			Measurement Point
	V_{CCIO} (V)	V_{REF} (V)	Edge Rate (ns)	VMEAS (V)
1.8-V HSTL Class II	1.660	0.830	1.660	0.83
1.5-V HSTL Class I	1.375	0.688	1.375	0.6875
1.5-V HSTL Class II	1.375	0.688	1.375	0.6875
1.2-V HSTL with OCT	1.140	0.570	1.140	0.570
Differential SSTL-2 Class I	2.325	1.163	2.325	1.1625
Differential SSTL-2 Class II	2.325	1.163	2.325	1.1625
Differential SSTL-18 Class I	1.660	0.830	1.660	0.83
Differential SSTL-18 Class II	1.660	0.830	1.660	0.83
1.5-V differential HSTL Class I	1.375	0.688	1.375	0.6875
1.5-V differential HSTL Class II	1.375	0.688	1.375	0.6875
1.8-V differential HSTL Class I	1.660	0.830	1.660	0.83
1.8-V differential HSTL Class II	1.660	0.830	1.660	0.83
LVDS	2.325		0.100	1.1625
LVPECL	3.135		0.100	1.5675

Notes to Table 4–54:

(1) Input buffer sees no load at buffer input.
(2) Input measuring point at buffer input is 0.5 V_{CCIO}.
(3) Output measuring point is 0.5 V_{CC} at internal node.
(4) Input edge rate is 1 V/ns.
(5) Less than 50-mV ripple on V_{CCIO} and V_{CCPD}, V_{CCINT} = 1.15 V with less than 30-mV ripple.
(6) V_{CCPD} = 2.97 V, less than 50-mV ripple on V_{CCIO} and V_{CCPD}, V_{CCINT} = 1.15 V.

Table 4–58. DSP Block Internal Timing Microparameters (Part 2 of 2)

Symbol	Parameter	-3 Speed Grade (1)		-3 Speed Grade (2)		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{INREG2PIPE9}$	Input register to DSP block pipeline register in 9 × 9-bit mode	1312	2030	1312	2131	1312	2266	1312	2720	ps
$t_{INREG2PIPE18}$	Input register to DSP block pipeline register in 18 × 18-bit mode	1302	2010	1302	2110	1302	2244	1302	2693	ps
$t_{INREG2PIPE36}$	Input register to DSP block pipeline register in 36 × 36-bit mode	1302	2010	1302	2110	1302	2244	1302	2693	ps
$t_{PIPE2OUTREG2ADD}$	DSP block pipeline register to output register delay in two-multipliers adder mode	924	1450	924	1522	924	1618	924	1943	ps
$t_{PIPE2OUTREG4ADD}$	DSP block pipeline register to output register delay in four-multipliers adder mode	1134	1850	1134	1942	1134	2065	1134	2479	ps
t_{PD9}	Combinational input to output delay for 9 × 9	2100	2880	2100	3024	2100	3214	2100	3859	ps
t_{PD18}	Combinational input to output delay for 18 × 18	2110	2990	2110	3139	2110	3337	2110	4006	ps
t_{PD36}	Combinational input to output delay for 36 × 36	2939	4450	2939	4672	2939	4967	2939	5962	ps
t_{CLR}	Minimum clear pulse width	2212		2322		2469		2964		ps
t_{CLKL}	Minimum clock low time	1190		1249		1328		1594		ps
t_{CLKH}	Minimum clock high time	1190		1249		1328		1594		ps

(1) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
(2) This column refers to –3 speed grades for EP2SGX130 devices.

Table 4–60. M4K Block Internal Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	-3 Speed Grade *(2)*		-3 Speed Grade *(3)*		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{M4KDATABH}$	B port data hold time after clock	203		213		226		272		ps
$t_{M4KRADDRBSU}$	B port address setup time before clock	22		23		24		29		ps
$t_{M4KRADDRBH}$	B port address hold time after clock	203		213		226		272		ps
$t_{M4KDATACO1}$	Clock-to-output delay when using output registers	334	524	334	549	334	584	334	701	ps
$t_{M4KDATACO2}$	Clock-to-output delay without output registers	1616	2453	1616	2574	1616	2737	1616	3286	ps
$t_{M4KCLKH}$	Minimum clock high time	1250		1312		1395		1675		ps
$t_{M4KCLKL}$	Minimum clock low time	1250		1312		1395		1675		ps
t_{M4KCLR}	Minimum clear pulse width	144		151		160		192		ps

(1) The M512 block f_{MAX} obtained using the Quartus II software does not necessarily equal to 1/TM4KRC.
(2) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
(3) This column refers to –3 speed grades for EP2SGX130 devices.

Table 4–61. M-RAM Block Internal Timing Microparameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	-3 Speed Grade *(2)*		-3 Speed Grade *(3)*		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{MEGARC}	Synchronous read cycle time	1866	2774	1866	2911	1866	3096	1866	3716	ps
$t_{MEGAWERESU}$	Write or read enable setup time before clock	144		151		160		192		ps
$t_{MEGAWEREH}$	Write or read enable hold time after clock	39		40		43		52		ps

Table 4–61. M-RAM Block Internal Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	-3 Speed Grade *(2)*		-3 Speed Grade *(3)*		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{MEGABESU}$	Byte enable setup time before clock	-9		-10		-11		-13		ps
$t_{MEGABEH}$	Byte enable hold time after clock	39		40		43		52		ps
$t_{MEGADATAASU}$	A port data setup time before clock	50		52		55		67		ps
$t_{MEGADATAAH}$	A port data hold time after clock	243		255		271		325		ps
$t_{MEGAADDRASU}$	A port address setup time before clock	589		618		657		789		ps
$t_{MEGAADDRAH}$	A port address hold time after clock	-347		-365		-388		-465		ps
$t_{MEGADATABSU}$	B port setup time before clock	50		52		55		67		ps
$t_{MEGADATABH}$	B port hold time after clock	243		255		271		325		ps
$t_{MEGAADDRBSU}$	B port address setup time before clock	589		618		657		789		ps
$t_{MEGAADDRBH}$	B port address hold time after clock	-347		-365		-388		-465		ps
$t_{MEGADATACO1}$	Clock-to-output delay when using output registers	480	715	480	749	480	797	480	957	ps
$t_{MEGADATACO2}$	Clock-to-output delay without output registers	1950	2899	1950	3042	1950	3235	1950	3884	ps
$t_{MEGACLKL}$	Minimum clock low time	1250		1312		1395		1675		ps
$t_{MEGACLKH}$	Minimum clock high time	1250		1312		1395		1675		ps
$t_{MEGACLR}$	Minimum clear pulse width	144		151		160		192		ps

(1) The M512 block f_{MAX} obtained using the Quartus II software does not necessarily equal to 1/TMEGARC.
(2) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
(3) This column refers to –3 speed grades for EP2SGX130 devices.

Table 4–86. Stratix II GX I/O Output Delay for Column Pins (Part 4 of 7)								
I/O Standard	**Drive Strength**	**Parameter**	**Fast Corner Industrial/ Commercial**	**-3 Speed Grade** *(3)*	**-3 Speed Grade** *(4)*	**-4 Speed Grade**	**-5 Speed Grade**	**Unit**
1.8-V HSTL Class I	4 mA	t_{OP}	956	1608	1687	1794	1943	ps
		t_{DIP}	978	1674	1757	1868	2033	ps
	6 mA	t_{OP}	962	1595	1673	1779	1928	ps
		t_{DIP}	984	1661	1743	1853	2018	ps
	8 mA	t_{OP}	940	1586	1664	1769	1917	ps
		t_{DIP}	962	1652	1734	1843	2007	ps
	10 mA	t_{OP}	944	1591	1669	1775	1923	ps
		t_{DIP}	966	1657	1739	1849	2013	ps
	12 mA *(1)*	t_{OP}	936	1585	1663	1768	1916	ps
		t_{DIP}	958	1651	1733	1842	2006	ps
1.8-V HSTL Class II	16 mA	t_{OP}	919	1385	1453	1545	1680	ps
		t_{DIP}	941	1451	1523	1619	1770	ps
	18 mA	t_{OP}	921	1394	1462	1555	1691	ps
		t_{DIP}	943	1460	1532	1629	1781	ps
	20 mA *(1)*	t_{OP}	921	1402	1471	1564	1700	ps
		t_{DIP}	943	1468	1541	1638	1790	ps
1.5-V HSTL Class I	4 mA	t_{OP}	956	1607	1686	1793	1942	ps
		t_{DIP}	978	1673	1756	1867	2032	ps
	6 mA	t_{OP}	961	1588	1666	1772	1920	ps
		t_{DIP}	983	1654	1736	1846	2010	ps
	8 mA	t_{OP}	943	1590	1668	1774	1922	ps
		t_{DIP}	965	1656	1738	1848	2012	ps
	10 mA	t_{OP}	943	1592	1670	1776	1924	ps
		t_{DIP}	965	1658	1740	1850	2014	ps
	12 mA *(1)*	t_{OP}	937	1590	1668	1774	1922	ps
		t_{DIP}	959	1656	1738	1848	2012	ps

Table 4–118. Document Revision History (Part 2 of 5)		
Date and Document Version	**Changes Made**	**Summary of Changes**
August 2007 v4.4	Removed note “The data in this table is preliminary. Altera will provide a report upon completion of characterization of the Stratix II GX devices. Conditions for testing the silicon have not been determined.” from each table.	
	Removed note “The data in Tables xxx through xxx is preliminary. Altera will provide a report upon completion of characterization of the Stratix II GX devices. Conditions for testing the silicon have not been determined.” in the clock timing parameters sections.	
	Updated clock timing parameter Tables 4–63 through 4–78 (Table 4–75 was unchanged).	
	Updated Table 4–21 and added new Table 4–22.	
	Updated: ● Table 4–6 ● Table 4–16 ● Table 4–19 ● Table 4–49 ● Table 4–52 ● Table 4–107	
	Added note to Table 4–50.	
	Added: ● Figure 4–3 ● Figure 4–4 ● Figure 4–5	
	Added the “Referenced Documents” section.	
May 2007 v4.3	Changed 1.875 KHz to 1.875 MHz in Table 4–19, XAUI Receiver Jitter Tolerance section.	