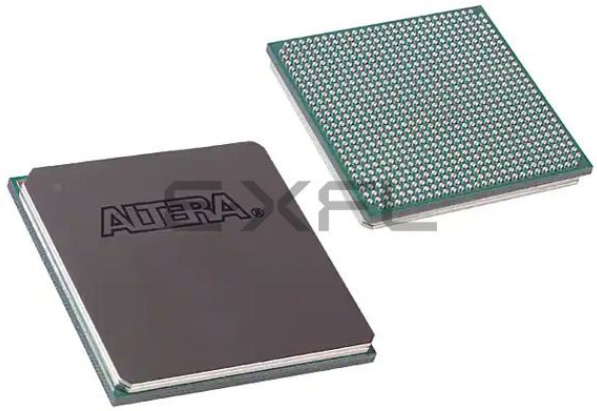

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

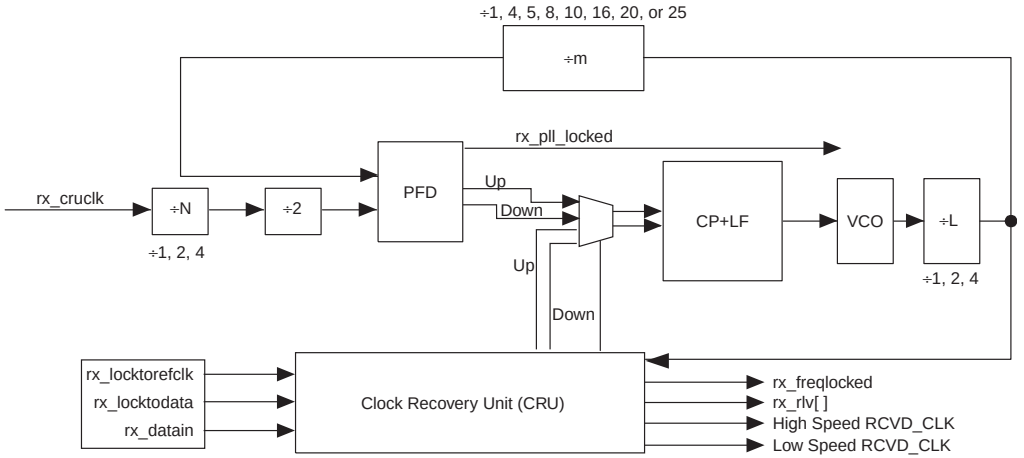
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1694
Number of Logic Elements/Cells	33880
Total RAM Bits	1369728
Number of I/O	361
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	780-BBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2sgx30cf780c4

Figure 2–16. Receiver PLL and CRU



The receiver PLLs and CRUs can support frequencies up to 6.375 Gbps. The input clock frequency is limited to the full clock range of 50 to 622 MHz but only when using `REFCLK0` or `REFCLK1`. An optional `RX_PLL_LOCKED` port is available to indicate whether the PLL is locked to the reference clock. The receiver PLL has a programmable loop bandwidth which can be set to low, medium, or high. The Quartus II software can statically set the loop bandwidth parameter.

All the parameters listed are programmable in the Quartus II software. The receiver PLL has the following features:

- Operates from 600 Mbps to 6.375 Gbps.
- Uses a reference clock between 50 MHz and 622.08 MHz.
- Programmable bandwidth settings: low, medium, and high.
- Programmable `rx_locktorefclk` (forces the receiver PLL to lock to the reference clock) and `rx_locktodata` (forces the receiver PLL to lock to the data).
- The voltage-controlled oscillator (VCO) operates at half rate and has two modes. These modes are for low or high frequency operation and provide optimized phase-noise performance.
- Programmable frequency multiplication *W* of 1, 4, 5, 8, 10, 16, 20, and 25. Not all settings are supported for any particular frequency.
- Two lock indication signals are provided. They are found in PFD mode (lock-to-reference clock), and PD (lock-to-data).

The CRU has a built-in switchover circuit to select whether the PLL VCO is aligned by the reference clock or the data. The optional port rx_freqlocked monitors when the CRU is in locked-to-data mode.

In the automatic mode, the CRU PLL must be within the prescribed PPM frequency threshold setting of the CRU reference clock for the CRU to switch from locked-to-reference to locked-to-data mode.

The automatic switchover circuit can be overridden by using the optional ports rx_locktorefclk and rx_locktodata. Table 2–6 shows the possible combinations of these two signals.

Table 2–6. Receiver Lock Combinations

rx_locktodata	rx_locktorefclk	VCO (Lock to Mode)
0	0	Auto
0	1	Reference clock
1	x	Data

If the rx_locktorefclk and rx_locktodata ports are not used, the default is auto mode.

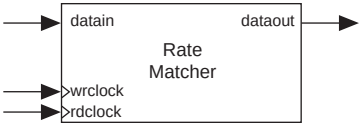
Deserializer (Serial-to-Parallel Converter)

The deserializer converts a serial bitstream into 8, 10, 16, or 20 bits of parallel data. The deserializer receives the LSB first. Figure 2–17 shows the deserializer.

Rate Matcher

Rate matcher is available in Basic, PCI Express, XAUI, and GIGE modes and consists of a 20-word deep FIFO buffer and a FIFO controller. Figure 2–20 shows the implementation of the rate matcher in the Stratix II GX device.

Figure 2–20. Rate Matcher



In a multi-crystal environment, the rate matcher compensates for up to a ± 300-PPM difference between the source and receiver clocks. Table 2–8 shows the standards supported and the PPM for the rate matcher tolerance.

Table 2–8. Rate Matcher PPM Support *Note (1)*

Standard	PPM
XAUI	± 100
PCI Express (PIPE)	± 300
GIGE	± 100
Basic Double-Width	± 300

Note to Table 2–8:

(1) Refer to the *Stratix II GX Transceiver User Guide* for the Altera®-defined scheme.

Basic Mode

In Basic mode, you can program the skip and control pattern for rate matching. In single-width Basic mode, there is no restriction on the deletion of a skip character in a cluster. The rate matcher deletes the skip characters as long as they are available. For insertion, the rate matcher inserts skip characters such that the number of skip characters at the output of rate matcher does not exceed five. In double-width mode, the rate matcher deletes skip character when they appear as pairs in the upper and lower bytes. There are no restrictions on the number of skip characters that are deleted. The rate matcher inserts skip characters as pairs.

R24 row interconnects span 24 LABs and provide the fastest resource for long row connections between LABs, TriMatrix memory, DSP blocks, and Row IOEs. The R24 row interconnects can cross M-RAM blocks. R24 row interconnects drive to other row or column interconnects at every fourth LAB and do not drive directly to LAB local interconnects. R24 row interconnects drive LAB local interconnects via R4 and C4 interconnects. R24 interconnects can drive R24, R4, C16, and C4 interconnects. The column interconnect operates similarly to the row interconnect and vertically routes signals to and from LABs, TriMatrix memory, DSP blocks, and IOEs. Each column of LABs is served by a dedicated column interconnect.

These column resources include:

- Shared arithmetic chain interconnects in a LAB
- Carry chain interconnects in a LAB and from LAB to LAB
- Register chain interconnects in a LAB
- C4 interconnects traversing a distance of four blocks in an up and down direction
- C16 column interconnects for high-speed vertical routing through the device

Stratix II GX devices include an enhanced interconnect structure in LABs for routing shared arithmetic chains and carry chains for efficient arithmetic functions. The register chain connection allows the register output of one ALM to connect directly to the register input of the next ALM in the LAB for fast shift registers. These ALM-to-ALM connections bypass the local interconnect. The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. Figure 2–47 shows the shared arithmetic chain, carry chain, and register chain interconnects.

A path in which a pin directly drives a register can require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinational logic may not require the delay. Programmable delays exist for decreasing input-pin-to-logic-array and IOE input register delays. The Quartus II Compiler can program these delays to automatically minimize setup time while providing a zero hold time. Programmable delays can increase the register-to-pin delays for output and/or output enable registers. Programmable delays are no longer required to ensure zero hold times for logic array register-to-IOE register transfers. The Quartus II Compiler can create the zero hold time for these transfers. Table 2–30 shows the programmable delays for Stratix II GX devices.

Table 2–30. Stratix II GX Programmable Delay Chain

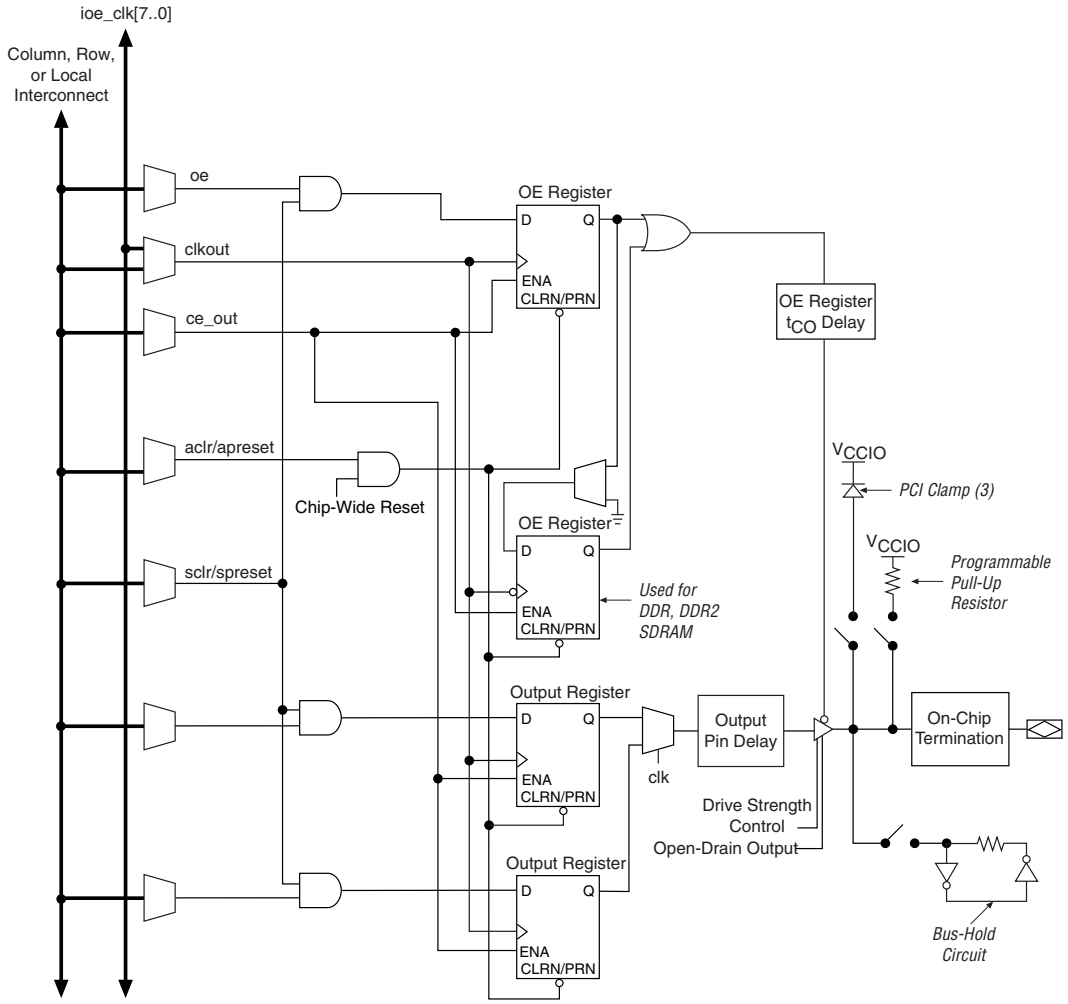
Programmable Delays	Quartus II Logic Option
Input pin to logic array delay	Input delay from pin to internal cells
Input pin to input register delay	Input delay from pin to input register
Output pin delay	Delay from output register to output pin
Output enable register t_{CO} delay	Delay to output enable pin

The IOE registers in Stratix II GX devices share the same source for clear or preset. You can program preset or clear for each individual IOE. You can also program the registers to power up high or low after configuration is complete. If programmed to power up low, an asynchronous clear can control the registers. If programmed to power up high, an asynchronous preset can control the registers. This feature prevents the inadvertent activation of another device's active-low input upon power-up. If one register in an IOE uses a preset or clear signal, all registers in the IOE must use that same signal if they require preset or clear. Additionally, a synchronous reset signal is available for the IOE registers.

Double Data Rate I/O Pins

Stratix II GX devices have six registers in the IOE, which support DDR interfacing by clocking data on both positive and negative clock edges. The IOEs in Stratix II GX devices support DDR inputs, DDR outputs, and bidirectional DDR modes. When using the IOE for DDR inputs, the two input registers clock double rate input data on alternating edges. An input latch is also used in the IOE for DDR input acquisition. The latch holds the data that is present during the clock high times, allowing both bits of data to be synchronous with the same clock edge (either rising or falling). Figure 2–82 shows an IOE configured for DDR input. Figure 2–83 shows the DDR input timing diagram.

Figure 2–84. Stratix II GX IOE in DDR Output I/O Configuration *Notes (1), (2)*



Notes to Figure 2–84:

(1) All input signals to the IOE can be inverted at the IOE.

(2) The tri-state buffer is active low. The DDIO megafunction represents the tri-state buffer as active-high with an inverter at the OE register data port.

(3) The optional PCI clamp is only available on column I/O pins.

Table 2–42. Document Revision History (Part 2 of 6)

Date and Document Version	Changes Made	Summary of Changes
February 2007 v2.0	Added Chapter 02 “Stratix II GX Transceivers” to the beginning of Chapter 03 “Stratix II GX Architecture”. • Changed chapter number to Chapter 02.	Combined Chapter 02 “Stratix II GX Transceivers” and Chapter 03 “Stratix II GX Architecture” in the new Chapter 02 “Stratix II GX Architecture”
	Added the “Document Revision History” section to this chapter.	
	Moved the “Stratix II GX Transceiver Clocking” section to after the “Receiver Path” section.	

4. DC and Switching Characteristics

SIIGX51006-4.6

Operating Conditions

Stratix® II GX devices are offered in both commercial and industrial grades. Industrial devices are offered in -4 speed grade and commercial devices are offered in -3 (fastest), -4, and -5 speed grades.

Tables 4–1 through 4–51 provide information on absolute maximum ratings, recommended operating conditions, DC electrical characteristics, and other specifications for Stratix II GX devices.

Absolute Maximum Ratings

Table 4–1 contains the absolute maximum ratings for the Stratix II GX device family.

Table 4–1. Stratix II GX Device Absolute Maximum Ratings *Notes (1), (2), (3)*

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage	With respect to ground	–0.5	1.8	V
V_{CCIO}	Supply voltage	With respect to ground	–0.5	4.6	V
V_{CCPD}	Supply voltage	With respect to ground	–0.5	4.6	V
V_I	DC input voltage *(4)*		–0.5	4.6	V
I_{OUT}	DC output current, per pin		–25	40	mA
T_{STG}	Storage temperature	No bias	–65	150	C
T_J	Junction temperature	BGA packages under bias	–55	125	C

Notes to Table 4–1:

(1) See the *Operating Requirements for Altera Devices Data Sheet* for more information.

(2) Conditions beyond those listed in Table 4–1 may cause permanent damage to a device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse affects on the device.

(3) Supply voltage specifications apply to voltage readings taken at the device pins, not at the power supply.

(4) During transitions, the inputs may overshoot to the voltage shown in Table 4–2 based upon the input duty cycle. The DC case is equivalent to 100% duty cycle. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 19 of 19)											
Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	

Notes to Table 4–19:

(1) Dedicated REFCLK pins were used to drive the input reference clocks.
(2) Jitter numbers specified are valid for the stated conditions only.
(3) Refer to the protocol characterization documents for detailed information.
(4) HiGig configuration is available in a -3 speed grade only. For more information, refer to the *Stratix II GX Transceiver Architecture Overview* chapter in volume 2 of the *Stratix II GX Device Handbook*.
(5) Stratix II GX transceivers meet CEI jitter generation specification of 0.3 UI for a V_{OD} range of 400 mV to 1000 mV.
(6) The Sinusoidal Jitter Tolerance Mask is defined only for low voltage (LV) variant of CPRI.
(7) The jitter numbers for SONET/SDH are compliant to the GR-253-CORE Issue 3 Specification.
(8) The jitter numbers for Fibre Channel are compliant to the FC-PI-4 Specification revision 6.10.
(9) The jitter numbers for XAUI are compliant to the IEEE802.3ae-2002 Specification.
(10) The jitter numbers for PCI Express are compliant to the PCIe Base Specification 2.0.
(11) The jitter numbers for Serial RapidIO are compliant to the RapidIO Specification 1.3.
(12) The jitter numbers for GIGE are compliant to the IEEE802.3-2002 Specification.
(13) The jitter numbers for HiGig are compliant to the IEEE802.3ae-2002 Specification.
(14) The jitter numbers for (OIF) CEI are compliant to the OIF-CEI-02.0 Specification.
(15) The jitter numbers for CPRI are compliant to the CPRI Specification V2.1.
(16) The HD-SDI and 3G-SDI jitter numbers are compliant to the SMPTE292M and SMPTE424M Specifications.
(17) The Fibre Channel transmitter jitter generation numbers are compliant to the specification at β_T interoperability point.
(18) The Fibre Channel receiver jitter tolerance numbers are compliant to the specification at β_R interoperability point.

Table 4–20 provides information on recommended input clock jitter for each mode.

Table 4–20. Recommended Input Clock Jitter (Part 1 of 2)						
Mode	Reference Clock (MHz)	Vectron LVPECL XO Type/Model	Frequency Range (MHz)	RMS Jitter (12 kHz to 20 MHz) (ps)	Period Jitter (Peak to Peak) (ps)	Phase Noise at 1 MHz (dB c/Hz)
PCI-E	100	VCC6-Q/R	10 to 270	0.3	23	-149.9957
(OIF) CEI PHY	156.25	VCC6-Q/R	10 to 270	0.3	23	-146.2169
	622.08	VCC6-Q	270 to 800	2	30	Not available
GIGE	62.5	VCC6-Q/R	10 to 270	0.3	23	-149.9957
	125	VCC6-Q/R	10 to 270	0.3	23	-146.9957
XAUI	156.25	VCC6-Q/R	10 to 270	0.3	23	-146.2169

Table 4–32. LVPECL Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO} *(1)*	I/O supply voltage		3.135	3.3	3.465	V
V_{ID}	Input differential voltage swing (single-ended)		300	600	1,000	mV
V_{ICM}	Input common mode voltage		1.0		2.5	V
V_{OD}	Output differential voltage (single-ended)	R_L = 100 Ω	525		970	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	1,650		2,250	mV
R_L	Receiver differential input resistor		90	100	110	Ω

Note to Table 4–32:

(1) The top and bottom clock input differential buffers in I/O banks 3, 4, 7, and 8 are powered by V_{CCINT}, not V_{CCIO}. The PLL clock output/feedback differential buffers are powered by VCC_PLL_OUT. For differential clock output/feedback operation, connect VCC_PLL_OUT to 3.3 V.

Table 4–33. 3.3-V PCI Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{IH}	High-level input voltage		0.5 V_{CCIO}		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage		–0.3		0.3 V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	0.9 V_{CCIO}			V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA			0.1 V_{CCIO}	V

Table 4–34. PCI-X Mode 1 Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		3.0		3.6	V
V_{IH}	High-level input voltage		0.5 V_{CCIO}		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage		–0.3		0.35 V_{CCIO}	V
V_{IPU}	Input pull-up voltage		0.7 V_{CCIO}			V
V_{OH}	High-level output voltage	I_{OUT} = –500 µA	0.9 V_{CCIO}			V
V_{OL}	Low-level output voltage	I_{OUT} = 1,500 µA			0.1 V_{CCIO}	V

Table 4–46. 1.8-V HSTL Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.71	1.80	1.89	V
V_{REF}	Input reference voltage		0.85	0.90	0.95	V
V_{TT}	Termination voltage		0.85	0.90	0.95	V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 16 mA *(1)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OH} = –16 mA *(1)*			0.4	V

Note to Table 4–46:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Table 4–47. 1.8-V HSTL Class I and II Differential Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage		1.71	1.80	1.89	V
V_{DIF} (DC)	DC input differential voltage		0.2			V
V_{CM} (DC)	DC common mode input voltage		0.78		1.12	V
V_{DIF} (AC)	AC differential input voltage		0.4			V
V_{OX} (AC)	AC differential cross point voltage		0.68		0.9	V

Bus Hold Specifications

Table 4–48 shows the Stratix II GX device family bus hold specifications.

Table 4–48. Bus Hold Parameters

Parameter	Conditions	V_{CCIO} Level										Unit
		1.2 V		1.5 V		1.8 V		2.5 V		3.3 V		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	$V_{IN} > V_{IL}$ (maximum)	22.5		25		30		50		70		µA
High sustaining current	$V_{IN} < V_{IH}$ (minimum)	–22.5		–25		–30		–50		–70		µA
Low overdrive current	$0 V < V_{IN} < V_{CCIO}$		120		160		200		300		500	µA
High overdrive current	$0 V < V_{IN} < V_{CCIO}$		–120		–160		–200		–300		–500	µA
Bus-hold trip point		0.45	0.95	0.5	1.0	0.68	1.07	0.7	1.7	0.8	2.0	V

On-Chip Termination Specifications

Tables 4–49 and 4–50 define the specification for internal termination resistance tolerance when using series or differential on-chip termination.

Table 4–49. On-Chip Termination Specification for Top and Bottom I/O Banks (Part 1 of 2) *Notes (1), (2)*

Symbol	Description	Conditions	Resistance Tolerance		
			Commercial Max	Industrial Max	Unit
25-Ω R_S 3.3/2.5	Internal series termination with calibration (25-Ω setting)	V_{CCIO} = 3.3/2.5 V	±5	±10	%
	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 3.3/2.5 V	±30	±30	%
50-Ω R_S 3.3/2.5	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 3.3/2.5 V	±5	±10	%
	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 3.3/2.5 V	±30	± 30	%

Power Consumption

Altera offers two ways to calculate power for a design: the Excel-based PowerPlay early power estimator power calculator and the Quartus® II PowerPlay power analyzer feature.

The interactive Excel-based PowerPlay early power estimator is typically used prior to designing the FPGA in order to get an estimate of device power. The Quartus II PowerPlay power analyzer provides better quality estimates based on the specifics of the design after place-and-route is complete. The power analyzer can apply a combination of user-entered, simulation-derived and estimated signal activities which, combined with detailed circuit models, can yield very accurate power estimates.

In both cases, these calculations should only be used as an estimation of power, not as a specification.

For more information on PowerPlay tools, refer to the *PowerPlay Early Power Estimators (EPE) and Power Analyzer,* the *Quartus II PowerPlay Analysis and Optimization Technology*, and the *PowerPlay Power Analyzer* chapter in volume 3 of the *Quartus II Handbook*. The PowerPlay early power estimators are available on the Altera web site at **www.altera. com**.

See Table 4–23 on page 42 for typical I_{CC} standby specifications.

Timing Model

The DirectDrive technology and MultiTrack interconnect ensure predictable performance, accurate simulation, and accurate timing analysis across all Stratix II GX device densities and speed grades. This section describes and specifies the performance, internal, external, and PLL timing specifications.

All specifications are representative of worst-case supply voltage and junction temperature conditions.

Preliminary and Final Timing

Timing models can have either preliminary or final status. The Quartus II software issues an informational message during the design compilation if the timing models are preliminary. Table 4–52 shows the status of the Stratix II GX device timing models.

Preliminary status means the timing model is subject to change. Initially, timing numbers are created using simulation results, process data, and other known parameters. These tests are used to make the preliminary numbers as close to the actual timing parameters as possible.

Final timing numbers are based on actual device operation and testing. These numbers reflect the actual performance of the device under worst-case voltage and junction temperature conditions.

Table 4–52. Stratix II GX Device Timing Model Status

Device	Preliminary	Final
EP2SGX30		✓
EP2SGX60		✓
EP2SGX90		✓
EP2SGX130		✓

I/O Timing Measurement Methodology

Different I/O standards require different baseline loading techniques for reporting timing delays. Altera characterizes timing delays with the required termination for each I/O standard and with 0 pF (except for PCI and PCI-X which use 10 pF) loading and the timing is specified up to the output pin of the FPGA device. The Quartus II software calculates the I/O timing for each I/O standard with a default baseline loading as specified by the I/O standards.

The following measurements are made during device characterization. Altera measures clock-to-output delays (t_{CO}) at worst-case process, minimum voltage, and maximum temperature (PVT) for default loading conditions shown in Table 4–53. Use the following equations to calculate clock pin to output pin timing for Stratix II GX devices.

t_{CO} from clock pin to I/O pin = delay from clock pad to I/O output register + IOE output register clock-to-output delay + delay from output register to output pin + I/O output delay

t_{xz}/t_{zx} from clock pin to I/O pin = delay from clock pad to I/O output register + IOE output register clock-to-output delay + delay from output register to output pin + I/O output delay + output enable pin delay

Simulation using IBIS models is required to determine the delays on the PCB traces in addition to the output pin delay timing reported by the Quartus II software and the timing model in the device handbook.

1. Simulate the output driver of choice into the generalized test setup, using values from Table 4–53.
2. Record the time to V_{MEAS}.

Table 4–57. IOE Internal Timing Microparameters (Part 2 of 2)

Symbol	Parameter	-3 Speed Grade (1)		-3 Speed Grade (2)		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{PIN2COMBOUT\_R}$	Row input pin to IOE combinational output	410	760	410	798	410	848	410	1018	ps
$t_{PIN2COMBOUT\_C}$	Column input pin to IOE combinational output	428	787	428	825	428	878	428	1054	ps
$t_{COMBIN2PIN\_R}$	Row IOE data input to combinational output pin	1101	2026	1101	2127	1101	2261	1101	2439	ps
$t_{COMBIN2PIN\_C}$	Column IOE data input to combinational output pin	991	1854	991	1946	991	2069	991	2246	ps
t_{CLR}	Minimum clear pulse width	200		210		223		268		ps
t_{PRE}	Minimum preset pulse width	200		210		223		268		ps
t_{CLKL}	Minimum clock low time	600		630		669		804		ps
t_{CLKH}	Minimum clock high time	600		630		669		804		ps

(1) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
(2) This column refers to –3 speed grades for EP2SGX130 devices.

Table 4–58. DSP Block Internal Timing Microparameters (Part 1 of 2)

Symbol	Parameter	-3 Speed Grade (1)		-3 Speed Grade (2)		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{SU}	Input, pipeline, and output register setup time before clock	50		52		55		67		ps
t_{H}	Input, pipeline, and output register hold time after clock	180		189		200		241		ps
t_{CO}	Input, pipeline, and output register clock-to-output delay	0	0	0	0	0	0	0	0	ps

Table 4–86. Stratix II GX I/O Output Delay for Column Pins (Part 3 of 7)								
I/O Standard	Drive Strength	Parameter	Fast Corner Industrial/ Commercial	-3 Speed Grade *(3)*	-3 Speed Grade *(4)*	-4 Speed Grade	-5 Speed Grade	Unit
SSTL-2 Class I	8 mA	t_{OP}	957	1715	1799	1913	2041	ps
		t_{DIP}	979	1781	1869	1987	2131	ps
	12 mA *(1)*	t_{OP}	940	1672	1754	1865	1991	ps
		t_{DIP}	962	1738	1824	1939	2081	ps
SSTL-2 Class II	16 mA	t_{OP}	918	1609	1688	1795	1918	ps
		t_{DIP}	940	1675	1758	1869	2008	ps
	20 mA	t_{OP}	919	1598	1676	1783	1905	ps
		t_{DIP}	941	1664	1746	1857	1995	ps
	24 mA *(1)*	t_{OP}	915	1596	1674	1781	1903	ps
		t_{DIP}	937	1662	1744	1855	1993	ps
SSTL-18 Class I	4 mA	t_{OP}	953	1690	1773	1886	2012	ps
		t_{DIP}	975	1756	1843	1960	2102	ps
	6 mA	t_{OP}	958	1656	1737	1848	1973	ps
		t_{DIP}	980	1722	1807	1922	2063	ps
	8 mA	t_{OP}	937	1640	1721	1830	1954	ps
		t_{DIP}	959	1706	1791	1904	2044	ps
	10 mA	t_{OP}	942	1638	1718	1827	1952	ps
		t_{DIP}	964	1704	1788	1901	2042	ps
	12 mA *(1)*	t_{OP}	936	1626	1706	1814	1938	ps
		t_{DIP}	958	1692	1776	1888	2028	ps
SSTL-18 Class II	8 mA	t_{OP}	925	1597	1675	1782	1904	ps
		t_{DIP}	947	1663	1745	1856	1994	ps
	16 mA	t_{OP}	937	1578	1655	1761	1882	ps
		t_{DIP}	959	1644	1725	1835	1972	ps
	18 mA	t_{OP}	933	1585	1663	1768	1890	ps
		t_{DIP}	955	1651	1733	1842	1980	ps
	20 mA *(1)*	t_{OP}	933	1583	1661	1766	1888	ps
		t_{DIP}	955	1649	1731	1840	1978	ps

Table 4–97. Maximum Output Clock Toggle Rate Derating Factors (Part 3 of 5)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate Derating Factors (ps/pF)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		-3	-4	-5	-3	-4	-5	-3	-4	-5
SSTL-18 Class II	8 mA	173	206	206	-	-	-	155	206	206
	16 mA	150	160	160	-	-	-	140	160	160
	18 mA	120	130	130	-	-	-	110	130	130
	20 mA	109	127	127	-	-	-	94	127	127
2.5-V SSTL-2 Class I	8 mA	364	680	680	364	680	680	350	680	680
	12 mA	163	207	207	163	207	207	188	207	207
2.5-V SSTL-2 Class II	16 mA	118	147	147	118	147	147	94	147	147
	20 mA	99	122	122	-	-	-	87	122	122
	24 mA	91	116	116	-	-	-	85	116	116
1.8-V SSTL-18 Class I	4 mA	458	570	570	458	570	570	505	570	570
	6 mA	305	380	380	305	380	380	336	380	380
	8 mA	225	282	282	225	282	282	248	282	282
	10 mA	167	220	220	167	220	220	190	220	220
	12 mA	129	175	175	-	-	-	148	175	175
1.8-V SSTL-18 Class II	8 mA	173	206	206	-	-	-	155	206	206
	16 mA	150	160	160	-	-	-	140	160	160
	18 mA	120	130	130	-	-	-	110	130	130
	20 mA	109	127	127	-	-	-	94	127	127
1.8-V HSTL Class I	4 mA	245	282	282	245	282	282	229	282	282
	6 mA	164	188	188	164	188	188	153	188	188
	8 mA	123	140	140	123	140	140	114	140	140
	10 mA	110	124	124	110	124	124	108	124	124
	12 mA	97	110	110	97	110	110	104	110	110
1.8-V HSTL Class II	16 mA	101	104	104	-	-	-	99	104	104
	18 mA	98	102	102	-	-	-	93	102	102
	20 mA	93	99	99	-	-	-	88	99	99
1.5-V HSTL Class I	4 mA	168	196	196	168	196	196	188	196	196
	6 mA	112	131	131	112	131	131	125	131	131
	8 mA	84	99	99	84	99	99	95	99	99
	10 mA	87	98	98	-	-	-	90	98	98
	12 mA	86	98	98	-	-	-	87	98	98

Therefore, the DCD percentage for the output clock is from 48.4% to 51.6%.

Table 4–101. Maximum DCD for DDIO Output on Row I/O Pins Without PLL in the Clock Path for -4 and -5 Devices *Note (1)*

Maximum DCD (ps) for Row DDIO Output I/O Standard	Input I/O Standard (No PLL in the Clock Path)					Unit
	TTL/CMOS		SSTL-2	SSTL/HSTL	LVDS	
	3.3/2.5V	1.8/1.5V	2.5V	1.8/1.5V	3.3V	
3.3-V LVTTL	440	495	170	160	105	ps
3.3-V LVCMOS	390	450	120	110	75	ps
2.5 V	375	430	105	95	90	ps
1.8 V	325	385	90	100	135	ps
1.5-V LVCMOS	430	490	160	155	100	ps
SSTL-2 Class I	355	410	85	75	85	ps
SSTL-2 Class II	350	405	80	70	90	ps
SSTL-18 Class I	335	390	65	65	105	ps
1.8-V HSTL Class I	330	385	60	70	110	ps
1.5-V HSTL Class I	330	390	60	70	105	ps
LVDS	180	180	180	180	180	ps

(1) Table 4–101 assumes the input clock has zero DCD.

Table 4–102. Maximum DCD for DDIO Output on Column I/O Pins Without PLL in the Clock Path for -3 Devices (Part 1 of 2) *Note (1)*

Maximum DCD (ps) for DDIO Column Output I/O Standard	Input IO Standard (No PLL in the Clock Path)					Unit
	TTL/CMOS		SSTL-2	SSTL/HSTL	HSTL12	
	3.3/2.5V	1.8/1.5V	2.5V	1.8/1.5V	1.2V	
3.3-V LVTTL	260	380	145	145	145	ps
3.3-V LVCMOS	210	330	100	100	100	ps
2.5 V	195	315	85	85	85	ps
1.8 V	150	265	85	85	85	ps
1.5-V LVCMOS	255	370	140	140	140	ps
SSTL-2 Class I	175	295	65	65	65	ps
SSTL-2 Class II	170	290	60	60	60	ps
SSTL-18 Class I	155	275	55	50	50	ps

Table 4–108 shows the high-speed I/O timing specifications for -4 speed grade Stratix II GX devices.

Table 4–108. High-Speed I/O Specifications for -4 Speed Grade *Notes (1), (2)*

Symbol	Conditions			-4 Speed Grade			Unit
				Min	Typ	Max	
$f_{IN} = f_{HSDR} / W$	W = 2 to 32 (LVDS, HyperTransport technology) *(3)*			16		520	MHz
	W = 1 (SERDES bypass, LVDS only)			16		500	MHz
	W = 1 (SERDES used, LVDS only)			150		717	MHz
f_{HSDR} (data rate)	J = 4 to 10 (LVDS, HyperTransport technology)			150		1,040	Mbps
	J = 2 (LVDS, HyperTransport technology)			*(4)*		760	Mbps
	J = 1 (LVDS only)			*(4)*		500	Mbps
$f_{HSDRDPA}$ (DPA data rate)	J = 4 to 10 (LVDS, HyperTransport technology)			150		1,040	Mbps
TCCS	All differential standards			-		200	ps
SW	All differential standards			330		-	ps
Output jitter						190	ps
Output t_{RISE}	All differential I/O standards					160	ps
Output t_{FALL}	All differential I/O standards					180	ps
t_{DUTY}				45	50	55	%
DPA run length						6,400	UI
DPA jitter tolerance	Data channel peak-to-peak jitter			0.44			UI
DPA lock time							Number of repetitions
	SPI-4	0000000000 1111111111	10%	256			
	Parallel Rapid I/O	00001111	25%	256			
		10010000	50%	256			
	Miscellaneous	10101010	100%	256			
		01010101		256			

(1) When J = 4 to 10, the SERDES block is used.
(2) When J = 1 or 2, the SERDES block is bypassed.
(3) The input clock frequency and the W factor must satisfy the following fast PLL VCO specification: 150 ≤nput clock frequency × W ≤1,040.
(4) The minimum specification is dependent on the clock source (fast PLL, enhanced PLL, clock pin, and so on) and the clock routing resource (global, regional, or local) utilized. The I/O differential buffer and input register do not have a minimum toggle rate.

Table 4–118. Document Revision History (Part 3 of 5)		
Date and Document Version	**Changes Made**	**Summary of Changes**
February 2007 v4.2	Added the “Document Revision History” section to this chapter.	Added support information for the Stratix II GX device.
	Updated Table 4–5: ● Removed last three lines ● Removed note 1 ● Added new note 4	
	Deleted table 6-6.	
	Replaced Table 4–6 with all new information.	
	Added Figures 4–1 and 4–2.	
	Added Tables 4–7 through 4–19.	
	Removed Figures 6-1 through 6-4.	
	Updated Table 4–22: ● Changed R_{CONF} information.	
	Updated Table 4–52 ● SSTL-18 Class I, column 1: changed 25 to 50.	
	Updated: ● Table 4–54 ● Table 4–87 ● Table 4–91 ● Table 4–94	
	Updated Tables 4–62 through 4–77	
	Updated Tables 4–79 and 4–80 ● Added “units” column	
	Updated Tables 4–83 through 4–86 ● Changed column title to “Fast Corner Industrial/Commercial”.	
	Updated Table 4–109. ● Added a new line to the bottom of the table.	
August 2006 v4.1	Update Table 6–75, Table 6–84, and Table 6–90.	