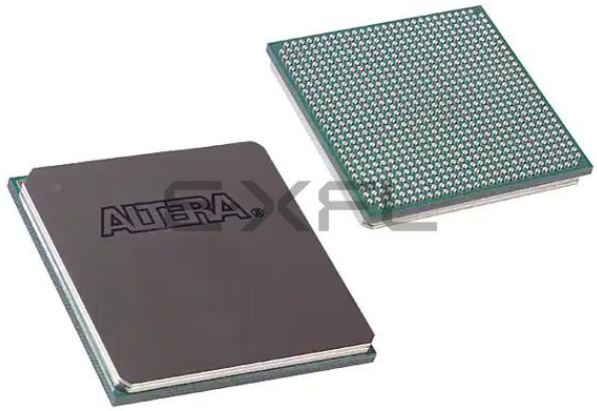

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

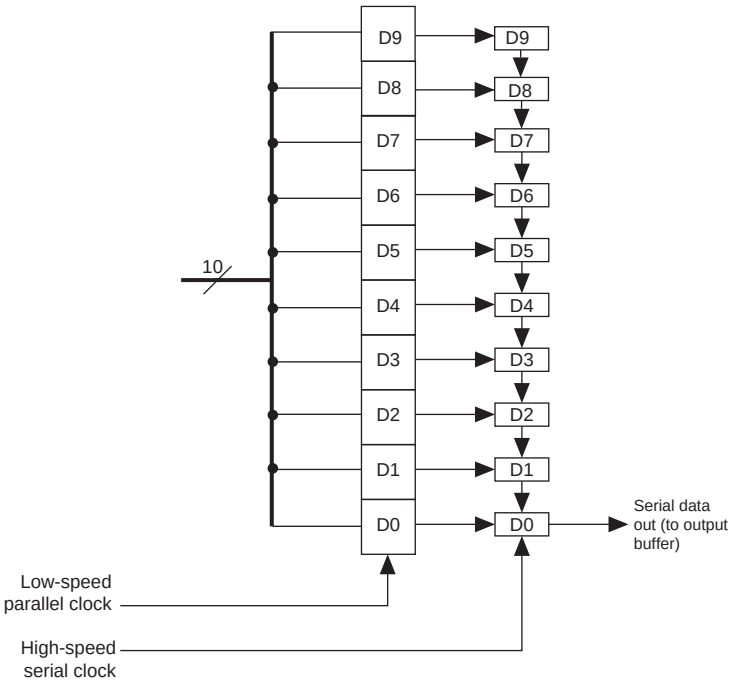
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1694
Number of Logic Elements/Cells	33880
Total RAM Bits	1369728
Number of I/O	361
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	780-BBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2sgx30cf780c4n

Serializer (Parallel-to-Serial Converter)

The serializer converts the parallel 8, 10, 16, or 20-bit data into a serial data bit stream, transmitting the least significant bit (LSB) first. The serialized data stream is then fed to the high-speed differential transmit buffer. Figure 2–7 is a diagram of the serializer.

Figure 2–7. Serializer *Note (1)*



Note to Figure 2–7:
(1) This is a 10-bit serializer. The serializer can also convert 8, 16, and 20 bits of data.

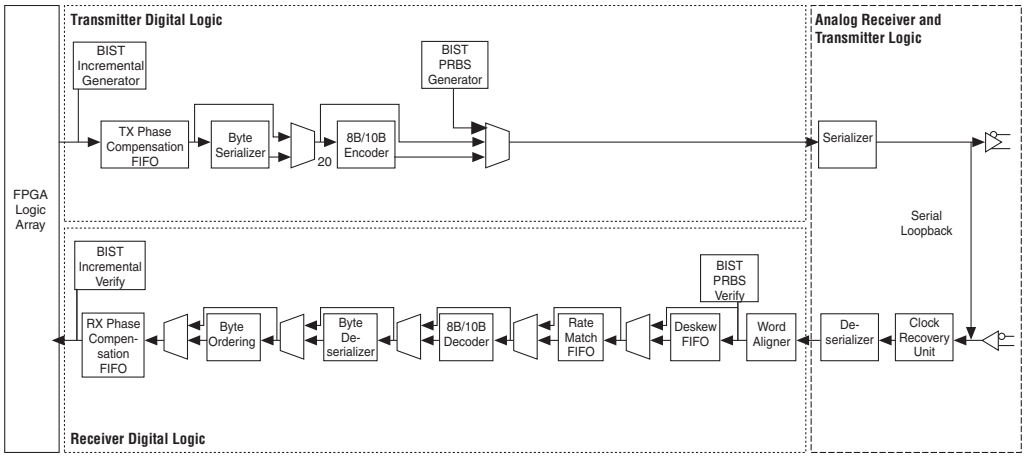
Transmit Buffer

The Stratix II GX transceiver buffers support the 1.2- and 1.5-V PCML I/O standard at rates up to 6.375 Gbps. The common mode voltage (V_{CM}) of the output driver is programmable. The following V_{CM} values are available when the buffer is in 1.2- and 1.5-V PCML.

- V_{CM} = 0.6 V
- V_{CM} = 0.7 V

Figure 2–24 shows the data path in serial loopback mode.

Figure 2–24. Stratix II GX Block in Serial Loopback Mode with BIST and PRBS



Parallel Loopback

The parallel loopback mode exercises the digital logic portion of the transceiver data path. The analog portions are not used in this loopback path, and the received high-speed serial data is not retimed. This protocol is available as one of the sub-protocols under Basic mode and can be used only for Basic double-width mode.

In this loopback mode, the data from the internally available BIST generator is transmitted. The data is looped back after the end of PCS and before the PMA. On the receive side, an internal BIST verifier checks for errors. This loopback enables you to verify the PCS block.

Table 2–16. Reset Signal Map to Stratix II GX Blocks

Reset Signal	Transmitter Phase Compensation FIFO Module/ Byte Serializer	Transmitter 8B/10B Encoder	Transmitter Serializer	Transmitter Analog Circuits	Transmitter PLL	Transmitter XAUI State Machine	BIST Generators	Receiver Deserializer	Receiver Word Aligner	Receiver Deskew FIFO Module	Receiver Rate Matcher	Receiver 8B/10B Decoder	Receiver Phase Comp FIFO Module/ Byte Deserializer	Receiver PLL / CRU	Receiver XAUI State Machine	BIST Verifiers	Receiver Analog Circuits
rx_digitalreset									✓	✓	✓	✓	✓		✓	✓	
rx_analogreset								✓						✓			✓
tx_digitalreset	✓	✓				✓	✓										
gxb_powerdown	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
gxb_enable	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Voltage Reference Capabilities

Stratix II GX transceivers provide voltage reference and bias circuitry. To set up internal bias for controlling the transmitter output driver voltage swings, as well as to provide voltage and current biasing for other analog circuitry, the device uses an internal bandgap voltage reference of 0.7 V. An external 2-KΩ resistor connected to ground generates a constant bias current (independent of power supply drift, process changes, or temperature variation). An on-chip resistor generates a tracking current that tracks on-chip resistor variation. These currents are mirrored and distributed to the analog circuitry in each channel.

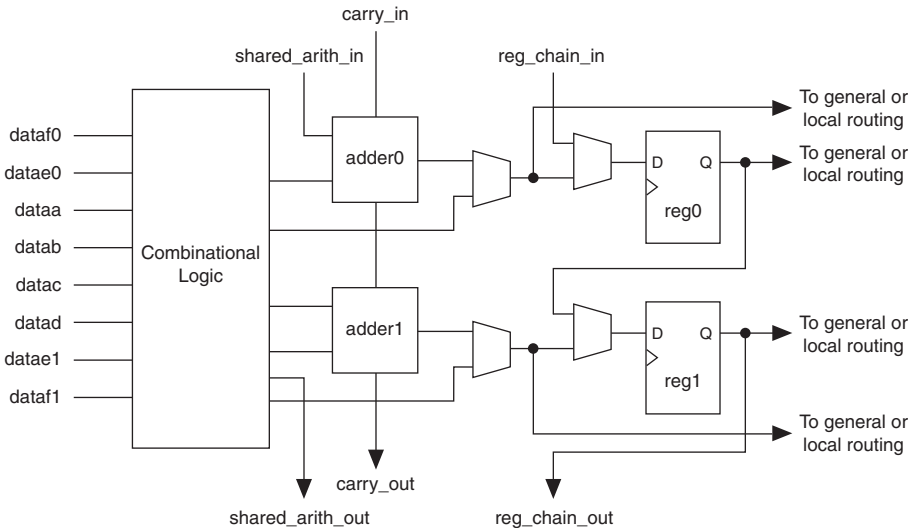
For more information, refer to the *DC and Switching Characteristics* chapter in volume 1 of the *Stratix II GX Handbook*.

Adaptive Logic Modules

The basic building block of logic in the Stratix II GX architecture is the ALM. The ALM provides advanced features with efficient logic utilization. Each ALM contains a variety of look-up table (LUT)-based resources that can be divided between two adaptive LUTs (ALUTs). With up to eight inputs to the two ALUTs, one ALM can implement various combinations of two functions. This adaptability allows the ALM to be completely backward-compatible with four-input LUT architectures. One ALM can also implement any function of up to six inputs and certain seven-input functions.

In addition to the adaptive LUT-based resources, each ALM contains two programmable registers, two dedicated full adders, a carry chain, a shared arithmetic chain, and a register chain. Through these dedicated resources, the ALM can efficiently implement various arithmetic functions and shift registers. Each ALM drives all types of interconnects: local, row, column, carry chain, shared arithmetic chain, register chain, and direct link interconnects. Figure 2–35 shows a high-level block diagram of the Stratix II GX ALM while Figure 2–36 shows a detailed view of all the connections in the ALM.

Figure 2–35. High-Level Block Diagram of the Stratix II GX ALM



M512 RAM blocks can have different clocks on its inputs and outputs. The wren, datain, and write address registers are all clocked together from one of the two clocks feeding the block. The read address, rden, and output registers can be clocked by either of the two clocks driving the block, allowing the RAM block to operate in read and write or input and output clock modes. Only the output register can be bypassed. The six labclk signals or local interconnect can drive the inclock, outclock, wren, rden, and outclr signals. Because of the advanced interconnect between the LAB and M512 RAM blocks, ALMs can also control the wren and rden signals and the RAM clock, clock enable, and asynchronous clear signals. Figure 2–49 shows the M512 RAM block control signal generation logic.

Figure 2–49. M512 RAM Block Control Signals

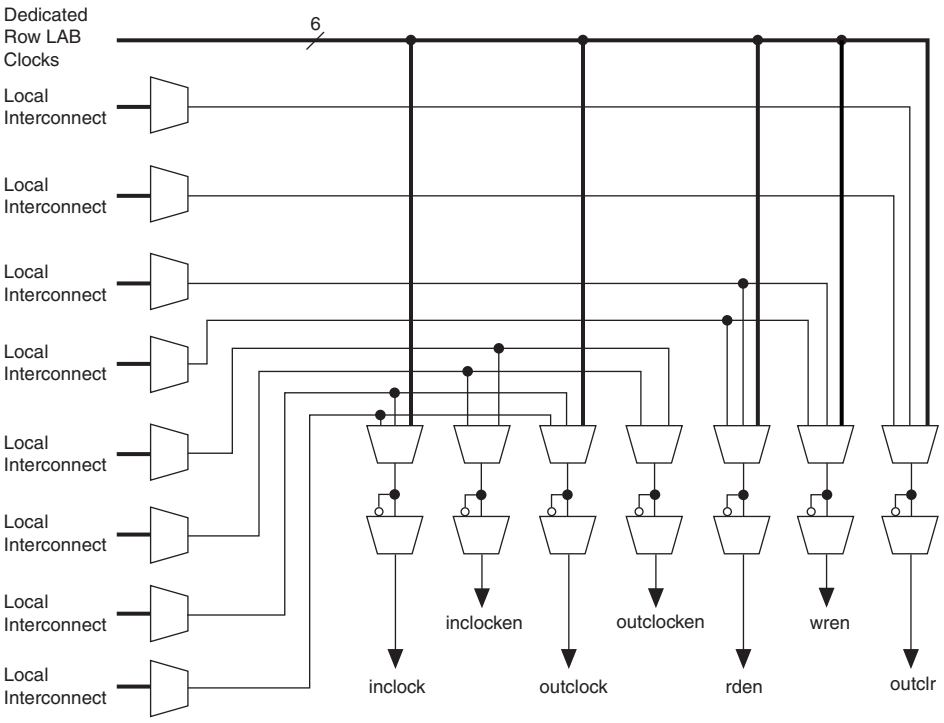
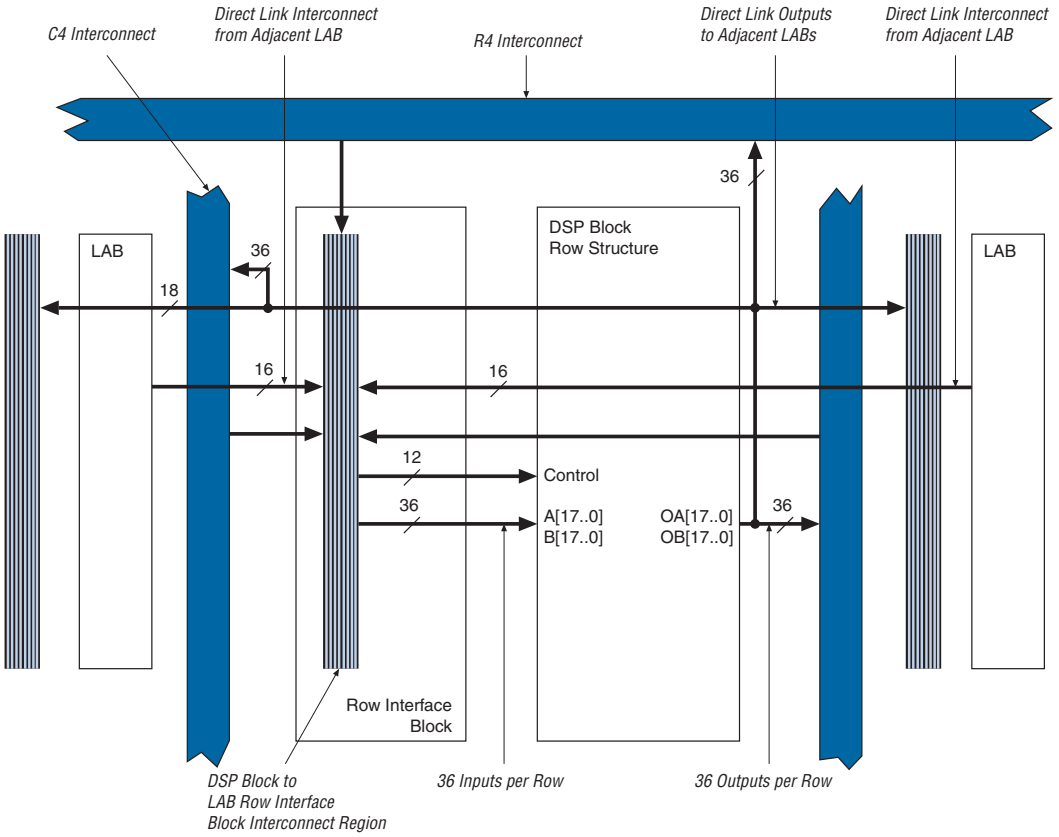


Figure 2–60. DSP Block Interface to Interconnect



A bus of 44 control signals feeds the entire DSP block. These signals include clocks, asynchronous clears, clock enables, signed and unsigned control signals, addition and subtraction control signals, rounding and saturation control signals, and accumulator synchronous loads. The clock signals are routed from LAB row clocks and are generated from specific LAB rows at the DSP block interface. The LAB row source for control signals, data inputs, and outputs is shown in Table 2–23.

Refer to the *DSP Blocks in Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook* for more information on DSP blocks.

IOE clocks have row and column block regions that are clocked by 8 I/O clock signals chosen from the 24 quadrant clock resources. Figures 2–65 and 2–66 show the quadrant relationship to the I/O clock regions.

Figure 2–65. EP2SGX30 Device I/O Clock Groups

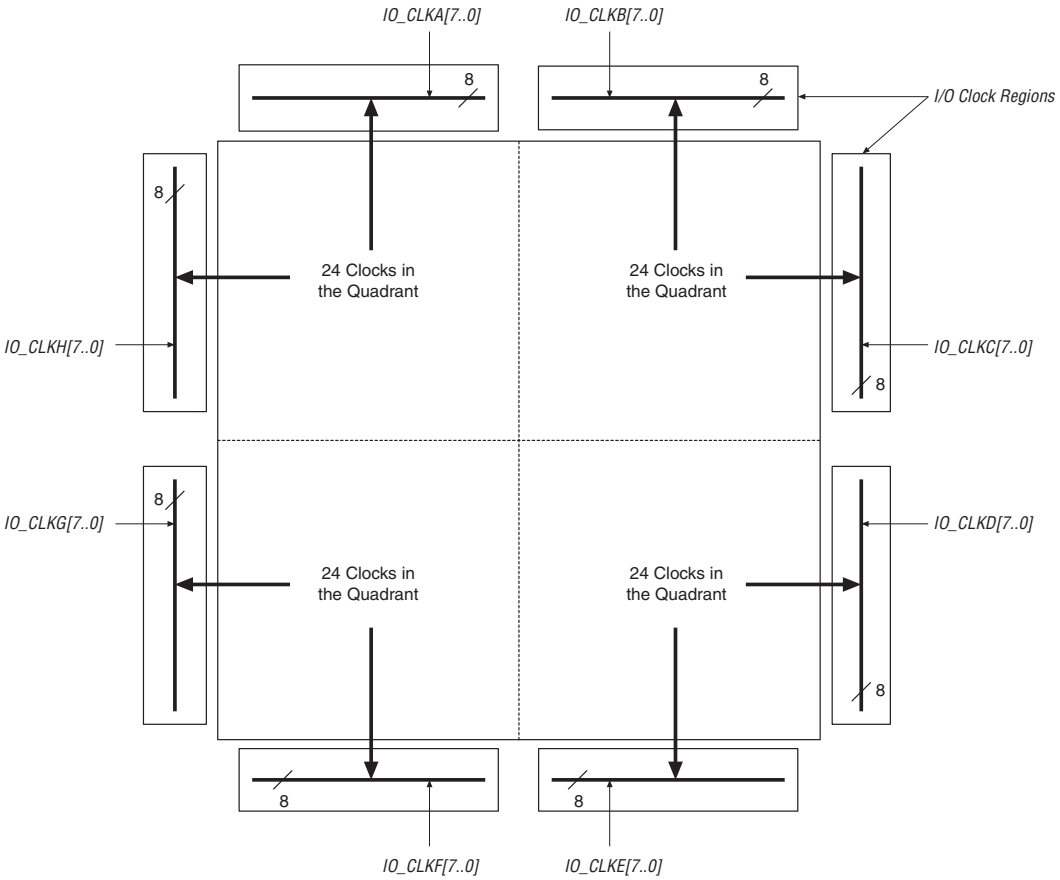
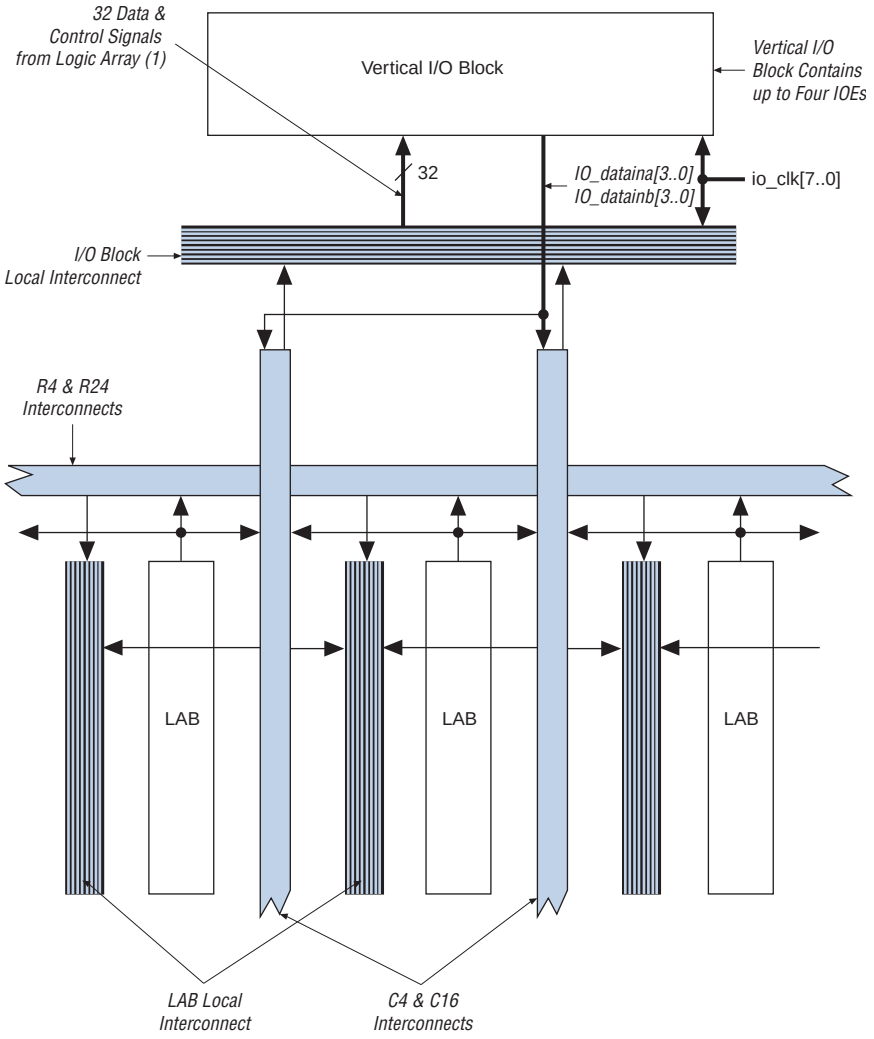


Figure 2–78 shows how a column I/O block connects to the logic array.

Figure 2–78. Column I/O Block Connection to the Interconnect



Note to Figure 2–78:

(1) The 32 data and control signals consist of eight data out lines: four lines each for DDR applications `io_dataouta[3..0]` and `io_dataoutb[3..0]`, four output enables `io_oe[3..0]`, four input clock enables `io_ce_in[3..0]`, four output clock enables `io_ce_out[3..0]`, four clocks `io_clk[3..0]`, four asynchronous clear and preset signals `io_aclr/apreset[3..0]`, and four synchronous clear and preset signals `io_sclr/spreset[3..0]`.

Table 2–42. Document Revision History (Part 2 of 6)

Date and Document Version	Changes Made	Summary of Changes
February 2007 v2.0	Added Chapter 02 “Stratix II GX Transceivers” to the beginning of Chapter 03 “Stratix II GX Architecture”. • Changed chapter number to Chapter 02.	Combined Chapter 02 “Stratix II GX Transceivers” and Chapter 03 “Stratix II GX Architecture” in the new Chapter 02 “Stratix II GX Architecture”
	Added the “Document Revision History” section to this chapter.	
	Moved the “Stratix II GX Transceiver Clocking” section to after the “Receiver Path” section.	

Table 2–42. Document Revision History (Part 5 of 6)

Date and Document Version	Changes Made	Summary of Changes
Previous Chapter 02 changes: June 2006, v1.2	• Updated notes 1 and 2 in Figure 2–1. • Updated "Byte Serializer" section. • Updated Tables 2–4, 2–7, and 2–16. • Updated "Programmable Output Driver" section. • Updated Figure 2–12. • Updated "Programmable Pre-Emphasis" section. • Added Table 2–11. • Added "Dynamic Reconfiguration" section. • Added "Calibration Block" section. • Updated "Programmable Equalizer" section, including addition of Figure 2–18.	Updated input frequency range in Table 2–4.
Previous Chapter 02 changes: April 2006, v1.1	• Updated Figure 2–3. • Updated Figure 2–7. • Updated Table 2–4. • Updated "Transmit Buffer" section.	Updated input frequency range in Table 2–4.
Previous Chapter 02 changes: October 2005 v1.0	Added chapter to the *Stratix II GX Device Handbook*.	
Previous Chapter 03 changes: August 2006, v1.4	• Updated Table 3–18 with note.	
Previous Chapter 03 changes: June 2006, v1.3	• Updated note 2 in Figure 3–41. • Updated column title in Table 3–21.	
Previous Chapter 03 changes: April 2006, v1.2	• Updated note 1 in Table 3–9. • Updated note 1 in Figure 3–40. • Updated note 2 in Figure 3–41. • Updated Table 3–16. • Updated Figure 3–56. • Updated Tables 3–19 through 3–22. • Updated Tables 3–25 and 3–26. • Updated "Fast PLL & Channel Layout" section.	Added 1,152-pin FineLine BGA package information for EP2SGX60 device in Table 3–16.

considerable flexibility for frequency synthesis, allowing real-time variation of the PLL frequency and delay. The rest of the device is functional while reconfiguring the PLL.

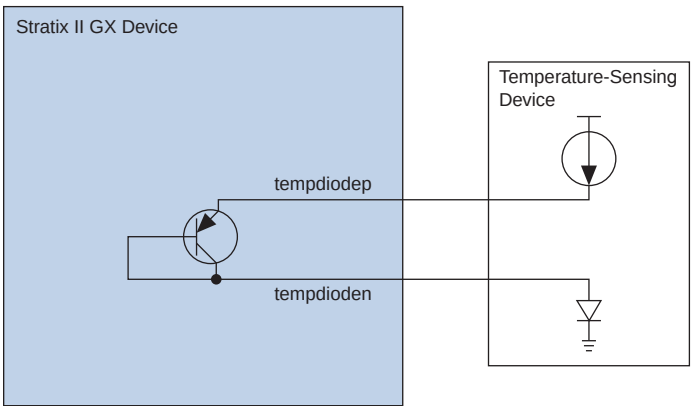
See the *PLLs in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook* for more information on Stratix II GX PLLs.

Temperature Sensing Diode (TSD)

Stratix II GX devices include a diode-connected transistor for use as a temperature sensor in power management. This diode is used with an external digital thermometer device. These devices steer bias current through the Stratix II GX diode, measuring forward voltage and converting this reading to temperature in the form of an 8-bit signed number (7 bits plus 1 sign bit). The external device's output represents the junction temperature of the Stratix II GX device and can be used for intelligent power management.

The diode requires two pins (`tempdiodep` and `tempdioden`) on the Stratix II GX device to connect to the external temperature-sensing device, as shown in Figure 3–1. The temperature sensing diode is a passive element and therefore can be used before the Stratix II GX device is powered.

Figure 3–1. External Temperature-Sensing Diode



4. DC and Switching Characteristics

SIIGX51006-4.6

Operating Conditions

Stratix® II GX devices are offered in both commercial and industrial grades. Industrial devices are offered in -4 speed grade and commercial devices are offered in -3 (fastest), -4, and -5 speed grades.

Tables 4–1 through 4–51 provide information on absolute maximum ratings, recommended operating conditions, DC electrical characteristics, and other specifications for Stratix II GX devices.

Absolute Maximum Ratings

Table 4–1 contains the absolute maximum ratings for the Stratix II GX device family.

Table 4–1. Stratix II GX Device Absolute Maximum Ratings *Notes (1), (2), (3)*

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage	With respect to ground	–0.5	1.8	V
V_{CCIO}	Supply voltage	With respect to ground	–0.5	4.6	V
V_{CCPD}	Supply voltage	With respect to ground	–0.5	4.6	V
V_I	DC input voltage *(4)*		–0.5	4.6	V
I_{OUT}	DC output current, per pin		–25	40	mA
T_{STG}	Storage temperature	No bias	–65	150	C
T_J	Junction temperature	BGA packages under bias	–55	125	C

Notes to Table 4–1:

(1) See the *Operating Requirements for Altera Devices Data Sheet* for more information.

(2) Conditions beyond those listed in Table 4–1 may cause permanent damage to a device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse affects on the device.

(3) Supply voltage specifications apply to voltage readings taken at the device pins, not at the power supply.

(4) During transitions, the inputs may overshoot to the voltage shown in Table 4–2 based upon the input duty cycle. The DC case is equivalent to 100% duty cycle. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Table 4–6. Stratix II GX Transceiver Block AC Specification (Part 5 of 6)

Symbol / Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Data rate		600	-	6375	600	-	5000	600	-	4250	Mbps
V_{OCM}	V_{OCM} = 0.6 V setting	580±10%			580±10%			580±10%			mV
	V_{OCM} = 0.7 V setting	680±10%			680±10%			680±10%			mV
On-chip termination resistors	100 Ω setting	108±10%			108±10%			108±10%			Ω
	120 Ω setting	125±10%			125±10%			125±10%			Ω
	150 Ω setting	152±10%			152±10%			152±10%			Ω
Return loss differential mode	312 MHz to 625 MHz (XAUI): -10 dB 625 MHz to 3.125 GHz (XAUI): -10 dB/decade slope 50 MHz to 1.25 GHz (PCI-E): -10dB 100 MHz to 4.875 GHz (OIF/CEI): -8db 4.875 GHz to 10 GHz (OIF/CEI): 16.6 dB/decade slope										
Return loss common mode	50 MHz to 1.25 GHz (PCI-E): -6dB 100 MHz to 4.875 GHz (OIF/CEI): -6db 4.875 GHz to 10 GHz (OIF/CEI): 16.6 dB/decade slope										
Rise time		35	-	65	35	-	65	35	-	65	ps
Fall time		35	-	65	35	-	65	35	-	65	ps
Intra differential pair skew	V_{OD} = 800 mV	-	-	15	-	-	15	-	-	15	ps
Intra-transceiver block skew (x4)		-	-	100	-	-	100	-	-	100	ps
Inter-transceiver block skew (x8)		-	-	300	-	-	300	-	-	300	ps
TXPLL (TXPLL0 and TXPLL1)											
VCO frequency range (low gear)		500	-	1562.5	500	-	1562.5	500	-	1562.5	MHz
VCO frequency range (high gear)		1562.5		3187.5	1562.5		2500	1562.5	-	2125	MHz

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 3 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Fibre Channel Transmit Jitter Generation *(8), (17)*											
Total jitter FC-1	REFCLK = 106.25 MHz Pattern = CRPAT V_{OD} = 800 mV No Pre-emphasis	-	-	0.23	-	-	0.23	-	-	0.23	UI
Deterministic jitter FC-1	REFCLK = 106.25 MHz Pattern = CRPAT V_{OD} = 800 mV No Pre-emphasis	-	-	0.11	-	-	0.11	-	-	0.11	UI
Total jitter FC-2	REFCLK = 106.25 MHz Pattern = CRPAT V_{OD} = 800 mV No Pre-emphasis	-	-	0.33	-	-	0.33	-	-	0.33	UI
Deterministic jitter FC-2	REFCLK = 106.25 MHz Pattern = CRPAT V_{OD} = 800 mV No Pre-emphasis	-	-	0.2	-	-	0.2	-	-	0.2	UI
Total jitter FC-4	REFCLK = 106.25 MHz Pattern = CRPAT V_{OD} = 800 mV No Pre-emphasis	-	-	0.52	-	-	0.52	-	-	0.52	UI
Deterministic jitter FC-4	REFCLK = 106.25 MHz Pattern = CRPAT V_{OD} = 800 mV No Pre-emphasis	-	-	0.33	-	-	0.33	-	-	0.33	UI
Fibre Channel Receiver Jitter Tolerance *(8), (18)*											
Deterministic jitter FC-1	Pattern = CJTPAT No Equalization DC Gain = 0 dB	> 0.37			> 0.37			> 0.37			UI
Random jitter FC-1	Pattern = CJTPAT No Equalization DC Gain = 0 dB	> 0.31			> 0.31			> 0.31			UI

Table 4–55 shows the Stratix II GX performance for some common designs. All performance values were obtained with the Quartus II software compilation of LPM or MegaCore functions for FIR and FFT designs.

Table 4–55. Stratix II GX Performance Notes (Part 1 of 3) *Note (1)*

Applications		Resources Used			Performance				
		ALUTs	TriMatrix Memory Blocks	DSP Blocks	-3 Speed Grade (2)	-3 Speed Grade (3)	-4 Speed Grade	-5 Speed Grade	Units
LE	16-to-1 multiplexer (4)	21	0	0	657.03	620.73	589.62	477.09	MHz
	32-to-1 multiplexer (4)	38	0	0	534.75	517.33	472.81	369.27	MHz
	16-bit counter	16	0	0	568.18	539.66	507.61	422.47	MHz
	64-bit counter	64	0	0	242.54	231.0	217.77	180.31	MHz
TriMatrix Memory M512 block	Simple dual-port RAM 32 x 18bit	0	1	0	500.0	476.19	447.22	373.13	MHz
	FIFO 32 x 18 bit	22	1	0	500.00	476.19	460.82	373.13	MHz
TriMatrix Memory M4K block	Simple dual-port RAM 128 x 36bit	0	1	0	540.54	515.46	483.09	401.6	MHz
	True dual-port RAM 128 x 18bit	0	1	0	540.54	515.46	483.09	401.6	MHz
	FIFO 128 x 36 bit	22	1	0	524.10	500.25	466.41	381.38	MHz

To calculate the output toggle rate for a non 0 pF load, use this formula:

The toggle rate for a non 0 pF load

= 1,000 / (1,000/ toggle rate at 0 pF load + derating factor × load value in pF /1,000)

For example, the output toggle rate at 0 pF load for SSTL-18 Class II 20 mA I/O standard is 550 MHz on a -3 device clock output pin. The derating factor is 94 ps/pF. For a 10 pF load the toggle rate is calculated as:

1,000 / (1,000/550 + 94 × 10 /1,000) = 363 (MHz)

Table 4–88 shows the maximum input clock toggle rates for Stratix II GX device column pins.

Table 4–88. Stratix II GX Maximum Input Clock Rate for Column I/O Pins (Part 1 of 2)

I/O Standard	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
LVTTL	500	500	450	MHz
2.5 V	500	500	450	MHz
1.8 V	500	500	450	MHz
1.5 V	500	500	450	MHz
LVCMOS	500	500	450	MHz
SSTL-2 Class I	500	500	500	MHz
SSTL-2 Class II	500	500	500	MHz
SSTL-18 Class I	500	500	500	MHz
SSTL-18 Class I I	500	500	500	MHz
1.5-V HSTL Class I	500	500	500	MHz
1.5-V HSTL Class I I	500	500	500	MHz
1.8-V HSTL Class I	500	500	500	MHz
1.8-V HSTL Class II	500	500	500	MHz
PCI	500	500	450	MHz
PCI-X	500	500	450	MHz
Differential SSTL-2 Class I	500	500	500	MHz
Differential SSTL-2 Class II	500	500	500	MHz
Differential SSTL-18 Class I	500	500	500	MHz

Table 4–89. Stratix II GX Maximum Input Clock Rate for Row I/O Pins (Part 2 of 2)				
I/O Standard	**-3 Speed Grade**	**-4 Speed Grade**	**-5 Speed Grade**	**Unit**
Differential SSTL-2 Class II	500	500	500	MHz
Differential SSTL-18 Class I	500	500	500	MHz
Differential SSTL-18 Class I I	500	500	500	MHz
1.8-V differential HSTL Class I	500	500	500	MHz
1.8-V differential HSTL Class I I	500	500	500	MHz
1.5-V differential HSTL Class I	500	500	500	MHz
1.5-V differential HSTL Class II	500	500	500	MHz
LVDS *(1)*	520	520	420	MHz
HyperTransport	520	520	420	MHz

(1) The parameters are only available on the left side of the device.

Table 4–90 shows the maximum input clock toggle rates for Stratix II GX device dedicated clock pins.

Table 4–90. Stratix II GX Maximum Input Clock Rate for Dedicated Clock Pins (Part 1 of 2)				
I/O Standard	**-3 Speed Grade**	**-4 Speed Grade**	**-5 Speed Grade**	**Unit**
LVTTL	500	500	400	MHz
2.5 V	500	500	400	MHz
1.8 V	500	500	400	MHz
1.5 V	500	500	400	MHz
LVCMOS	500	500	400	MHz
SSTL-2 Class I	500	500	500	MHz
SSTL-2 Class II	500	500	500	MHz
SSTL-18 Class I	500	500	500	MHz
SSTL-18 Class II	500	500	500	MHz
1.5-V HSTL Class I	500	500	500	MHz
1.5-V HSTL Class II	500	500	500	MHz
1.8-V HSTL CLass I	500	500	500	MHz

Table 4–96. Stratix II GX Maximum Output Clock Rate for Dedicated Clock Pins (Series Termination) (Part 2 of 2)

I/O Standard	Drive Strength	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
SSTL-18 Class II	OCT_25_OHMS	550	500	450	MHz
1.5-V HSTL Class I	OCT_50_OHMS	600	550	500	MHz
1.8-V HSTL Class I	OCT_50_OHMS	650	600	600	MHz
1.8-V HSTL Class II	OCT_25_OHMS	500	500	450	MHz
DIfferential SSTL-2 Class I	OCT_50_OHMS	600	500	500	MHz
DIfferential SSTL-2 Class II	OCT_25_OHMS	600	550	500	MHz
DIfferential SSTL-18 Class I	OCT_50_OHMS	560	400	350	MHz
DIfferential SSTL-18 Class II	OCT_25_OHMS	550	500	450	MHz
1.8-V differential HSTL Class I	OCT_50_OHMS	650	600	600	MHz
1.8-V differential HSTL Class II	OCT_25_OHMS	500	500	450	MHz
1.5-V differential HSTL Class I	OCT_50_OHMS	600	550	500	MHz

Table 4–97 specifies the derating factors for the output clock toggle rate for a non 0 pF load.

Table 4–97. Maximum Output Clock Toggle Rate Derating Factors (Part 1 of 5)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate Derating Factors (ps/pF)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		-3	-4	-5	-3	-4	-5	-3	-4	-5
3.3-V LVTTL	4 mA	478	510	510	478	510	510	466	510	510
	8 mA	260	333	333	260	333	333	291	333	333
	12 mA	213	247	247	213	247	247	211	247	247
	16 mA	136	197	197	-	-	-	166	197	197
	20 mA	138	187	187	-	-	-	154	187	187
	24 mA	134	177	177	-	-	-	143	177	177

Table 4–112. DLL Frequency Range Specifications (Part 2 of 2)		
Frequency Mode	**Frequency Range (MHz)**	**Resolution (Degrees)**
3	240 to 400 (–3 speed grade)	36
	240 to 350 (–4 and –5 speed grade)	36

Table 4–113. DQS Jitter Specifications for DLL-Delayed Clock (t_{DQS_JITTER}) Note (1)		
Number of DQS Delay Buffer Stages *(2)*	**Commercial (ps)**	**Industrial (ps)**
1	80	110
2	110	130
3	130	180
4	160	210

(1) Peak-to-peak period jitter on the phase-shifted DQS clock. For example, jitter on two delay stages under commercial conditions is 200 ps peak-to-peak or 100 ps.
(2) Delay stages used for requested DQS phase shift are reported in a project's Compilation Report in the Quartus II software.

Table 4–114. DQS Phase-Shift Error Specifications for DLL-Delayed Clock (t_{DQS_PSERR})			
Number of DQS Delay Buffer Stages *(1)*	**–3 Speed Grade (ps)**	**–4 Speed Grade (ps)**	**–5 Speed Grade (ps)**
1	25	30	35
2	50	60	70
3	75	90	105
4	100	120	140

(1) Delay stages used for request DQS phase shift are reported in a project's Compilation Report in the Quartus II software. For example, phase-shift error on two delay stages under -3 conditions is 50 ps peak-to-peak or 25 ps.