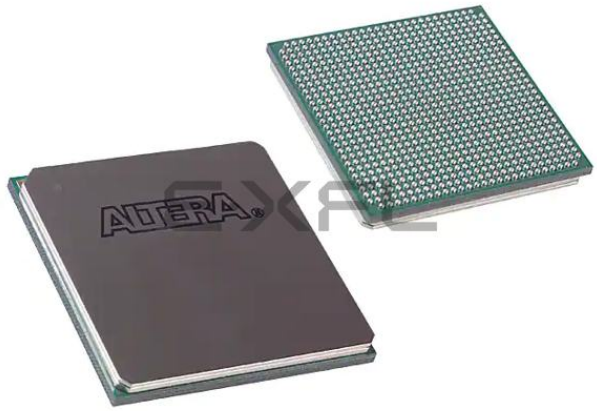

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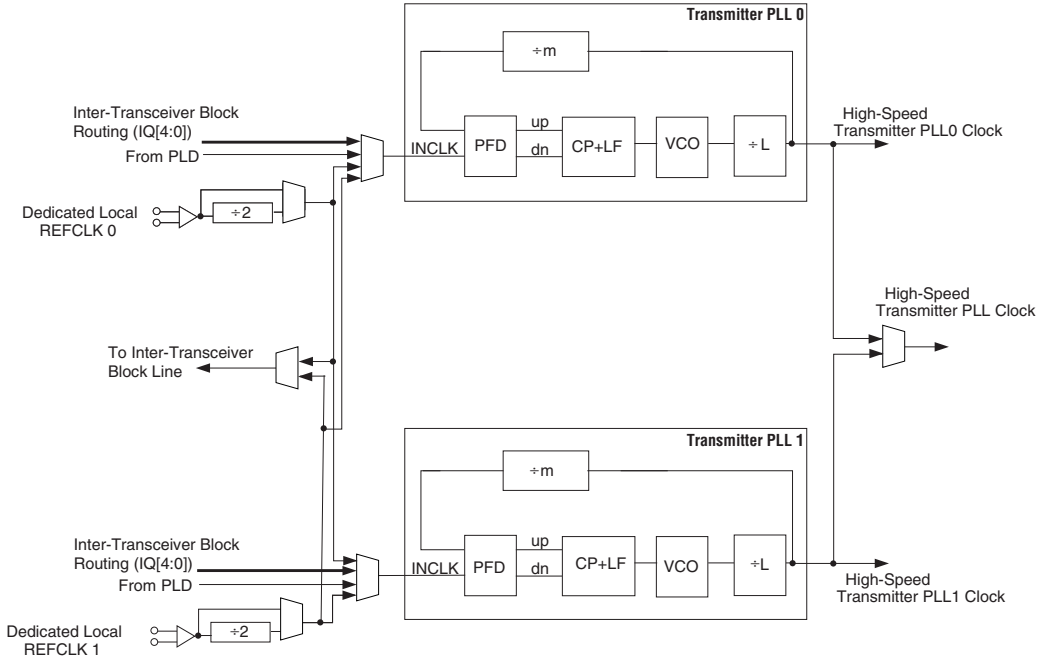
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1694
Number of Logic Elements/Cells	33880
Total RAM Bits	1369728
Number of I/O	361
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	780-BBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2sgx30df780c3

Figure 2–4. Transmitter PLL Block Note (1)



Note to Figure 2–4:
(1) The global clock line must be driven by an input pin.

The transmitter PLLs support data rates up to 6.375 Gbps. The input clock frequency is limited to 622.08 MHz. An optional `pll_locked` port is available to indicate whether the transmitter PLL is locked to the reference clock. Both transmitter PLLs have a programmable loop bandwidth parameter that can be set to low, medium, or high. The loop bandwidth parameter can be statically set in the Quartus II software.

Table 2–2 lists the adjustable parameters in the transmitter PLL.

Table 2–2. Transmitter PLL Specifications

Parameter	Specifications
Input reference frequency range	50 MHz to 622.08 MHz
Data rate support	600 Mbps to 6.375 Gbps
Multiplication factor (W)	1, 4, 5, 8, 10, 16, 20, 25
Bandwidth	Low, medium, or high

Transmit State Machine

The transmit state machine operates in either PCI Express mode, XAUI mode, or GIGE mode, depending on the protocol used. The state machine is not utilized for certain protocols, such as SONET.

GIGE Mode

In GIGE mode, the transmit state machine converts all idle ordered sets (/K28.5/, /Dx.y/) to either /I1/ or /I2/ ordered sets. /I1/ consists of a negative-ending disparity /K28.5/ (denoted by /K28.5/-) followed by a neutral /D5.6/. /I2/ consists of a positive-ending disparity /K28.5/ (denoted by /K28.5/+) and a negative-ending disparity /D16.2/ (denoted by /D16.2/-). The transmit state machines do not convert any of the ordered sets to match /C1/ or /C2/, which are the configuration ordered sets. (/C1/ and /C2/ are defined by [/K28.5/, /D21.5/] and [/K28.5/, /D2.2/], respectively). Both the /I1/ and /I2/ ordered sets guarantee a negative-ending disparity after each ordered set.

XAUI Mode

The transmit state machine translates the XAUI XGMII code group to the XAUI PCS code group. Table 2–5 shows the code conversion.

Table 2–5. Code Conversion

XGMII TXC	XGMII TXD	PCS Code-Group	Description
0	00 through FF	Dxx.y	Normal data
1	07	K28.0 or K28.3 or K28.5	Idle in ||**I**||
1	07	K28.5	Idle in ||**T**||
1	9C	K28.4	Sequence
1	FB	K27.7	Start
1	FD	K29.7	Terminate
1	FE	K30.7	Error
1	See IEEE 802.3 reserved code groups	See IEEE 802.3 reserved code groups	Reserved code groups
1	Other value	K30.7	Invalid XGMII character

The XAUI PCS idle code groups, /K28.0/ (/R/) and /K28.5/ (/K/), are automatically randomized based on a PRBS7 pattern with an $x^7 + x^6 + 1$ polynomial. The /K28.3/ (/A/) code group is automatically generated between 16 and 31 idle code groups. The idle randomization on the /A/, /K/, and /R/ code groups is done automatically by the transmit state machine.

.

Table 2–15. Available Clocking Connections for Transceivers in 2SGX130G

Region	Clock Resource		Transceiver				
	Global Clock	Regional Clock	Bank 13 8 Clock I/O	Bank 14 8 Clock I/O	Bank 15 8 clock I/O	Bank 16 8 Clock I/O	Bank 17 8 Clock I/O
Region0 8 LRIO clock	✓	RCLK 20-27	✓				
Region1 8 LRIO clock	✓	RCLK 20-27		✓			
Region2 8 LRIO clock	✓	RCLK 12-19			✓	✓	
Region3 8 LRIO clock	✓	RCLK 12-19				✓	✓

Other Transceiver Features

Other important features of the Stratix II GX transceivers are the power down and reset capabilities, external voltage reference and bias circuitry, and hot swapping.

Calibration Block

The Stratix II GX device uses the calibration block to calibrate the on-chip termination for the PLLs and their associated output buffers and the terminating resistors on the transceivers. The calibration block counters the effects of process, voltage, and temperature (PVT). The calibration block references a derived voltage across an external reference resistor to calibrate the on-chip termination resistors on the Stratix II GX device. The calibration block can be powered down. However, powering down the calibration block during operations may yield transmit and receive data errors.

Dynamic Reconfiguration

This feature allows you to dynamically reconfigure the PMA portion and the channel parameters, such as data rate and functional mode, of the Stratix II GX transceiver. The PMA reconfiguration allows you to quickly optimize the settings for the transceiver's PMA to achieve the intended bit error rate (BER).

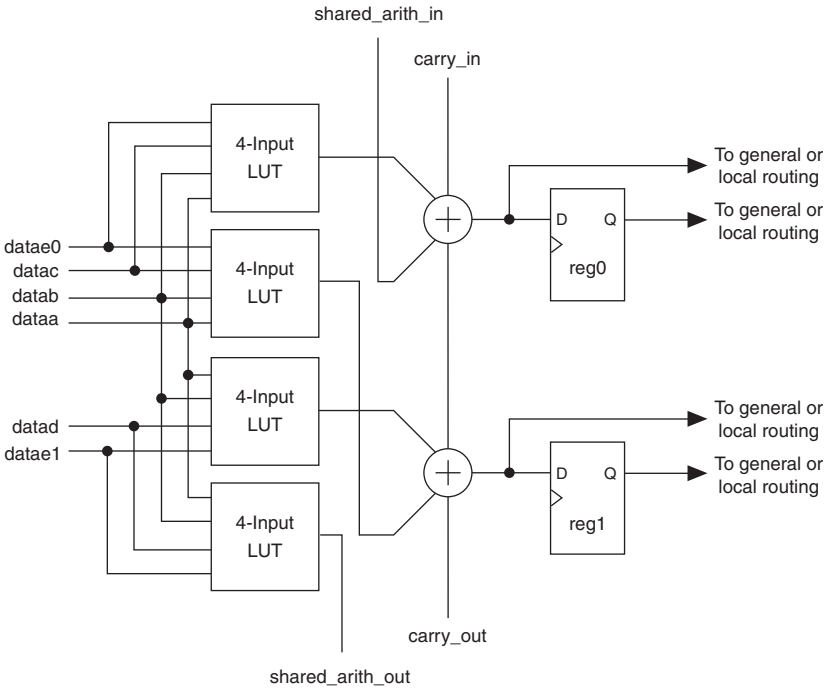
asynchronous clear, asynchronous preset/load, synchronous clear, synchronous load, and clock enable control for the register. These LAB wide signals are available in all ALM modes. Refer to "LAB Control Signals" on page 2–46 for more information on the LAB-wide control signals.

The Quartus II software and supported third-party synthesis tools, in conjunction with parameterized functions such as library of parameterized modules (LPM) functions, automatically choose the appropriate mode for common functions such as counters, adders, subtractors, and arithmetic functions. If required, you can also create special-purpose functions that specify which ALM operating mode to use for optimal performance.

Normal Mode

The normal mode is suitable for general logic applications and combinational functions. In this mode, up to eight data inputs from the LAB local interconnect are inputs to the combinational logic. The normal mode allows two functions to be implemented in one Stratix II GX ALM, or an ALM to implement a single function of up to six inputs. The ALM can support certain combinations of completely independent functions and various combinations of functions which have common inputs. Figure 2–37 shows the supported LUT combinations in normal mode.

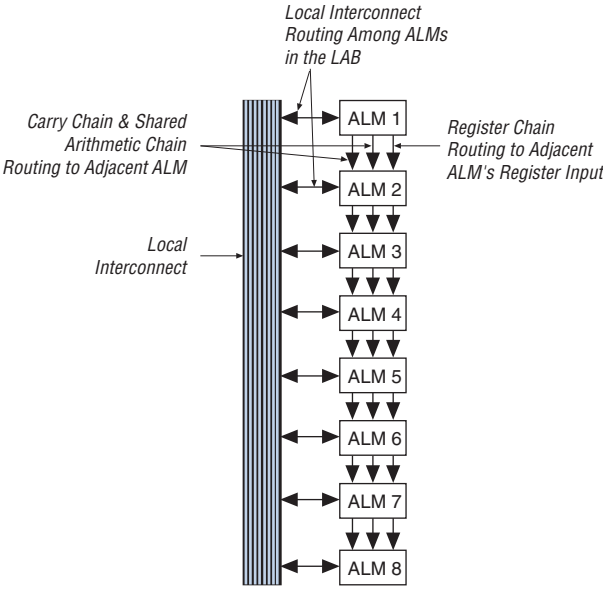
Figure 2–43. ALM in Shared Arithmetic Mode



Note to Figure 2–43:
(1) Inputs `dataf0` and `dataf1` are available for register packing in shared arithmetic mode.

Adder trees are used in many different applications. For example, the summation of the partial products in a logic-based multiplier can be implemented in a tree structure. Another example is a correlator function that can use a large adder tree to sum filtered data samples in a given time frame to recover or to de-spread data which was transmitted utilizing spread spectrum technology. An example of a three-bit add operation utilizing the shared arithmetic mode is shown in Figure 2–44. The partial sum (`S[2..0]`) and the partial carry (`C[2..0]`) is obtained using the LUTs, while the result (`R[2..0]`) is computed using the dedicated adders.

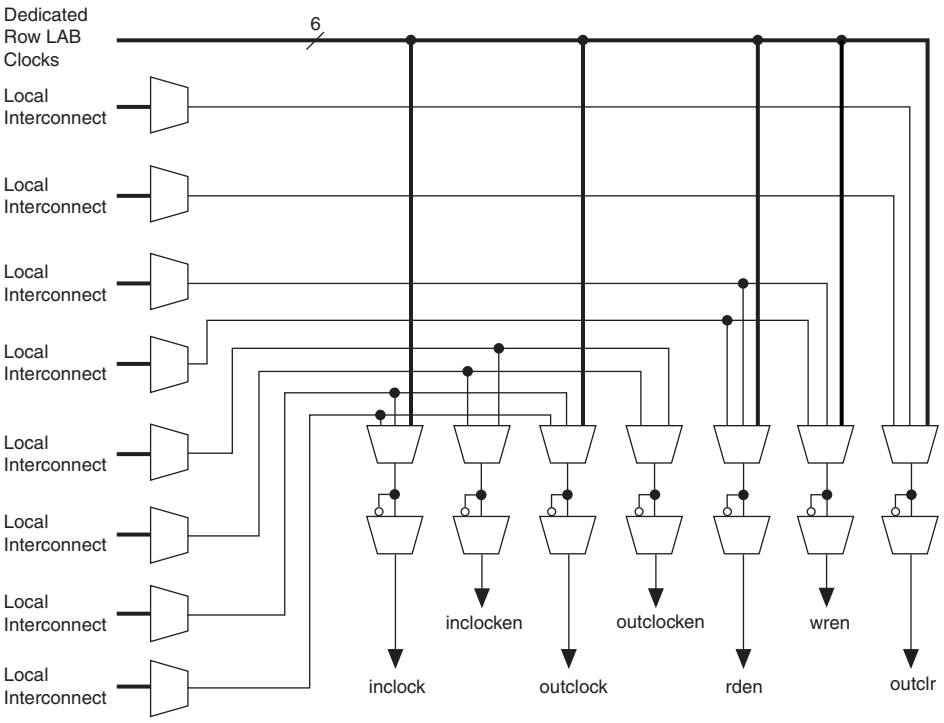
Figure 2–47. Shared Arithmetic Chain, Carry Chain and Register Chain Interconnects



The C4 interconnects span four LABs, M512, or M4K blocks up or down from a source LAB. Every LAB has its own set of C4 interconnects to drive either up or down. Figure 2–48 shows the C4 interconnect connections from a LAB in a column. The C4 interconnects can drive and be driven by all types of architecture blocks, including DSP blocks, TriMatrix memory blocks, and column and row IOEs. For LAB interconnection, a primary LAB or its LAB neighbor can drive a given C4 interconnect. C4 interconnects can drive each other to extend their range as well as drive row interconnects for column-to-column connections.

M512 RAM blocks can have different clocks on its inputs and outputs. The wren, datain, and write address registers are all clocked together from one of the two clocks feeding the block. The read address, rden, and output registers can be clocked by either of the two clocks driving the block, allowing the RAM block to operate in read and write or input and output clock modes. Only the output register can be bypassed. The six labclk signals or local interconnect can drive the inclock, outclock, wren, rden, and outclr signals. Because of the advanced interconnect between the LAB and M512 RAM blocks, ALMs can also control the wren and rden signals and the RAM clock, clock enable, and asynchronous clear signals. Figure 2–49 shows the M512 RAM block control signal generation logic.

Figure 2–49. M512 RAM Block Control Signals



The connections to the global and regional clocks from the top clock pins and enhanced PLL outputs are shown in Table 2–28. The connections to the clocks from the bottom clock pins are shown in Table 2–29.

Table 2–28. Global and Regional Clock Connections from Top Clock Pins and Enhanced PLL Outputs (Part 1 of 2)

Top Side Global and Regional Clock Network Connectivity	DLLCLK	CLK12	CLK13	CLK14	CLK15	RCLK24	RCLK25	RCLK26	RCLK27	RCLK28	RCLK29	RCLK30	RCLK31
Clock pins													
CLK12p	✓	✓	✓			✓				✓			
CLK13p	✓	✓	✓				✓				✓		
CLK14p	✓			✓	✓			✓				✓	
CLK15p	✓			✓	✓				✓				✓
CLK12n		✓				✓				✓			
CLK13n			✓				✓				✓		
CLK14n				✓				✓				✓	
CLK15n					✓				✓				✓
Drivers from internal logic													
GCLKDRV0		✓											
GCLKDRV1			✓										
GCLKDRV2				✓									
GCLKDRV3					✓								
RCLKDRV0						✓				✓			
RCLKDRV1							✓				✓		
RCLKDRV2								✓				✓	
RCLKDRV3									✓				✓
RCLKDRV4						✓				✓			
RCLKDRV5							✓				✓		
RCLKDRV6								✓				✓	
RCLKDRV7									✓				✓
Enhanced PLL5 outputs													
c0	✓	✓	✓			✓				✓			
c1	✓	✓	✓				✓				✓		

Table 3–1. Stratix II GX JTAG Instructions

JTAG Instruction	Instruction Code	Description
SAMPLE/PRELOAD	00 0000 0101	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation and permits an initial data pattern to be output at the device pins. Also used by the SignalTap II embedded logic analyzer.
EXTEST *(1)*	00 0000 1111	Allows the external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	11 1111 1111	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	00 0000 0111	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	00 0000 0110	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
HIGHZ *(1)*	00 0000 1011	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins.
CLAMP *(1)*	00 0000 1010	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding the I/O pins to a state defined by the data in the boundary-scan register.
ICR instructions		Used when configuring a Stratix II GX device via the JTAG port with a USB-Blaster™, MasterBlaster™, ByteBlasterMV™, or ByteBlaster II download cable, or when using a **.jam** or **.jbc** via an embedded processor or JRunner.
PULSE_NCONFIG	00 0000 0001	Emulates pulsing the nCONFIG pin low to trigger reconfiguration even though the physical pin is unaffected.
CONFIG_IO *(2)*	00 0000 1101	Allows configuration of I/O standards through the JTAG chain for JTAG testing. Can be executed before, during, or after configuration. Stops configuration if executed during configuration. Once issued, the CONFIG_IO instruction holds nSTATUS low to reset the configuration device. nSTATUS is held low until the IOE configuration register is loaded and the TAP controller state machine transitions to the UPDATE_DR state.
SignalTap II instructions		Monitors internal device operation with the SignalTap II embedded logic analyzer.

Notes to Table 3–1:

(1) Bus hold and weak pull-up resistor features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.

(2) For more information on using the CONFIG_IO instruction, refer to the *MorphIO: An I/O Reconfiguration Solution for Altera Devices White Paper.*

Table 4–8. Typical V_{OD} Setting, TX Term = 120 Ω Note (1)					
V_{CCH} TX = 1.5 V	**V_{OD} Setting (mV)**				
	240	**480**	**720**	**960**	**1200**
V_{OD} Typical (mV)	260	510	750	975	1200

Note to Table 4–8:
(1) Applicable to data rates from 600 Mbps to 6.375 Gbps. Specification is for measurement at the package ball.

Table 4–9. Typical V_{OD} Setting, TX Term = 150 Ω Note (1)				
V_{CCH} TX = 1.5 V	**V_{OD} Setting (mV)**			
	300	**600**	**900**	**1200**
V_{OD} Typical (mV)	325	625	920	1200

Note to Table 4–9:
(1) Applicable to data rates from 600 Mbps to 6.375 Gbps. Specification is for measurement at the package ball.

Table 4–10. Typical V_{OD} Setting, TX Term = 100 Ω Note (1)					
V_{CCH} TX = 1.2 V	**V_{OD} Setting (mV)**				
	320	**480**	**640**	**800**	**960**
V_{OD} Typical (mV)	344	500	664	816	960

Note to Table 4–10:
(1) Applicable to data rates from 600 Mbps to 3.125 Gbps. Specification is for measurement at the package ball.

Table 4–11. Typical V_{OD} Setting, TX Term = 120 Ω Note (1)					
V_{CCH} TX = 1.2 V	V_{OD} Setting (mV)				
	192	384	576	768	960
V_{OD} Typical (mV)	210	410	600	780	960

Note to Table 4–11:
(1) Applicable to data rates from 600 Mbps to 3.125 Gbps. Specification is for measurement at the package ball.

Table 4–12. Typical V_{OD} Setting, TX Term = 150 Ω Note (1)				
V_{CCH} TX = 1.2 V	V_{OD} Setting (mV)			
	240	480	720	960
V_{OD} Typical (mV)	260	500	730	960

Note to Table 4–12:
(1) Applicable to data rates from 600 Mbps to 3.125 Gbps. Specification is for measurement at the package ball.

Tables 4–13 through 4–18 show the typical first post-tap pre-emphasis.

Table 4–13. Typical Pre-Emphasis (First Post-Tap), Note (1) (Part 1 of 2)												
V_{CCH} TX = 1.5 V	First Post Tap Pre-Emphasis Level											
V_{OD} Setting (mV)	1	2	3	4	5	6	7	8	9	10	11	12
	TX Term = 100 Ω											
400	24%	62%	112%	184%								
600		31%	56%	86%	122%	168%	230%	329%	457%			
800		20%	35%	53%	73%	96%	123%	156%	196%	237%	312%	387%
1000			23%	36%	49%	64%	79%	97%	118%	141%	165%	200%
1200			17%	25%	35%	45%	56%	68%	82%	95%	110%	125%

Table 4–17. Typical Pre-Emphasis (First Post-Tap), Note (1)

V_{CCH} TX = 1.2 V	First Post Tap Pre-Emphasis Level											
V_{OD} Setting (mV)	1	2	3	4	5	6	7	8	9	10	11	12
	TX Term = 120 Ω											
192	45%											
384		41%	76%	114%	166%	257%	355%					
576		23%	38%	55%	84%	108%	137%	179%	226%	280%	405%	477%
768		15%	24%	36%	47%	64%	80%	97%	122%	140%	170%	196%
960			18%	22%	30%	41%	51%	63%	77%	86%	98%	116%

Note to Table 4–17:
(1) Applicable to data rates from 600 Mbps to 3.125 Gbps. Specification is for measurement at the package ball.

Table 4–18. Typical Pre-Emphasis (First Post-Tap), Note (1)

V_{CCH} TX = 1.2 V	First Post Tap Pre-Emphasis Level											
V_{OD} Setting (mV)	1	2	3	4	5	6	7	8	9	10	11	12
	TX Term = 150 Ω											
240	31%	85%										
480		32%	52%	78%	112%	152%	195%	275%				
720		19%	28%	37%	56%	68%	86%	108%	133%	169%	194%	239%
960			17%	22%	30%	39%	51%	59%	75%	85%	94%	109%

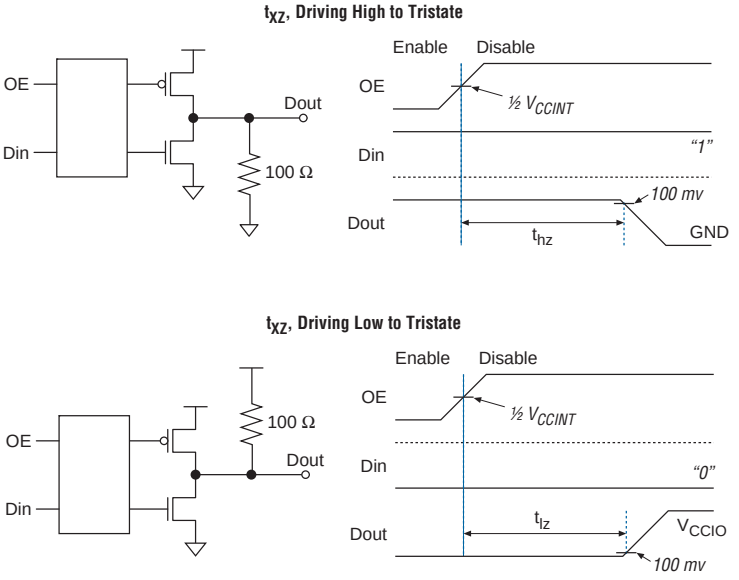
Note to Table 4–18:
(1) Applicable to data rates from 600 Mbps to 3.125 Gbps. Specification is for measurement at the package ball.

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 8 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
GIGE Transmit Jitter Generation *(12)*											
Deterministic Jitter (peak-to-peak)	Data Rate = 1.25 Gbps REFCLK = 125 MHz Pattern = CRPAT V_{OD} = 1400 mV No Pre-emphasis	-	-	0.14	-	-	0.14	-	-	0.14	UI
Total Jitter (peak-to-peak)	Data Rate = 1.25 Gbps REFCLK = 125 MHz Pattern = CRPAT V_{OD} = 1400 mV No Pre-emphasis	-	-	0.279	-	-	0.279	-	-	0.279	UI
GIGE Receiver Jitter Tolerance *(12)*											
Deterministic Jitter Tolerance (peak-to-peak)	Data Rate = 1.25 Gbps REFCLK = 125 MHz Pattern = CJPAT No Equalization	> 0.4			> 0.4			> 0.4			UI
Combined Deterministic and Random Jitter Tolerance (peak-to-peak)	Data Rate = 1.25 Gbps REFCLK = 125 MHz Pattern = CJPAT No Equalization	> 0.66			> 0.66			> 0.66			UI
HiGig Transmit Jitter Generation *(4), (13)*											
Deterministic Jitter (peak-to-peak)	Data Rate = 3.75 Gbps REFCLK = 187.5 MHz Pattern = CJPAT V_{OD} = 1200 mV No Pre-emphasis	-	-	0.17	-						UI
Total Jitter (peak-to-peak)	Data Rate = 3.75 Gbps REFCLK = 187.5 MHz Pattern = CJPAT V_{OD} = 1200 mV No Pre-emphasis	-	-	0.35	-						UI

Figures 4–9 and 4–10 show the measurement setup for output disable and output enable timing.

Figure 4–9. Measurement Setup for t_{xz} *Note (1)*



Note to Figure 4–9:

(1) V_{CCINT} is 1.12 V for this measurement.

Figure 4–10. Measurement Setup for t_{zx}

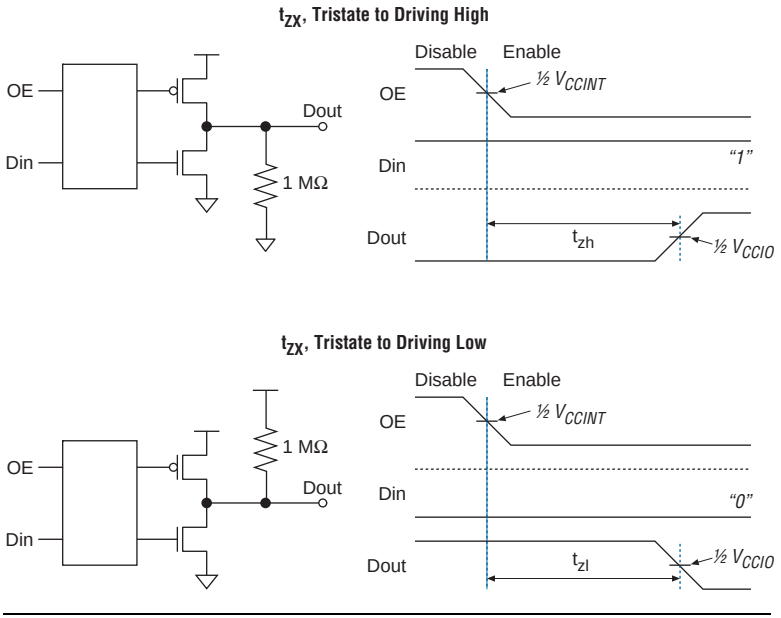


Table 4–54 specifies the input timing measurement setup.

Table 4–54. Timing Measurement Methodology for Input Pins (Part 1 of 2) *Notes (1), (2), (3), (4)*

I/O Standard	Measurement Conditions			Measurement Point
	V_{CCIO} (V)	V_{REF} (V)	Edge Rate (ns)	VMEAS (V)
LVTTL *(5)*	3.135		3.135	1.5675
LVCMOS *(5)*	3.135		3.135	1.5675
2.5 V *(5)*	2.375		2.375	1.1875
1.8 V *(5)*	1.710		1.710	0.855
1.5 V *(5)*	1.425		1.425	0.7125
PCI *(6)*	2.970		2.970	1.485
PCI-X *(6)*	2.970		2.970	1.485
SSTL-2 Class I	2.325	1.163	2.325	1.1625
SSTL-2 Class II	2.325	1.163	2.325	1.1625
SSTL-18 Class I	1.660	0.830	1.660	0.83
SSTL-18 Class II	1.660	0.830	1.660	0.83
1.8-V HSTL Class I	1.660	0.830	1.660	0.83

Table 4–61. M-RAM Block Internal Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	-3 Speed Grade *(2)*		-3 Speed Grade *(3)*		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{MEGABESU}$	Byte enable setup time before clock	-9		-10		-11		-13		ps
$t_{MEGABEH}$	Byte enable hold time after clock	39		40		43		52		ps
$t_{MEGADATAASU}$	A port data setup time before clock	50		52		55		67		ps
$t_{MEGADATAAH}$	A port data hold time after clock	243		255		271		325		ps
$t_{MEGAADDRASU}$	A port address setup time before clock	589		618		657		789		ps
$t_{MEGAADDRAH}$	A port address hold time after clock	-347		-365		-388		-465		ps
$t_{MEGADATABSU}$	B port setup time before clock	50		52		55		67		ps
$t_{MEGADATABH}$	B port hold time after clock	243		255		271		325		ps
$t_{MEGAADDRBSU}$	B port address setup time before clock	589		618		657		789		ps
$t_{MEGAADDRBH}$	B port address hold time after clock	-347		-365		-388		-465		ps
$t_{MEGADATACO1}$	Clock-to-output delay when using output registers	480	715	480	749	480	797	480	957	ps
$t_{MEGADATACO2}$	Clock-to-output delay without output registers	1950	2899	1950	3042	1950	3235	1950	3884	ps
$t_{MEGACLKL}$	Minimum clock low time	1250		1312		1395		1675		ps
$t_{MEGACLKH}$	Minimum clock high time	1250		1312		1395		1675		ps
$t_{MEGACLR}$	Minimum clear pulse width	144		151		160		192		ps

(1) The M512 block f_{MAX} obtained using the Quartus II software does not necessarily equal to 1/TMEGARC.
(2) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
(3) This column refers to –3 speed grades for EP2SGX130 devices.

Table 4–84. Stratix II GX I/O Input Delay for Column Pins (Part 2 of 3)

I/O Standard	Parameter	Fast Corner Industrial/ Commercial	-3 Speed Grade *(2)*	-3 Speed Grade *(3)*	-4 Speed Grade	-5 Speed Grade	Unit
2.5 V	t_{PI}	717	1210	1269	1349	1619	ps
	t_{PCOUT}	438	774	812	863	1036	ps
1.8 V	t_{PI}	783	1366	1433	1523	1829	ps
	t_{PCOUT}	504	930	976	1037	1246	ps
1.5 V	t_{PI}	786	1436	1506	1602	1922	ps
	t_{PCOUT}	507	1000	1049	1116	1339	ps
LVCMOS	t_{PI}	707	1223	1282	1364	1637	ps
	t_{PCOUT}	428	787	825	878	1054	ps
SSTL-2 Class I	t_{PI}	530	818	857	912	1094	ps
	t_{PCOUT}	251	382	400	426	511	ps
SSTL-2 Class II	t_{PI}	530	818	857	912	1094	ps
	t_{PCOUT}	251	382	400	426	511	ps
SSTL-18 Class I	t_{PI}	569	898	941	1001	1201	ps
	t_{PCOUT}	290	462	484	515	618	ps
SSTL-18 Class II	t_{PI}	569	898	941	1001	1201	ps
	t_{PCOUT}	290	462	484	515	618	ps
1.5-V HSTL Class I	t_{PI}	587	993	1041	1107	1329	ps
	t_{PCOUT}	308	557	584	621	746	ps
1.5-V HSTL Class II	t_{PI}	587	993	1041	1107	1329	ps
	t_{PCOUT}	308	557	584	621	746	ps
1.8-V HSTL Class I	t_{PI}	569	898	941	1001	1201	ps
	t_{PCOUT}	290	462	484	515	618	ps
1.8-V HSTL Class II	t_{PI}	569	898	941	1001	1201	ps
	t_{PCOUT}	290	462	484	515	618	ps
PCI	t_{PI}	712	1214	1273	1354	1625	ps
	t_{PCOUT}	433	778	816	868	1042	ps
PCI-X	t_{PI}	712	1214	1273	1354	1625	ps
	t_{PCOUT}	433	778	816	868	1042	ps
Differential SSTL-2 Class I *(1)*	t_{PI}	530	818	857	912	1094	ps
	t_{PCOUT}	251	382	400	426	511	ps

Table 4–87. Stratix II GX I/O Output Delay for Row Pins (Part 3 of 4)

I/O Standard	Drive Strength	Parameter	Fast Corner Industrial/ Commercial	-3 Speed Grade *(3)*	-3 Speed Grade *(4)*	-4 Speed Grade	-5 Speed Grade	Unit
SSTL-18 Class I	4 mA	t_{OP}	1038	1709	1793	1906	2046	ps
		t_{DIP}	995	1654	1736	1846	1973	ps
	6 mA	t_{OP}	1042	1648	1729	1838	1975	ps
		t_{DIP}	999	1593	1672	1778	1902	ps
	8 mA	t_{OP}	1018	1633	1713	1821	1958	ps
		t_{DIP}	975	1578	1656	1761	1885	ps
	10 mA *(1)*	t_{OP}	1021	1615	1694	1801	1937	ps
		t_{DIP}	978	1560	1637	1741	1864	ps
1.8-V HSTL Class I	4 mA	t_{OP}	1019	1610	1689	1795	1956	ps
		t_{DIP}	976	1555	1632	1735	1883	ps
	6 mA	t_{OP}	1022	1580	1658	1762	1920	ps
		t_{DIP}	979	1525	1601	1702	1847	ps
	8 mA	t_{OP}	1004	1576	1653	1757	1916	ps
		t_{DIP}	961	1521	1596	1697	1843	ps
	10 mA	t_{OP}	1008	1567	1644	1747	1905	ps
		t_{DIP}	965	1512	1587	1687	1832	ps
	12 mA *(1)*	t_{OP}	999	1566	1643	1746	1904	ps
		t_{DIP}	956	1511	1586	1686	1831	ps
1.5-V HSTL Class I	4 mA	t_{OP}	1018	1591	1669	1774	1933	ps
		t_{DIP}	975	1536	1612	1714	1860	ps
	6 mA	t_{OP}	1021	1579	1657	1761	1919	ps
		t_{DIP}	978	1524	1600	1701	1846	ps
	8 mA *(1)*	t_{OP}	1006	1572	1649	1753	1911	ps
		t_{DIP}	963	1517	1592	1693	1838	ps
Differential SSTL-2 Class I	8 mA	t_{OP}	1050	1759	1846	1962	2104	ps
		t_{DIP}	1007	1704	1789	1902	2031	ps
	12 mA	t_{OP}	1026	1694	1777	1889	2028	ps
		t_{DIP}	983	1639	1720	1829	1955	ps
Differential SSTL-2 Class II	16 mA	t_{OP}	992	1581	1659	1763	1897	ps
		t_{DIP}	949	1526	1602	1703	1824	ps

Table 4–93. Stratix II GX Maximum Output Clock Rate for Dedicated Clock Pins (Part 4 of 4)					
I/O Standard	Drive Strength	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
1.8-V differential Class II	16 mA	500	500	450	MHz
	18 mA	550	500	500	MHz
	20 mA	550	550	550	MHz
1.5-V differential Class I	4 mA	350	300	300	MHz
	6 mA	500	500	450	MHz
	8 mA	700	650	600	MHz
	10 mA	700	700	650	MHz
	12 mA	700	700	700	MHz
1.5-V differential Class II	16 mA	600	600	550	MHz
	18 mA	650	600	600	MHz
	20 mA	700	650	600	MHz
HyperTransport	-	300	250	125	MHz
LVPECL	-	450	400	300	MHz

(1) This is the default setting in Quartus II software.

Table 4–94 shows the maximum output clock toggle rate for Stratix II GX device series-terminated column pins.

Table 4–94. Stratix II GX Maximum Output Clock Rate for Column Pins (Series Termination) (Part 1 of 2)					
I/O Standard	Drive Strength	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
LVTTL	OCT_25_OHMS	400	400	350	MHz
	OCT_50_OHMS	400	400	350	MHz
LVCMOS	OCT_25_OHMS	350	350	300	MHz
	OCT_50_OHMS	350	350	300	MHz
2.5 V	OCT_25_OHMS	350	350	300	MHz
	OCT_50_OHMS	350	350	300	MHz
1.8 V	OCT_25_OHMS	700	550	450	MHz
	OCT_50_OHMS	700	550	450	MHz
1.5 V	OCT_50_OHMS	550	450	400	MHz
SSTL-2 Class I	OCT_50_OHMS	600	500	500	MHz
SSTL-2 Class II	OCT_25_OHMS	600	550	500	MHz