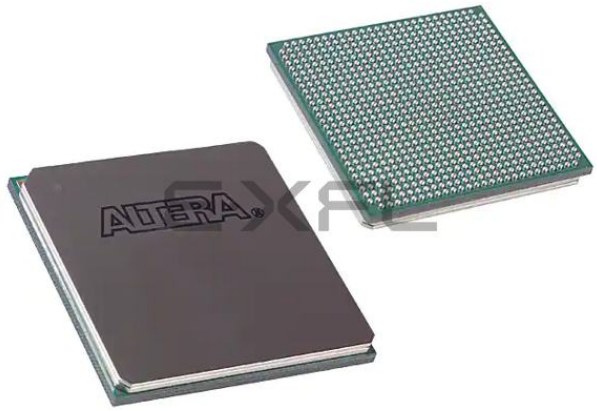

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1694
Number of Logic Elements/Cells	33880
Total RAM Bits	1369728
Number of I/O	361
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	780-BBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2sgx30df780c4

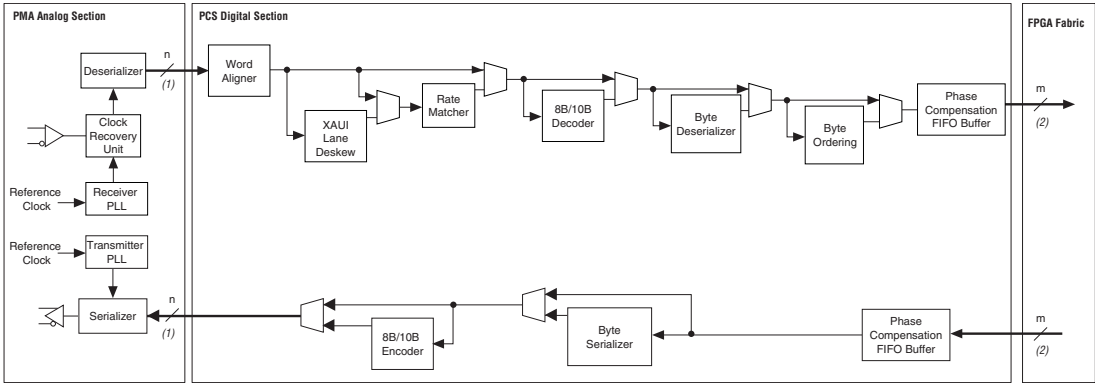
2. Stratix II GX Architecture

SIIGX51003-2.2

Transceivers

Stratix® II GX devices incorporate dedicated embedded circuitry on the right side of the device, which contains up to 20 high-speed 6.375-Gbps serial transceiver channels. Each Stratix II GX transceiver block contains four full-duplex channels and supporting logic to transmit and receive high-speed serial data streams. The transceivers deliver bidirectional point-to-point data transmissions, with up to 51 Gbps (6.375 Gbps per channel) of full-duplex data transmission per transceiver block. Figure 2–1 shows the function blocks that make up a transceiver channel within the Stratix II GX device.

Figure 2–1. Stratix II GX Transceiver Block Diagram



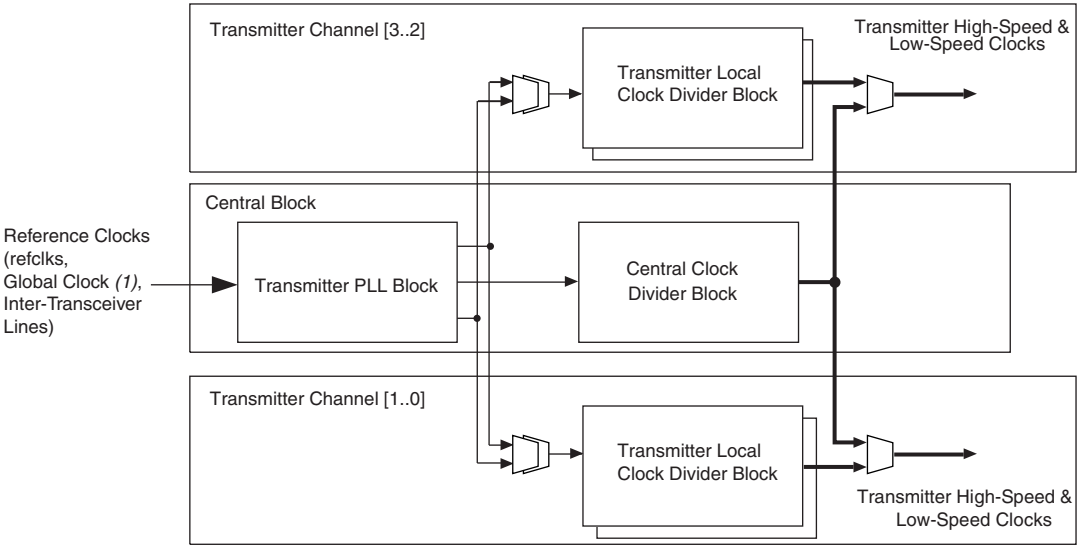
Notes to Figure 2–1:

(1) *n* represents the number of bits in each word that need to be serialized by the transmitter portion of the PMA or have been deserialized by the receiver portion of the PMA. *n* = 8, 10, 16, or 20.

(2) *m* represents the number of bits in the word that pass between the FPGA logic and the PCS portion of the transceiver. *m* = 8, 10, 16, 20, 32, or 40.

Transceivers within each block are independent and have their own set of dividers. Therefore, each transceiver can operate at different frequencies. Each block can select from two reference clocks to provide two clock domains that each transceiver can select from.

Figure 2–3. Clock Distribution for the Transmitters Note (1)



Note to Figure 2–3:
(1) The global clock line must be driven by an input pin.

The transmitter PLLs in each transceiver block clock the PMA and PCS circuitry in the transmit path. The Quartus II software automatically powers down the transmitter PLLs that are not used in the design. Figure 2–4 is a block diagram of the transmitter PLL.

The transmitter phase/frequency detector references the clock from one of the following sources:

- Reference clocks
- Reference clock from the adjacent transceiver block
- Inter-transceiver block clock lines
- Global clock line driven by input pin

Two reference clocks, `REFCLK0` and `REFCLK1`, are available per transceiver block. The inter-transceiver block bus allows multiple transceivers to use the same reference clocks. Each transceiver block has one outgoing reference clock which connects to one inter-transceiver block line. The incoming reference clock can be selected from five inter-transceiver block lines `IQ[4..0]` or from the global clock line that is driven by an input pin.

Programmable Run Length Violation

The word aligner supports a programmable run length violation counter. Whenever the number of the continuous '0' (or '1') exceeds a user programmable value, the `rx_rlv` signal goes high for a minimum pulse width of two recovered clock cycles. The maximum run values supported are shown in Table 2–7.

Table 2–7. Maximum Run Length (UI)

Mode	PMA Serialization			
	8 Bit	10 Bit	16 Bit	20 Bit
Single-Width	128	160	—	—
Double-Width	—	—	512	640

Running Disparity Check

The running disparity error `rx_disperr` and running disparity value `rx_runningdisp` are sent along with aligned data from the 8B/10B decoder to the FPGA. You can ignore or act on the reported running disparity value and running disparity error signals.

Bit-Slip Mode

The word aligner can operate in either pattern detection mode or in bit-slip mode.

The bit-slip mode provides the option to manually shift the word boundary through the FPGA. This feature is useful for:

- Longer synchronization patterns than the pattern detector can accommodate
- Scrambled data stream
- Input stream consisting of over-sampled data

This feature can be applied at 10-bit and 16-bit data widths.

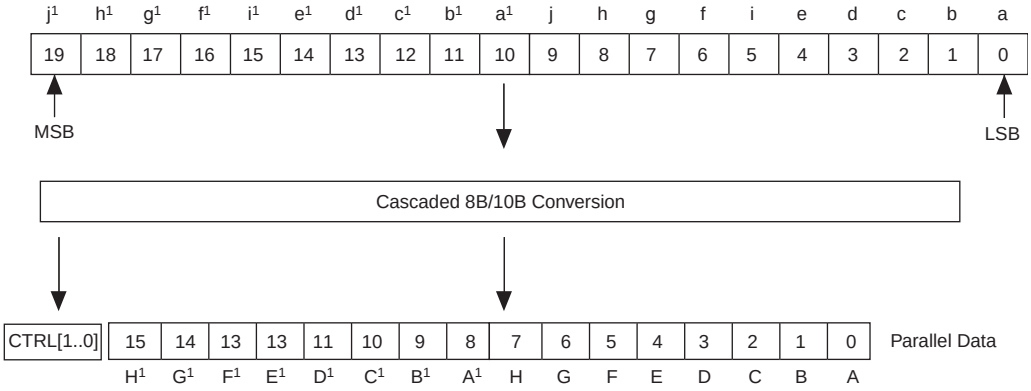
The word aligner outputs a word boundary as it is received from the analog receiver after reset. You can examine the word and search its boundary in the FPGA. To do so, assert the `rx_bitslip` signal. The `rx_bitslip` signal should be toggled and held constant for at least two FPGA clock cycles.

For every rising edge of the `rx_bitslip` signal, the current word boundary is slipped by one bit. Every time a bit is slipped, the bit received earliest is lost. If bit slipping shifts a complete round of bus width, the word boundary is back to the original boundary.

asserted. All 8B/10B control signals, such as disparity error or control detect, are pipelined with the data in the Stratix II GX receiver block and are edge aligned with the data.

Figure 2–23 shows how the 20-bit code is decoded to the 16-bit data + 2-bit control indicator.

Figure 2–23. 20-Bit to 16-Bit Decoding Process



There are two optional error status ports available in the 8B/10B decoder, `rx_errdetect` and `rx_disperr`. These status signals are aligned with the code group in which the error occurred.

Receiver State Machine

The receiver state machine operates in Basic, GIGE, PCI Express, and XAUI modes. In GIGE mode, the receiver state machine replaces invalid code groups with K30.7. In XAUI mode, the receiver state machine translates the XAUI PCS code group to the XAUI XGMII code group.

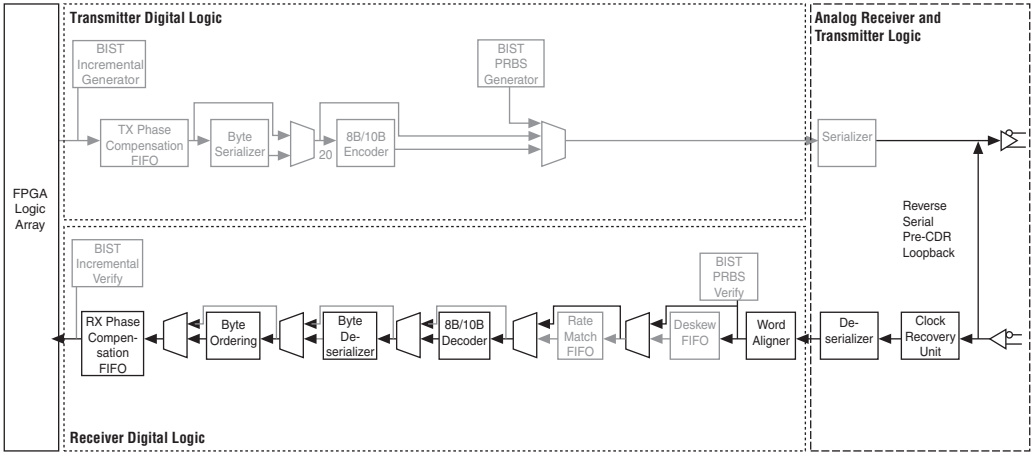
Byte Deserializer

The byte deserializer widens the transceiver data path before the FPGA interface. This reduces the rate at which the received data needs to be clocked at in the FPGA logic. The byte deserializer block is available in both single- and double-width modes.

The byte deserializer converts the one- or two-byte interface into a two- or four-byte-wide data path from the transceiver to the FPGA logic (see Table 2–9). The FPGA interface has a limit of 250 MHz, so the byte deserializer is needed to widen the bus width at the FPGA interface and

Figure 2–27 show the Stratix II GX block in reverse serial pre-CDR loopback mode.

Figure 2–27. Stratix II GX Block in Reverse Serial Pre-CDR Loopback Mode



PCI Express PIPE Reverse Parallel Loopback

This loopback mode, available only in PIPE mode, can be dynamically enabled by the `tx_detectrxloopback` port of the PIPE interface. Figure 2–28 shows the datapath for this mode.

Figure 2–28. Stratix II GX Block in PCI Express PIPE Reverse Parallel Loopback Mode

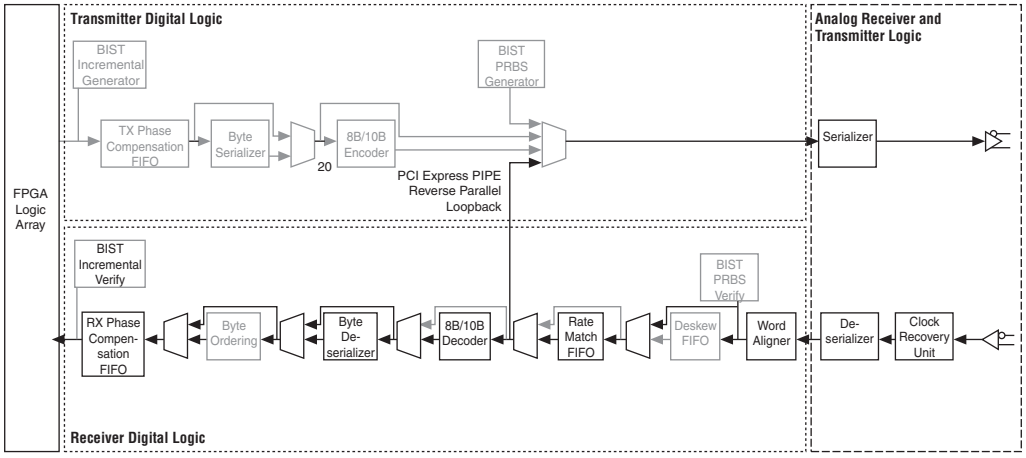


Table 2–11 summarizes the possible clocking connections for the transceivers.

Table 2–11. Available Clocking Connections for Transceivers

Source	Destination				
	Transmitter PLL	Receiver PLL	Global Clock	Regional Clock	Inter-Transceiver Lines
REFCLK[1..0]	✓	✓	✓	✓	✓
Transmitter PLL			✓	✓	
Receiver PLL			✓	✓	
Global clock (driven from an input pin)	✓	✓			
Inter-transceiver lines	✓	✓			

Clock Resource for PLD-Transceiver Interface

For the regional or global clock network to route into the transceiver, a local route input output (LRIO) channel is required. Each LRIO clock region has up to eight clock paths and each transceiver block has a maximum of eight clock paths for connecting with LRIO clocks. These resources are limited and determine the number of clocks that can be used between the PLD and transceiver blocks. Table 2–12 shows the number of LRIO resources available for Stratix II GX devices with different numbers of transceiver blocks.

Tables 2–12 through 2–15 show the connection of the LRIO clock resource to the transceiver block.

Table 2–12. Available Clocking Connections for Transceivers in 2SGX30D

Region	Clock Resource		Transceiver	
	Global Clock	Regional Clock	Bank 13 8 Clock I/O	Bank 14 8 Clock I/O
Region0 8 LRIO clock	✓	RCLK 20-27	✓	
Region1 8 LRIO clock	✓	RCLK 12-19		✓

Table 2–23. DSP Block Signal Sources and Destinations

LAB Row at Interface	Control Signals Generated	Data Inputs	Data Outputs
0	clock0 aclr0 ena0 mult01_saturate addnsub1_round/ accum_round addnsub1 signa sourcea sourceb	A1[17..0] B1[17..0]	OA[17..0] OB[17..0]
1	clock1 aclr1 ena1 accum_saturate mult01_round accum_sload sourcea sourceb mode0	A2[17..0] B2[17..0]	OC[17..0] OD[17..0]
2	clock2 aclr2 ena2 mult23_saturate addnsub3_round/ accum_round addnsub3 sign_b sourcea sourceb	A3[17..0] B3[17..0]	OE[17..0] OF[17..0]
3	clock3 aclr3 ena3 accum_saturate mult23_round accum_sload sourcea sourceb mode1	A4[17..0] B4[17..0]	OG[17..0] OH[17..0]

The Stratix II GX clock networks can be disabled (powered down) by both static and dynamic approaches. When a clock net is powered down, all the logic fed by the clock net is in an off-state, thereby reducing the overall power consumption of the device. The global and regional clock networks can be powered down statically through a setting in the configuration file (**.sof** or **.pof**). Clock networks that are not used are automatically powered down through configuration bit settings in the configuration file generated by the Quartus II software. The dynamic clock enable and disable feature allows the internal logic to control power up and down synchronously on GCLK and RCLK nets and PLL_OUT pins. This function is independent of the PLL and is applied directly on the clock network or PLL_OUT pin, as shown in Figures 2–67 through 2–69.

Enhanced and Fast PLLs

Stratix II GX devices provide robust clock management and synthesis using up to four enhanced PLLs and four fast PLLs. These PLLs increase performance and provide advanced clock interfacing and clock frequency synthesis. With features such as clock switchover, spread spectrum clocking, reconfigurable bandwidth, phase control, and reconfigurable phase shifting, the Stratix II GX device's enhanced PLLs provide you with complete control of clocks and system timing. The fast PLLs provide general purpose clocking with multiplication and phase shifting as well as high-speed outputs for high-speed differential I/O support. Enhanced and fast PLLs work together with the Stratix II GX high-speed I/O and advanced clock architecture to provide significant improvements in system performance and bandwidth.

Table 2–26 shows the enhanced PLL and fast PLL features in Stratix II GX devices.

Table 2–26. Stratix II GX PLL Features

Feature	Enhanced PLL	Fast PLL
Clock multiplication and division	*m*/(*n* × post-scale counter) *(1)*	*m*/(*n* × post-scale counter) *(2)*
Phase shift	Down to 125-ps increments *(3)*, *(4)*	Down to 125-ps increments *(3)*, *(4)*
Clock switchover	✓	✓ *(5)*
PLL reconfiguration	✓	✓
Reconfigurable bandwidth	✓	✓
Spread spectrum clocking	✓	
Programmable duty cycle	✓	✓
Number of internal clock outputs	6	4
Number of external clock outputs	Three differential/six single-ended	*(6)*
Number of feedback clock inputs	One single-ended or differential *(7)*, *(8)*	

Notes to Table 2–26:

(1) For enhanced PLLs, *m*, *n* range from 1 to 256 and post-scale counters range from 1 to 512 with 50% duty cycle.
(2) For fast PLLs, *m*, and post-scale counters range from 1 to 32. The *n* counter ranges from 1 to 4.
(3) The smallest phase shift is determined by the voltage controlled oscillator (VCO) period divided by 8.
(4) For degree increments, Stratix II GX devices can shift all output frequencies in increments of at least 45. Smaller degree increments are possible depending on the frequency and divide parameters.
(5) Stratix II GX fast PLLs only support manual clock switchover.
(6) Fast PLLs can drive to any I/O pin as an external clock. For high-speed differential I/O pins, the device uses a data channel to generate `txclkout`.
(7) If the feedback input is used, you will lose one (or two, if f_{BIN} is differential) external clock output pin.
(8) Every Stratix II GX device has at least two enhanced PLLs with one single-ended or differential external feedback input per PLL.

- Differential SSTL-2 class I and II
- 1.2-V HSTL class I and II
- 1.5-V HSTL class I and II
- 1.8-V HSTL class I and II
- SSTL-2 class I and II
- SSTL-18 class I and II

Table 2–33 describes the I/O standards supported by Stratix II GX devices.

Table 2–33. Stratix II GX Supported I/O Standards

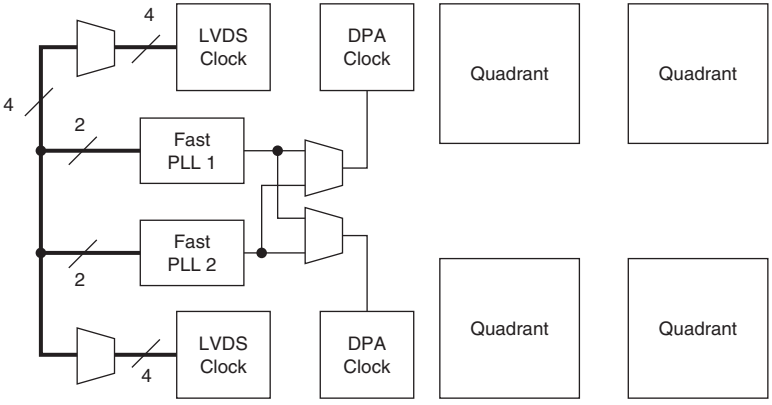
I/O Standard	Type	Input Reference Voltage (V_{REF}) (V)	Output Supply Voltage (V_{CCIO}) (V)	Board Termination Voltage (V_{TT}) (V)
LVTTL	Single-ended	—	3.3	—
LVCMOS	Single-ended	—	3.3	—
2.5 V	Single-ended	—	2.5	—
1.8 V	Single-ended	—	1.8	—
1.5-V LVCMOS	Single-ended	—	1.5	—
3.3-V PCI	Single-ended	—	3.3	—
3.3-V PCI-X mode 1	Single-ended	—	3.3	—
LVDS	Differential	—	2.5 *(3)*	—
LVPECL *(1)*	Differential	—	3.3	—
HyperTransport technology	Differential	—	2.5 *(3)*	—
Differential 1.5-V HSTL class I and II *(2)*	Differential	0.75	1.5	0.75
Differential 1.8-V HSTL class I and II *(2)*	Differential	0.90	1.8	0.90
Differential SSTL-18 class I and II *(2)*	Differential	0.90	1.8	0.90
Differential SSTL-2 class I and II *(2)*	Differential	1.25	2.5	1.25
1.2-V HSTL*(4)*	Voltage-referenced	0.6	1.2	0.6
1.5-V HSTL class I and II	Voltage-referenced	0.75	1.5	0.75
1.8-V HSTL class I and II	Voltage-referenced	0.9	1.8	0.9
SSTL-18 class I and II	Voltage-referenced	0.90	1.8	0.90

For high-speed source synchronous interfaces such as POS-PHY 4 and the Parallel RapidIO standard, the source synchronous clock rate is not a byte- or SERDES-rate multiple of the data rate. Byte alignment is necessary for these protocols because the source synchronous clock does not provide a byte or word boundary since the clock is one half the data rate, not one eighth. The Stratix II GX device's high-speed differential I/O circuitry provides dedicated data realignment circuitry for user-controlled byte boundary shifting. This simplifies designs while saving ALM resources. You can use an ALM-based state machine to signal the shift of receiver byte boundaries until a specified pattern is detected to indicate byte alignment.

Fast PLL and Channel Layout

The receiver and transmitter channels are interleaved such that each I/O bank on the left side of the device has one receiver channel and one transmitter channel per LAB row. Figure 2–90 shows the fast PLL and channel layout in the EP2SGX30C/D and EP2SGX60C/D devices. Figure 2–91 shows the fast PLL and channel layout in EP2SGX60E, EP2SGX90E/F, and EP2SGX130G devices.

Figure 2–90. Fast PLL and Channel Layout in the EP2SGX30C/D and EP2SGX60C/D Devices *Note (1)*



Note to Figure 2–90:
(1) See Table 2–38 for the number of channels each device supports.

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 14 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Sinusoidal Jitter Tolerance (peak-to-peak) *(6)*	Jitter Frequency = 22.1 KHz Data Rate = 614.4 Mbps, 1.2288 Gbps, 2.4576 Gbps REFCLK = 61.44 MHz for 614.4 Mbps REFCLK = 122.88 MHz for 1.2288 Gbps and 2.4576 Gbps Pattern = CJPAT Equalizer Setting = 6 DC Gain = 0 dB		> 8.5			> 8.5			N/A		UI
	Jitter Frequency = 1.875 MHz Data Rate = 614.4 Mbps, 1.2288 Gbps, 2.4576 Gbps REFCLK = 61.44 MHz for 614.4 Mbps REFCLK = 122.88 MHz for 1.2288 Gbps and 2.4576 Gbps Pattern = CJPAT Equalizer Setting = 6 DC Gain = 0 dB		> 0.1			> 0.1			N/A		UI

Figures 4–6 and 4–7 show receiver input and transmitter output waveforms, respectively, for all differential I/O standards (LVDS and LVPECL).

Figure 4–6. Receiver Input Waveforms for Differential I/O Standards

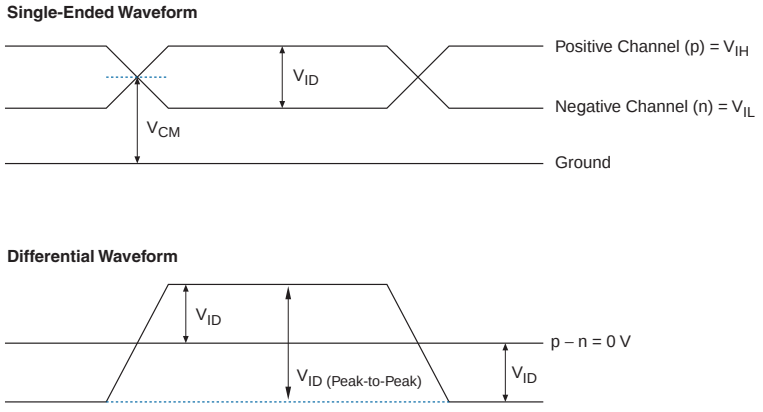
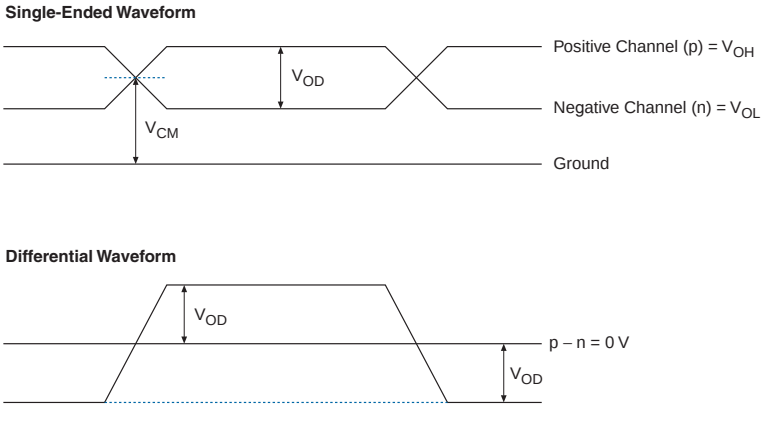


Figure 4–7. Transmitter Output Waveforms for Differential I/O Standards



Power Consumption

Altera offers two ways to calculate power for a design: the Excel-based PowerPlay early power estimator power calculator and the Quartus® II PowerPlay power analyzer feature.

The interactive Excel-based PowerPlay early power estimator is typically used prior to designing the FPGA in order to get an estimate of device power. The Quartus II PowerPlay power analyzer provides better quality estimates based on the specifics of the design after place-and-route is complete. The power analyzer can apply a combination of user-entered, simulation-derived and estimated signal activities which, combined with detailed circuit models, can yield very accurate power estimates.

In both cases, these calculations should only be used as an estimation of power, not as a specification.

For more information on PowerPlay tools, refer to the *PowerPlay Early Power Estimators (EPE) and Power Analyzer,* the *Quartus II PowerPlay Analysis and Optimization Technology*, and the *PowerPlay Power Analyzer* chapter in volume 3 of the *Quartus II Handbook*. The PowerPlay early power estimators are available on the Altera web site at **www.altera. com**.

See Table 4–23 on page 42 for typical I_{CC} standby specifications.

Timing Model

The DirectDrive technology and MultiTrack interconnect ensure predictable performance, accurate simulation, and accurate timing analysis across all Stratix II GX device densities and speed grades. This section describes and specifies the performance, internal, external, and PLL timing specifications.

All specifications are representative of worst-case supply voltage and junction temperature conditions.

Preliminary and Final Timing

Timing models can have either preliminary or final status. The Quartus II software issues an informational message during the design compilation if the timing models are preliminary. Table 4–52 shows the status of the Stratix II GX device timing models.

Preliminary status means the timing model is subject to change. Initially, timing numbers are created using simulation results, process data, and other known parameters. These tests are used to make the preliminary numbers as close to the actual timing parameters as possible.

Table 4–57. IOE Internal Timing Microparameters (Part 2 of 2)

Symbol	Parameter	-3 Speed Grade (1)		-3 Speed Grade (2)		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{PIN2COMBOUT\_R}$	Row input pin to IOE combinational output	410	760	410	798	410	848	410	1018	ps
$t_{PIN2COMBOUT\_C}$	Column input pin to IOE combinational output	428	787	428	825	428	878	428	1054	ps
$t_{COMBIN2PIN\_R}$	Row IOE data input to combinational output pin	1101	2026	1101	2127	1101	2261	1101	2439	ps
$t_{COMBIN2PIN\_C}$	Column IOE data input to combinational output pin	991	1854	991	1946	991	2069	991	2246	ps
t_{CLR}	Minimum clear pulse width	200		210		223		268		ps
t_{PRE}	Minimum preset pulse width	200		210		223		268		ps
t_{CLKL}	Minimum clock low time	600		630		669		804		ps
t_{CLKH}	Minimum clock high time	600		630		669		804		ps

(1) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
(2) This column refers to –3 speed grades for EP2SGX130 devices.

Table 4–58. DSP Block Internal Timing Microparameters (Part 1 of 2)

Symbol	Parameter	-3 Speed Grade (1)		-3 Speed Grade (2)		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{SU}	Input, pipeline, and output register setup time before clock	50		52		55		67		ps
t_{H}	Input, pipeline, and output register hold time after clock	180		189		200		241		ps
t_{CO}	Input, pipeline, and output register clock-to-output delay	0	0	0	0	0	0	0	0	ps

Table 4–61. M-RAM Block Internal Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	-3 Speed Grade *(2)*		-3 Speed Grade *(3)*		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{MEGABESU}$	Byte enable setup time before clock	-9		-10		-11		-13		ps
$t_{MEGABEH}$	Byte enable hold time after clock	39		40		43		52		ps
$t_{MEGADATAASU}$	A port data setup time before clock	50		52		55		67		ps
$t_{MEGADATAAH}$	A port data hold time after clock	243		255		271		325		ps
$t_{MEGAADDRASU}$	A port address setup time before clock	589		618		657		789		ps
$t_{MEGAADDRAH}$	A port address hold time after clock	-347		-365		-388		-465		ps
$t_{MEGADATABSU}$	B port setup time before clock	50		52		55		67		ps
$t_{MEGADATABH}$	B port hold time after clock	243		255		271		325		ps
$t_{MEGAADDRBSU}$	B port address setup time before clock	589		618		657		789		ps
$t_{MEGAADDRBH}$	B port address hold time after clock	-347		-365		-388		-465		ps
$t_{MEGADATACO1}$	Clock-to-output delay when using output registers	480	715	480	749	480	797	480	957	ps
$t_{MEGADATACO2}$	Clock-to-output delay without output registers	1950	2899	1950	3042	1950	3235	1950	3884	ps
$t_{MEGACLKL}$	Minimum clock low time	1250		1312		1395		1675		ps
$t_{MEGACLKH}$	Minimum clock high time	1250		1312		1395		1675		ps
$t_{MEGACLR}$	Minimum clear pulse width	144		151		160		192		ps

(1) The M512 block f_{MAX} obtained using the Quartus II software does not necessarily equal to 1/TMEGARC.
(2) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
(3) This column refers to –3 speed grades for EP2SGX130 devices.

Table 4–79. Clock Network Specifications (Part 2 of 2)					
Name	**Description**	**Min**	**Typ**	**Max**	**Unit**
Clock skew adder EP2SGX130 *(1)*	Inter-clock network, same side			±63	ps
	Inter-clock network, entire chip			±125	ps

(1) This is in addition to intra-clock network skew, which is modeled in the Quartus II software.

IOE Programmable Delay

See Tables 4–80 and 4–81 for IOE programmable delay.

Table 4–80. Stratix II GX IOE Programmable Delay on Column Pins *Note (1)*													
Parameter	**Paths Affected**	**Available Settings**	**Minimum Timing**		**-3 Speed Grade** *(2)*		**-3 Speed Grade** *(3)*		**-4 Speed Grade**		**-5 Speed Grade**		**Unit**
			Min Offset	**Max Offset**	**Min Offset**	**Max Offset**	**Min Offset**	**Max Offset**	**Min Offset**	**Max Offset**	**Min Offset**	**Max Offset**	
Input delay from pin to internal cells	Pad to I/O dataout to core	8	0	1781	0	2881	0	3025	0	3217	0	3,860	ps
Input delay from pin to input register	Pad to I/O input register	64	0	2053	0	3275	0	3439	0	3657	0	4388	ps
Delay from output register to output pin	I/O output register to pad	2	0	332	0	500	0	525	0	559	0	670	ps
Output enable pin delay	t_{XZ}, t_{ZX}	2	0	320	0	483	0	507	0	539	0	647	ps

(1) The incremental values for the settings are generally linear. For the exact delay associated with each setting, use the latest version of the Quartus II software.
(2) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
(3) This column refers to –3 speed grades for EP2SGX130 devices.

To calculate the output toggle rate for a non 0 pF load, use this formula:

The toggle rate for a non 0 pF load

= 1,000 / (1,000/ toggle rate at 0 pF load + derating factor × load value in pF /1,000)

For example, the output toggle rate at 0 pF load for SSTL-18 Class II 20 mA I/O standard is 550 MHz on a -3 device clock output pin. The derating factor is 94 ps/pF. For a 10 pF load the toggle rate is calculated as:

1,000 / (1,000/550 + 94 × 10 /1,000) = 363 (MHz)

Table 4–88 shows the maximum input clock toggle rates for Stratix II GX device column pins.

Table 4–88. Stratix II GX Maximum Input Clock Rate for Column I/O Pins (Part 1 of 2)

I/O Standard	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
LVTTL	500	500	450	MHz
2.5 V	500	500	450	MHz
1.8 V	500	500	450	MHz
1.5 V	500	500	450	MHz
LVCMOS	500	500	450	MHz
SSTL-2 Class I	500	500	500	MHz
SSTL-2 Class II	500	500	500	MHz
SSTL-18 Class I	500	500	500	MHz
SSTL-18 Class I I	500	500	500	MHz
1.5-V HSTL Class I	500	500	500	MHz
1.5-V HSTL Class I I	500	500	500	MHz
1.8-V HSTL Class I	500	500	500	MHz
1.8-V HSTL Class II	500	500	500	MHz
PCI	500	500	450	MHz
PCI-X	500	500	450	MHz
Differential SSTL-2 Class I	500	500	500	MHz
Differential SSTL-2 Class II	500	500	500	MHz
Differential SSTL-18 Class I	500	500	500	MHz

PLL Timing Specifications

Tables 4–110 and 4–111 describe the Stratix II GX PLL specifications when operating in both the commercial junction temperature range (0 to 85 C) and the industrial junction temperature range (–40 to 100 C), except for the clock switchover and phase-shift stepping features. These two features are only supported from the 0 to 100 C junction temperature range.

Table 4–110. Enhanced PLL Specifications (Part 1 of 2)

Name	Description	Min	Typ	Max	Unit
f_{IN}	Input clock frequency	4		500	MHz
f_{INPFD}	Input frequency to the PFD	4		420	MHz
f_{INDUTY}	Input clock duty cycle	40		60	%
f_{ENDUTY}	External feedback input clock duty cycle	40		60	%
$t_{INJITTER}$	Input or external feedback clock input jitter tolerance in terms of period jitter. Bandwidth ≤0.85 MHz		0.5		ns (peak-to-peak)
	Input or external feedback clock input jitter tolerance in terms of period jitter. Bandwidth > 0.85 MHz		1.0		ns (peak-to-peak)
$t_{OUTJITTER}$	Dedicated clock output period jitter			250 ps for ≥ 100 MHz outclk 25 mUI for < 100 MHz outclk	ps or mUI (p-p)
t_{FCOMP}	External feedback compensation time			10	ns
f_{OUT}	Output frequency for internal global or regional clock	1.5 *(2)*		550	MHz
$f_{OUTDUTY}$	Duty cycle for external clock output	45	50	55	%
$f_{SCANCLK}$	Scanclk frequency			100	MHz
$t_{CONFIGEPLL}$	Time required to reconfigure scan chains for EPLLs		$174/f_{SCANCLK}$		ns
f_{OUT_EXT}	PLL external clock output frequency	1.5 *(2)*		*(1)*	MHz
t_{LOCK}	Time required for the PLL to lock from the time it is enabled or the end of device configuration		0.03	1	ms
t_{DLOCK}	Time required for the PLL to lock dynamically after automatic clock switchover between two identical clock frequencies			1	ms
$f_{SWITCHOVER}$	Frequency range where the clock switchover performs properly	1.5	1	500	MHz
f_{CLBW}	PLL closed-loop bandwidth	0.13	1.2	16.9	MHz

Table 4–111. Fast PLL Specifications (Part 2 of 2)					
Name	**Description**	**Min**	**Typ**	**Max**	**Unit**
f_{VCO}	Upper VCO frequency range for –3 and –4 speed grades	300		1,040	MHz
	Upper VCO frequency range for –5 speed grades	300		840	MHz
	Lower VCO frequency range for –3 and –4 speed grades	150		520	MHz
	Lower VCO frequency range for –5 speed grades	150		420	MHz
f_{OUT}	PLL output frequency to GCLK or RCLK	4.6875		550	MHz
	PLL output frequency to LVDS or DPA clock	150		1,040	MHz
f_{OUT_EXT}	PLL clock output frequency to regular I/O	4.6875		*(1)*	MHz
$t_{CONFIGPLL}$	Time required to reconfigure scan chains for fast PLLs		$75/f_{SCANCLK}$		ns
f_{CLBW}	PLL closed-loop bandwidth	1.16	5	28	MHz
t_{LOCK}	Time required for the PLL to lock from the time it is enabled or the end of the device configuration		0.03	1	ms
t_{PLL_PSERR}	Accuracy of PLL phase shift			±30	ps
t_{ARESET}	Minimum pulse width on areset signal.	10			ns
$t_{ARESET\_RECONFIG}$	Minimum pulse width on the areset signal when using PLL reconfiguration. Reset the PLL after scandone goes high.	500			ns

(1) This is limited by the I/O f_{MAX}. See Tables 4–91 through 4–95 for the maximum.

External Memory Interface Specifications

Tables 4–112 through 4–116 contain Stratix II GX device specifications for the dedicated circuitry used for interfacing with external memory devices.

Table 4–112. DLL Frequency Range Specifications (Part 1 of 2)		
Frequency Mode	**Frequency Range (MHz)**	**Resolution (Degrees)**
0	100 to 175	30
1	150 to 230	22.5
2	200 to 350 (–3 speed grade)	30
	200 to 310 (–4 and –5 speed grade)	30