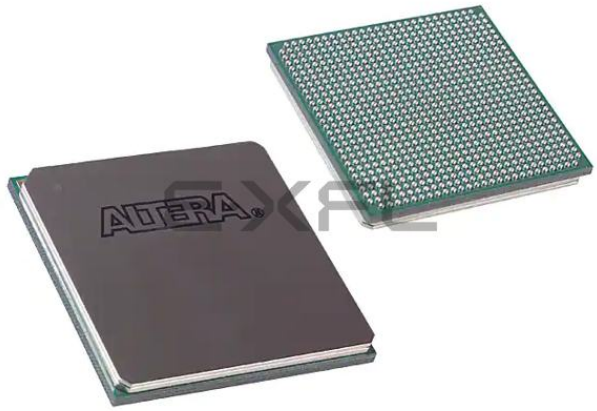

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

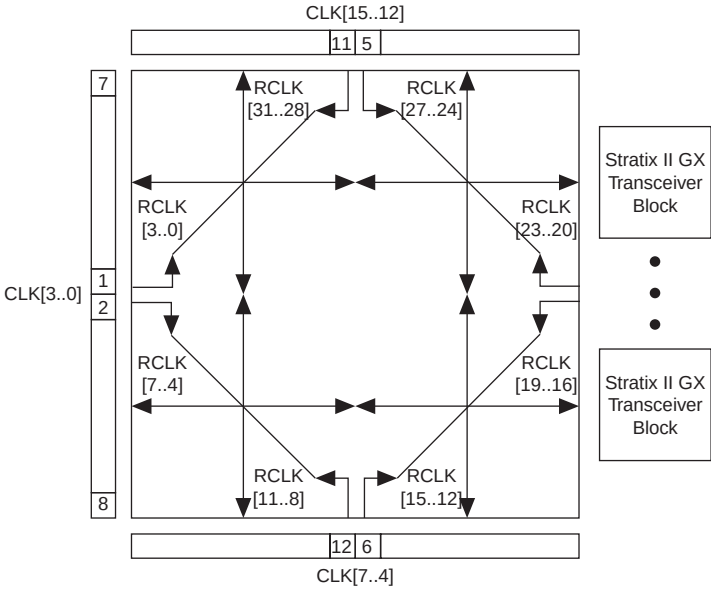
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1694
Number of Logic Elements/Cells	33880
Total RAM Bits	1369728
Number of I/O	361
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	780-BBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2sgx30df780i4

Figure 2–31. Stratix II GX Receiver PLL Recovered Clock to Regional Clock Connection *Notes (1), (2)*



Notes to Figure 2–31:

(1) CLK# pins are clock pins and their associated number. These are pins for global and local clocks.

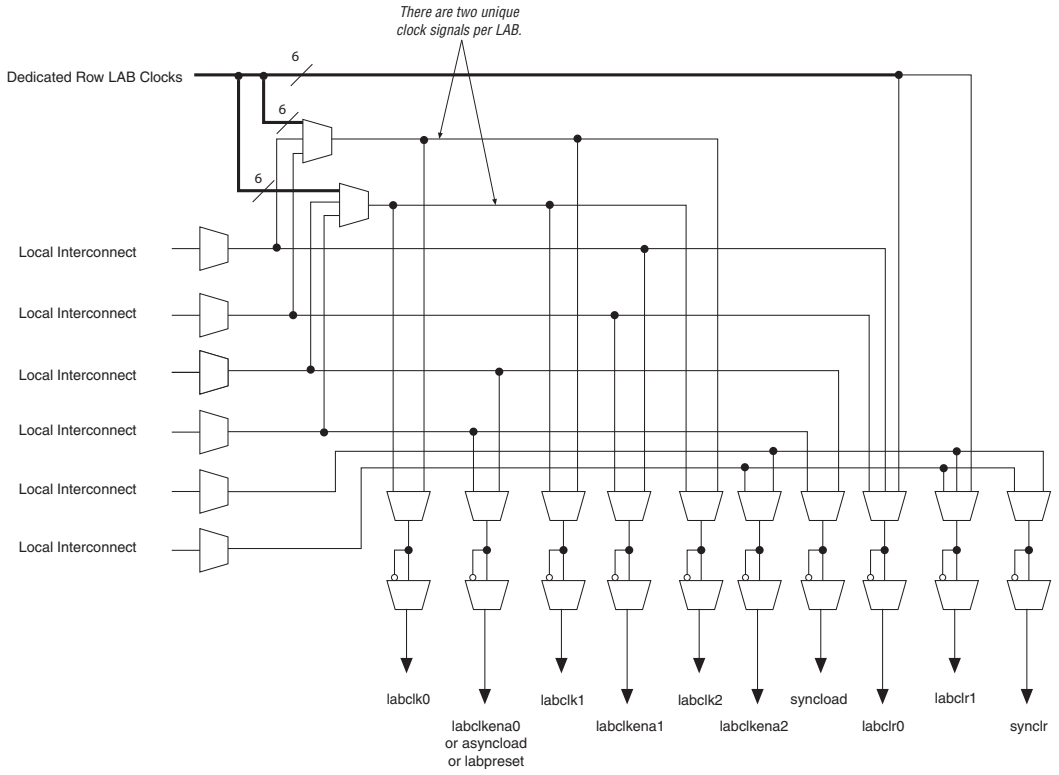
(2) RCLK# pins are regional clock pins.

load acts as a preset when the asynchronous load data input is tied high. When the asynchronous load/preset signal is used, the `labclkena0` signal is no longer available.

The LAB row clocks `[5..0]` and LAB local interconnect generate the LAB-wide control signals. The MultiTrack™ interconnects have inherently low skew. This low skew allows the MultiTrack interconnects to distribute clock and control signals in addition to data.

Figure 2–34 shows the LAB control signal generation circuit.

Figure 2–34. LAB-Wide Control Signals



R24 row interconnects span 24 LABs and provide the fastest resource for long row connections between LABs, TriMatrix memory, DSP blocks, and Row IOEs. The R24 row interconnects can cross M-RAM blocks. R24 row interconnects drive to other row or column interconnects at every fourth LAB and do not drive directly to LAB local interconnects. R24 row interconnects drive LAB local interconnects via R4 and C4 interconnects. R24 interconnects can drive R24, R4, C16, and C4 interconnects. The column interconnect operates similarly to the row interconnect and vertically routes signals to and from LABs, TriMatrix memory, DSP blocks, and IOEs. Each column of LABs is served by a dedicated column interconnect.

These column resources include:

- Shared arithmetic chain interconnects in a LAB
- Carry chain interconnects in a LAB and from LAB to LAB
- Register chain interconnects in a LAB
- C4 interconnects traversing a distance of four blocks in an up and down direction
- C16 column interconnects for high-speed vertical routing through the device

Stratix II GX devices include an enhanced interconnect structure in LABs for routing shared arithmetic chains and carry chains for efficient arithmetic functions. The register chain connection allows the register output of one ALM to connect directly to the register input of the next ALM in the LAB for fast shift registers. These ALM-to-ALM connections bypass the local interconnect. The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. Figure 2–47 shows the shared arithmetic chain, carry chain, and register chain interconnects.

Digital Signal Processing (DSP) Block

The most commonly used DSP functions are finite impulse response (FIR) filters, complex FIR filters, infinite impulse response (IIR) filters, fast Fourier transform (FFT) functions, direct cosine transform (DCT) functions, and correlators. All of these use the multiplier as the fundamental building block. Additionally, some applications need specialized operations such as multiply-add and multiply-accumulate operations. Stratix II GX devices provide DSP blocks to meet the arithmetic requirements of these functions.

Each Stratix II GX device has two to four columns of DSP blocks to efficiently implement DSP functions faster than ALM-based implementations. Stratix II GX devices have up to 24 DSP blocks per column (see Table 2–21). Each DSP block can be configured to support up to:

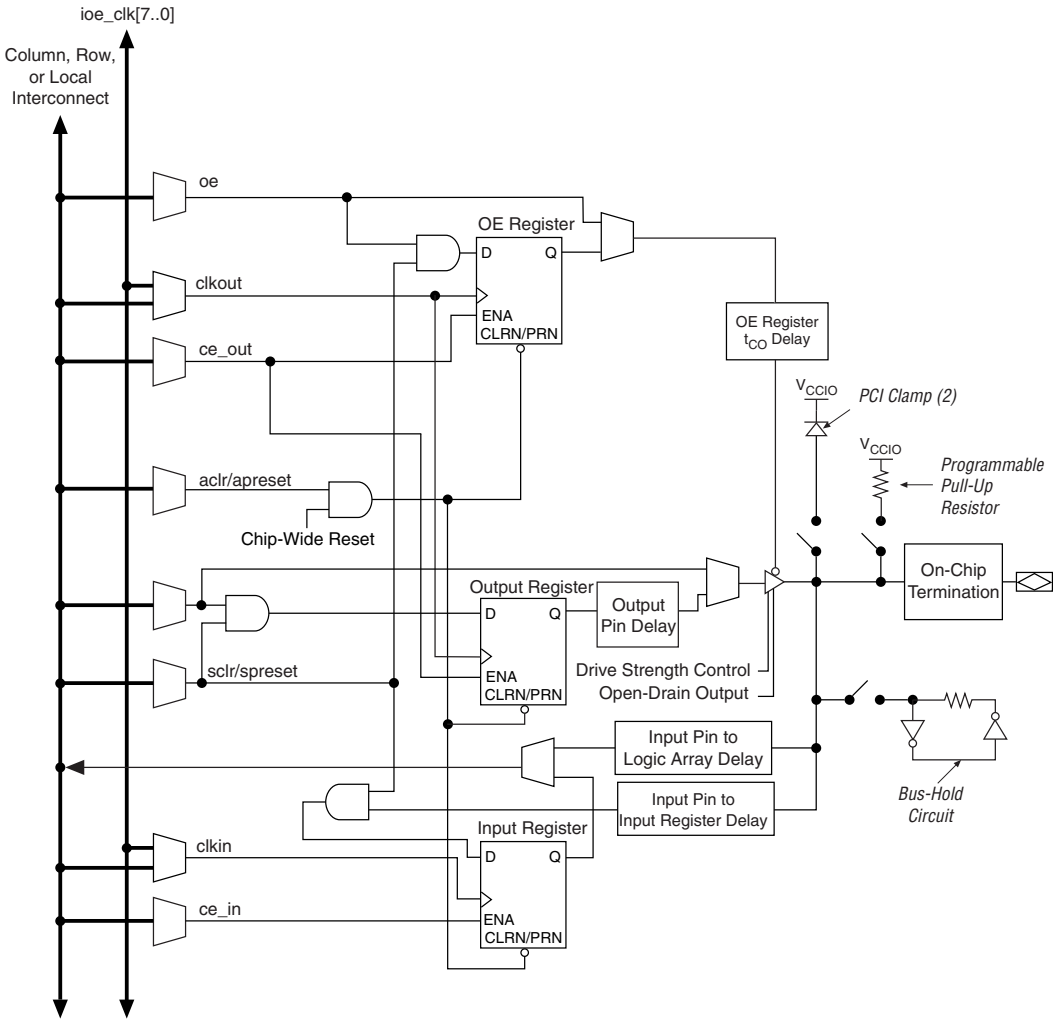
- Eight 9 × 9-bit multipliers
- Four 18 × 18-bit multipliers
- One 36 × 36-bit multiplier

As indicated, the Stratix II GX DSP block can support one 36 × 36-bit multiplier in a single DSP block, and is true for any combination of signed, unsigned, or mixed sign multiplications.

Table 2–29. Global and Regional Clock Connections from Bottom Clock Pins and Enhanced PLL Outputs (Part 2 of 2)

Bottom Side Global and Regional Clock Network Connectivity	DLLCLK	CLK4	CLK5	CLK6	CLK7	RCLK8	RCLK9	RCLK10	RCLK11	RCLK12	RCLK13	RCLK14	RCLK15
GCLKDRV2				✓									
GCLKDRV3					✓								
RCLKDRV0						✓				✓			
RCLKDRV1							✓				✓		
RCLKDRV2								✓				✓	
RCLKDRV3									✓				✓
RCLKDRV4						✓				✓			
RCLKDRV5							✓				✓		
RCLKDRV6								✓				✓	
RCLKDRV7									✓				✓
Enhanced PLL 6 outputs													
c0	✓	✓	✓			✓				✓			
c1	✓	✓	✓				✓				✓		
c2	✓			✓	✓			✓				✓	
c3	✓			✓	✓				✓				✓
c4	✓					✓		✓		✓		✓	
c5	✓						✓		✓		✓		✓
Enhanced PLL 12 outputs													
c0		✓	✓			✓				✓			
c1		✓	✓				✓				✓		
c2				✓	✓			✓				✓	
c3				✓	✓				✓				✓
c4						✓		✓		✓		✓	
c5							✓		✓		✓		✓

Figure 2–81. Stratix II GX IOE in Bidirectional I/O Configuration *Note (1)*



Notes to Figure 2–81:
(1) All input signals to the IOE can be inverted at the IOE.
(2) The optional PCI clamp is only available on column I/O pins.

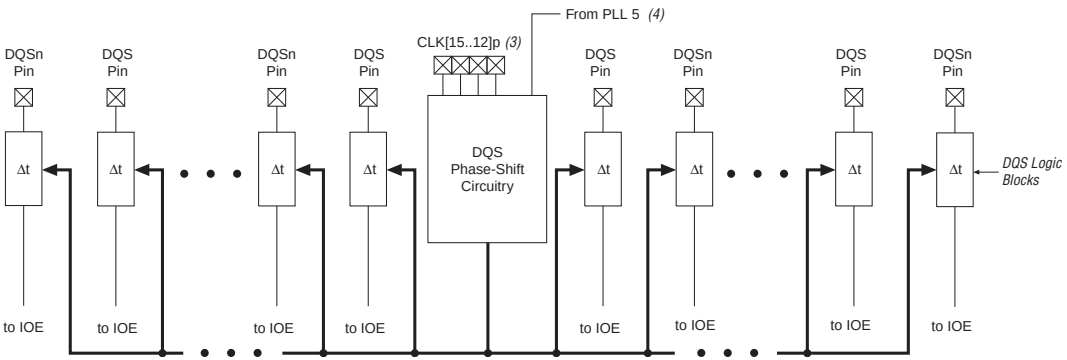
The Stratix II GX device IOE includes programmable delays that can be activated to ensure input IOE register-to-logic array register transfers, input pin-to-logic array register transfers, or output IOE register-to-pin transfers.

A compensated delay element on each DQS pin automatically aligns input DQS synchronization signals with the data window of their corresponding DQ data signals. The DQS signals drive a local DQS bus in the top and bottom I/O banks. This DQS bus is an additional resource to the I/O clocks and is used to clock DQ input registers with the DQS signal.

The Stratix II GX device has two phase-shifting reference circuits, one on the top and one on the bottom of the device. The circuit on the top controls the compensated delay elements for all DQS pins on the top. The circuit on the bottom controls the compensated delay elements for all DQS pins on the bottom.

Each phase-shifting reference circuit is driven by a system reference clock, which must have the same frequency as the DQS signal. Clock pins `CLK[15..12]p` feed the phase circuitry on the top of the device and clock pins `CLK[7..4]p` feed the phase circuitry on the bottom of the device. In addition, PLL clock outputs can also feed the phase-shifting reference circuits. Figure 2–86 shows the phase-shift reference circuit control of each DQS delay shift on the top of the device. This same circuit is duplicated on the bottom of the device.

Figure 2–86. DQS Phase-Shift Circuitry *Notes (1), (2)*



Notes to Figure 2–86:

(1) There are up to 18 pairs of DQS and DQSn pins available on the top or the bottom of the Stratix II GX device. There are up to 10 pairs on the right side and 8 pairs on the left side of the DQS phase-shift circuitry.

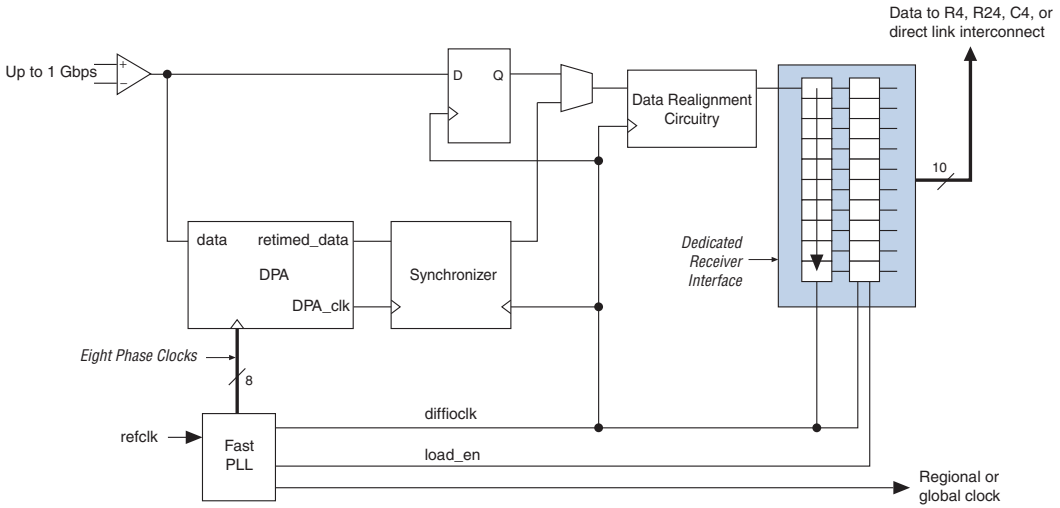
(2) The "t" module represents the DQS logic block.

(3) Clock pins `CLK[15..12]p` feed the phase-shift circuitry on the top of the device and clock pins `CLK[7..4]p` feed the phase circuitry on the bottom of the device. You can also use a PLL clock output as a reference clock to the phaseshift circuitry.

(4) You can only use PLL 5 to feed the DQS phase-shift circuitry on the top of the device and PLL 6 to feed the DQS phase-shift circuitry on the bottom of the device.

Figure 2–89 shows the block diagram of the Stratix II GX receiver channel.

Figure 2–89. Stratix II GX Receiver Channel



An external pin or global or regional clock can drive the fast PLLs, which can output up to three clocks: two multiplied high-speed clocks to drive the SERDES block and/or external pin, and a low-speed clock to drive the logic array. In addition, eight phase-shifted clocks from the VCO can feed to the DPA circuitry.

For more information on the fast PLL, see the *PLLs in Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Handbook*.

The eight phase-shifted clocks from the fast PLL feed to the DPA block. The DPA block selects the closest phase to the center of the serial data eye to sample the incoming data. This allows the source-synchronous circuitry to capture incoming data correctly regardless of the channel-to-channel or clock-to-channel skew. The DPA block locks to a phase closest to the serial data phase. The phase-aligned DPA clock is used to write the data into the synchronizer.

The synchronizer sits between the DPA block and the data realignment and SERDES circuitry. Since every channel utilizing the DPA block can have a different phase selected to sample the data, the synchronizer is needed to synchronize the data to the high-speed clock domain of the data realignment and the SERDES circuitry.

Table 3–5 shows the specifications for bias voltage and current of the Stratix II GX temperature sensing diode.

Table 3–5. Temperature-Sensing Diode Electrical Characteristics

Parameter	Minimum	Typical	Maximum	Unit
IBIAS high	80	100	120	µA
IBIAS low	8	10	12	µA
VBP - VBN	0.3		0.9	V
VBN		0.7		V
Series resistance			3	Ω

The temperature-sensing diode works for the entire operating range shown in Figure 3–2.

Figure 3–2. Temperature Versus Temperature-Sensing Diode Voltage

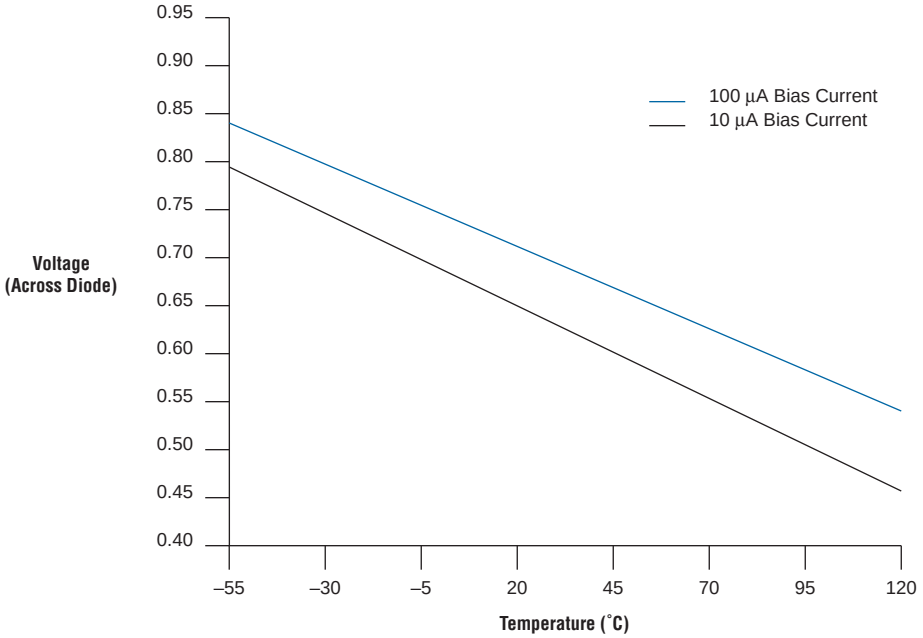


Table 4–6. Stratix II GX Transceiver Block AC Specification (Part 6 of 6)

Symbol / Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Bandwidth at 6.375 Gbps	BW = Low	-	2	-	-	-	-	-	-	-	MHz
	BW = Med	-	3	-	-	-	-	-	-	-	MHz
	BW = High	-	7	-	-	-	-	-	-	-	MHz
Bandwidth at 3.125 Gbps	BW = Low	-	3	-	-	3	-	-	3	-	MHz
	BW = Med	-	5	-	-	5	-	-	5	-	MHz
	BW = High	-	9	-	-	9	-	-	9	-	MHz
Bandwidth at 2.5 Gbps	BW = Low	-	1	-	-	1	-	-	1	-	MHz
	BW = Med	-	2	-	-	2	--	-	2	-	MHz
	BW = High	-	4	-	-	4	-	-	4	-	MHz
TX PLL lock time from `gxb_powerdown` deassertion *(9)*, *(10)*		-	-	100	-	-	100	-	-	100	us
PLD-Transceiver Interface											
Interface speed		25	-	250	25	-	250	25	-	200	MHz
Digital Reset Pulse Width		Minimum is 2 parallel clock cycles									

Notes to Table 4–6:

(1) The device cannot tolerate prolonged operation at this absolute maximum. Refer to Figure 4–5 for more information.
(2) The rate matcher supports only up to +/-300 ppm.
(3) This parameter is measured by embedding the run length data in a PRBS sequence.
(4) This feature is only available in PCI-Express (PIPE) mode.
(5) Time taken to `rx_pll_locked` goes high from `rx_analogreset` deassertion. Refer to Figure 4–1.
(6) This is how long GXB needs to stay in LTR mode after `rx_pll_locked` is asserted and before `rx_locktodata` is asserted in manual mode. Refer to Figure 4–1.
(7) Time taken to recover valid data from GXB after `rx_locktodata` signal is asserted in manual mode. Measurement results are based on PRBS31, for native data rates only. Refer to Figure 4–1.
(8) Time taken to recover valid data from GXB after `rx_freqlocked` signal goes high in automatic mode. Measurement results are based on PRBS31, for native data rates only. Refer to Figure 4–1.
(9) Please refer to the Protocol Characterization documents for lock times specific to the protocols.
(10) Time taken to lock TX PLL from `gxb_powerdown` deassertion.
(11) The 1.2 V RX V_{ICM} setting is intended for DC-coupled LVDS links.
(12) For AC-coupled links, the on-chip biasing circuit is switched off before and during configuration. Make sure that input specifications are not violated during this period.

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 13 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
CPRI Receiver Jitter Tolerance *(15)*											
Deterministic Jitter Tolerance (peak-to-peak)	Data Rate = 614.4 Mbps, 1.2288 Gbps, 2.4576 Gbps REFCLK = 61.44 MHz for 614.4 Mbps REFCLK = 122.88 MHz for 1.2288 Gbps and 2.4576 Gbps Pattern = CJPAT Equalizer Setting = 6 DC Gain = 0 dB		> 0.4			> 0.4			N/A		UI
Combined Deterministic and Random Jitter Tolerance (peak-to-peak)	Data Rate = 614.4 Mbps, 1.2288 Gbps, 2.4576 Gbps REFCLK = 61.44 MHz for 614.4 Mbps REFCLK = 122.88 MHz for 1.2288 Gbps and 2.4576 Gbps Pattern = CJPAT Equalizer Setting = 6 DC Gain = 0 dB		> 0.66			> 0.66			N/A		UI

Table 4–31. PCML Specifications *Note (1)*

Symbol	Parameter	References
Reference Clock		
3.3-V PCML 1.5-V PCML 1.2-V PCML	Reference clock supported PCML standards	
V_{ID}	Peak-to-peak differential input voltage	The specifications are located in the Reference Clock section of Table 4–6 on page 4–4. The specifications listed in Table 4–6 are applicable to PCML input standards.
V_{ICM}	Input common mode voltage	
R	On-chip termination resistors	
Receiver		
3.3-V PCML 1.5-V PCML 1.2-V PCML	Receiver supported PCML standards	
V_{ID}	Peak-to-peak differential input voltage	The specifications are located in the Receiver section of Table 4–6 on page 4–4. The specifications listed in Table 4–6 are applicable to PCML input standards.
V_{ICM}	Input common mode voltage	
R	On-chip termination resistors	
Transmitter		
1.5-V PCML 1.2-V PCML	Transmitter supported PCML standards	
V_{CCH}	Output buffer supply voltage	The specifications are located in Table 4–5 on page 4–4.
V_{OD}	Peak-to-peak differential output voltage	The specifications are located in Tables 4–7, 4–8, 4–9, 4–10, 4–11, and 4–12. The specifications listed in these tables are applicable to PCML output standards.
V_{OCM}	Output common mode voltage	The specifications are located in the Transmitter section of Table 4–6 on page 4–4. The specifications listed in Table 4–6 are applicable to PCML output standards.
R	On-chip termination resistors	

Note to Table 4–31:

(1) Stratix II GX devices support PCML input and output on GXB banks 13, 14, 15, 16, and 17. This table references Stratix II GX PCML specifications that are located in other sections of the *Stratix II GX Device Handbook*.

Table 4–46. 1.8-V HSTL Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.71	1.80	1.89	V
V_{REF}	Input reference voltage		0.85	0.90	0.95	V
V_{TT}	Termination voltage		0.85	0.90	0.95	V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 16 mA *(1)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OH} = –16 mA *(1)*			0.4	V

Note to Table 4–46:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Table 4–47. 1.8-V HSTL Class I and II Differential Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage		1.71	1.80	1.89	V
V_{DIF} (DC)	DC input differential voltage		0.2			V
V_{CM} (DC)	DC common mode input voltage		0.78		1.12	V
V_{DIF} (AC)	AC differential input voltage		0.4			V
V_{OX} (AC)	AC differential cross point voltage		0.68		0.9	V

Bus Hold Specifications

Table 4–48 shows the Stratix II GX device family bus hold specifications.

Table 4–48. Bus Hold Parameters

Parameter	Conditions	V_{CCIO} Level										Unit
		1.2 V		1.5 V		1.8 V		2.5 V		3.3 V		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	$V_{IN} > V_{IL}$ (maximum)	22.5		25		30		50		70		µA
High sustaining current	$V_{IN} < V_{IH}$ (minimum)	–22.5		–25		–30		–50		–70		µA
Low overdrive current	$0 V < V_{IN} < V_{CCIO}$		120		160		200		300		500	µA
High overdrive current	$0 V < V_{IN} < V_{CCIO}$		–120		–160		–200		–300		–500	µA
Bus-hold trip point		0.45	0.95	0.5	1.0	0.68	1.07	0.7	1.7	0.8	2.0	V

On-Chip Termination Specifications

Tables 4–49 and 4–50 define the specification for internal termination resistance tolerance when using series or differential on-chip termination.

Table 4–49. On-Chip Termination Specification for Top and Bottom I/O Banks (Part 1 of 2) *Notes (1), (2)*

Symbol	Description	Conditions	Resistance Tolerance		
			Commercial Max	Industrial Max	Unit
25-Ω R_S 3.3/2.5	Internal series termination with calibration (25-Ω setting)	V_{CCIO} = 3.3/2.5 V	±5	±10	%
	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 3.3/2.5 V	±30	±30	%
50-Ω R_S 3.3/2.5	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 3.3/2.5 V	±5	±10	%
	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 3.3/2.5 V	±30	± 30	%

Table 4–53. Output Timing Measurement Methodology for Output Pins (Part 2 of 2) Notes (1), (2), (3)

I/O Standard	Loading and Termination						Measurement Point
	R_S (Ω)	R_D (Ω)	R_T (Ω)	V_{CCIO} (V)	V_{TT} (V)	C_L (pF)	V_{MEAS} (V)
PCI (5)				2.970		10	1.485
PCI-X (5)				2.970		10	1.485
SSTL-2 Class I	25		50	2.325	1.123	0	1.1625
SSTL-2 Class II	25		25	2.325	1.123	0	1.1625
SSTL-18 Class I	25		50	1.660	0.790	0	0.83
SSTL-18 Class II	25		25	1.660	0.790	0	0.83
1.8-V HSTL Class I			50	1.660	0.790	0	0.83
1.8-V HSTL Class II			25	1.660	0.790	0	0.83
1.5-V HSTL Class I			50	1.375	0.648	0	0.6875
1.5-V HSTL Class II			25	1.375	0.648	0	0.6875
1.2-V HSTL with OCT				1.140		0	0.570
Differential SSTL-2 Class I	25		50	2.325	1.123	0	1.1625
Differential SSTL-2 Class II	25		25	2.325	1.123	0	1.1625
Differential SSTL-18 Class I	50		50	1.660	0.790	0	0.83
Differential SSTL-18 Class II	25		25	1.660	0.790	0	0.83
1.5-V differential HSTL Class I			50	1.375	0.648	0	0.6875
1.5-V differential HSTL Class II			25	1.375	0.648	0	0.6875
1.8-V differential HSTL Class I			50	1.660	0.790	0	0.83
1.8-V differential HSTL Class II			25	1.660	0.790	0	0.83
LVDS		100		2.325		0	1.1625
LVPECL		100		3.135		0	1.5675

Notes to Table 4–53:

(1) Input measurement point at internal node is 0.5 V_{CCINT}.
(2) Output measuring point for V_{MEAS} at buffer output is 0.5 V_{CCIO}.
(3) Input stimulus edge rate is 0 to V_{CC} in 0.2 ns (internal signal) from the driver preceding the I/O buffer.
(4) Less than 50-mV ripple on V_{CCIO} and V_{CCPD}, V_{CCINT} = 1.15 V with less than 30-mV ripple.
(5) V_{CCPD} = 2.97 V, less than 50-mV ripple on V_{CCIO} and V_{CCPD}, V_{CCINT} = 1.15 V.

Table 4–74. EP2SGX90 Row Pins Regional Clock Timing Parameters						
Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.444	1.461	2.792	3.108	3.716	ns
t_{COUT}	1.449	1.466	2.792	3.108	3.716	ns
t_{PLLCIN}	-0.348	-0.333	0.204	0.217	0.243	ns
$t_{PLLCOUT}$	-0.343	-0.328	0.212	0.217	0.254	ns

EP2SGX130 Clock Timing Parameters

Tables 4–75 through 4–78 show the maximum clock timing parameters for EP2SGX130 devices.

Table 4–75. EP2SGX130 Column Pins Global Clock Timing Parameters						
Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.980	1.998	3.491	3.706	4.434	ns
t_{COUT}	1.815	1.833	3.237	3.436	4.110	ns
t_{PLLCIN}	-0.027	-0.009	0.307	0.322	0.376	ns
$t_{PLLCOUT}$	-0.192	-0.174	0.053	0.052	0.052	ns

Table 4–76. EP2SGX130 Row Pins Global Clock Timing Parameters						
Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.741	1.759	3.112	3.303	3.950	ns
t_{COUT}	1.746	1.764	3.108	3.299	3.945	ns
t_{PLLCIN}	-0.261	-0.243	-0.089	-0.099	-0.129	ns
$t_{PLLCOUT}$	-0.256	-0.238	-0.093	-0.103	-0.134	ns

Table 4–97. Maximum Output Clock Toggle Rate Derating Factors (Part 2 of 5)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate Derating Factors (ps/pF)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		-3	-4	-5	-3	-4	-5	-3	-4	-5
3.3-V LVCMOS	4 mA	377	391	391	377	391	391	377	391	391
	8 mA	206	212	212	206	212	212	178	212	212
	12 mA	141	145	145	-	-	-	115	145	145
	16 mA	108	111	111	-	-	-	86	111	111
	20 mA	83	88	88	-	-	-	79	88	88
	24 mA	65	72	72	-	-	-	74	72	72
2.5-V LVTTL/ LVCMOS	4 mA	387	427	427	387	427	427	391	427	427
	8 mA	163	224	224	163	224	224	170	224	224
	12 mA	142	203	203	142	203	203	152	203	203
	16 mA	120	182	182	-	-	-	134	182	182
1.8-V LVTTL/ LVCMOS	2 mA	951	1,421	1,421	951	1,421	1,421	904	1,421	1,421
	4 mA	405	516	516	405	516	516	393	516	516
	6 mA	261	325	325	261	325	325	253	325	325
	8 mA	223	274	274	223	274	274	224	274	274
	10 mA	194	236	236	-	-	-	199	236	236
	12 mA	174	209	209	-	-	-	180	209	209
1.5-V LVTTL/ LVCMOS	2 mA	652	963	963	652	963	963	618	963	963
	4 mA	333	347	347	333	347	347	270	347	347
	6 mA	182	247	247	-	-	-	198	247	247
	8 mA	135	194	194	-	-	-	155	194	194
SSTL-2 Class I	8 mA	364	680	680	364	680	680	350	680	680
	12 mA	163	207	207	163	207	207	188	207	207
SSTL-2 Class II	16 mA	118	147	147	118	147	147	94	147	147
	20 mA	99	122	122	-	-	-	87	122	122
	24 mA	91	116	116	-	-	-	85	116	116
SSTL-18 Class I	4 mA	458	570	570	458	570	570	505	570	570
	6 mA	305	380	380	305	380	380	336	380	380
	8 mA	225	282	282	225	282	282	248	282	282
	10 mA	167	220	220	167	220	220	190	220	220
	12 mA	129	175	175	-	-	-	148	175	175

Table 4–112. DLL Frequency Range Specifications (Part 2 of 2)		
Frequency Mode	**Frequency Range (MHz)**	**Resolution (Degrees)**
3	240 to 400 (–3 speed grade)	36
	240 to 350 (–4 and –5 speed grade)	36

Table 4–113. DQS Jitter Specifications for DLL-Delayed Clock (t_{DQS_JITTER}) Note (1)		
Number of DQS Delay Buffer Stages *(2)*	**Commercial (ps)**	**Industrial (ps)**
1	80	110
2	110	130
3	130	180
4	160	210

(1) Peak-to-peak period jitter on the phase-shifted DQS clock. For example, jitter on two delay stages under commercial conditions is 200 ps peak-to-peak or 100 ps.
(2) Delay stages used for requested DQS phase shift are reported in a project's Compilation Report in the Quartus II software.

Table 4–114. DQS Phase-Shift Error Specifications for DLL-Delayed Clock (t_{DQS_PSERR})			
Number of DQS Delay Buffer Stages *(1)*	**–3 Speed Grade (ps)**	**–4 Speed Grade (ps)**	**–5 Speed Grade (ps)**
1	25	30	35
2	50	60	70
3	75	90	105
4	100	120	140

(1) Delay stages used for request DQS phase shift are reported in a project's Compilation Report in the Quartus II software. For example, phase-shift error on two delay stages under -3 conditions is 50 ps peak-to-peak or 25 ps.

Referenced Documents

This chapter references the following documents:

- *Operating Requirements for Altera Devices Data Sheet*
- *PowerPlay Power Analyzer* chapter in volume 3 of the *Quartus II Handbook*.
- *PowerPlay Early Power Estimator (EPE) and Power Analyzer*
- *Quartus II PowerPlay Analysis and Optimization Technology*
- *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*
- *Stratix II GX Transceiver Architecture Overview* chapter in volume 2 of the *Stratix II GX Device Handbook*
- Volume 2, *Stratix II GX Device Handbook*

Document Revision History

Table 6–105 shows the revision history for this chapter.

Table 4–118. Document Revision History (Part 1 of 5)

Date and Document Version	Changes Made	Summary of Changes
June 2009 v4.6	Replaced Table 4–31 Updated: • Table 4–5 • Table 4–6 • Table 4–7 • Table 4–8 • Table 4–9 • Table 4–10 • Table 4–11 • Table 4–12 • Table 4–13 • Table 4–14 • Table 4–15 • Table 4–16 • Table 4–17 • Table 4–18 • Table 4–20 • Table 4–50 • Table 4–95 • Table 4–105 • Table 4–110 • Table 4–111	
October 2007 v4.5	Updated: • Table 4–3 • Table 4–6 • Table 4–16 • Table 4–19 • Table 4–20 • Table 4–21 • Table 4–22 • Table 4–55 • Table 4–106 • Table 4–107 • Table 4–108 • Table 4–109 • Table 4–112	
	Updated title only in Tables 4–88 and 4–89.	
	Minor text edits.	