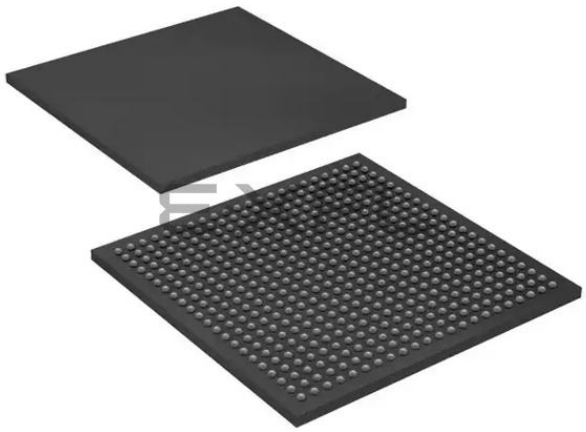

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3022
Number of Logic Elements/Cells	60440
Total RAM Bits	2544192
Number of I/O	291
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2sgx60cf484i4

Table 1–3. Stratix II GX FineLine BGA Package Sizes			
Dimension	**780 Pins**	**1,152 Pins**	**1,508 Pins**
Pitch (mm)	1.00	1.00	1.00
Area (mm^2)	841	1,225	1,600
Length width (mm × mm)	29 × 29	35 × 35	40 × 40

Referenced Document

This chapter references the following document:

- *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*

Document Revision History

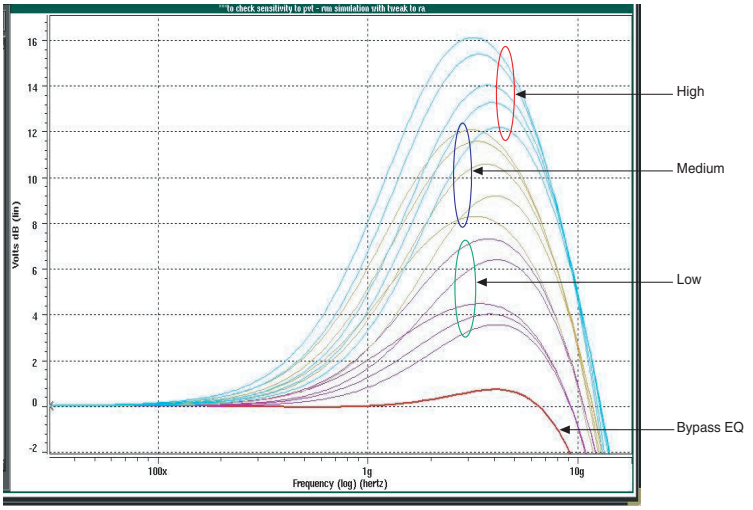
Table 1–4 shows the revision history for this chapter.

Table 1–4. Document Revision History		
Date and Document Version	**Changes Made**	**Summary of Changes**
October 2007, v1.6	Updated "Features" section.	
	Minor text edits.	
August 2007, v1.5	Added "Referenced Documents" section.	
	Minor text edits.	
February 2007, v1.4	• Changed 622 Mbps to 600 Mbps on page 1-2 and Table 1–1. • Deleted "DC coupling" from the Transceiver Block Features list. • Changed 4 to 6 in the PLLs row (columns 3 and 4) of Table 1–1.	
	Added the "Document Revision History" section to this chapter.	Added support information for the Stratix II GX device.
June 2006, v1.3	• Updated Table 1–2.	
April 2006, v1.2	• Updated Table 1–1. • Updated Table 1–2.	Updated numbers for receiver channels and user I/O pin counts in Table 1–2.
February 2006, v1.1	• Updated Table 1–1.	
October 2005 v1.0	Added chapter to the *Stratix II GX Device Handbook*.	

The Stratix II GX receivers also have adaptive equalization capability that adjusts the equalization levels to compensate for changing link characteristics. The adaptive equalization can be powered down dynamically after it selects the appropriate equalization levels.

The receiver equalization circuit is comprised of a programmable amplifier. Each stage is a peaking equalizer with a different center frequency and programmable gain. This allows varying amounts of gain to be applied, depending on the overall frequency response of the channel loss. Channel loss is defined as the summation of all losses through the PCB traces, vias, connectors, and cables present in the physical link. Figure 2–15 shows the frequency response for the 16 programmable settings allowed by the Quartus II software for Stratix II GX devices.

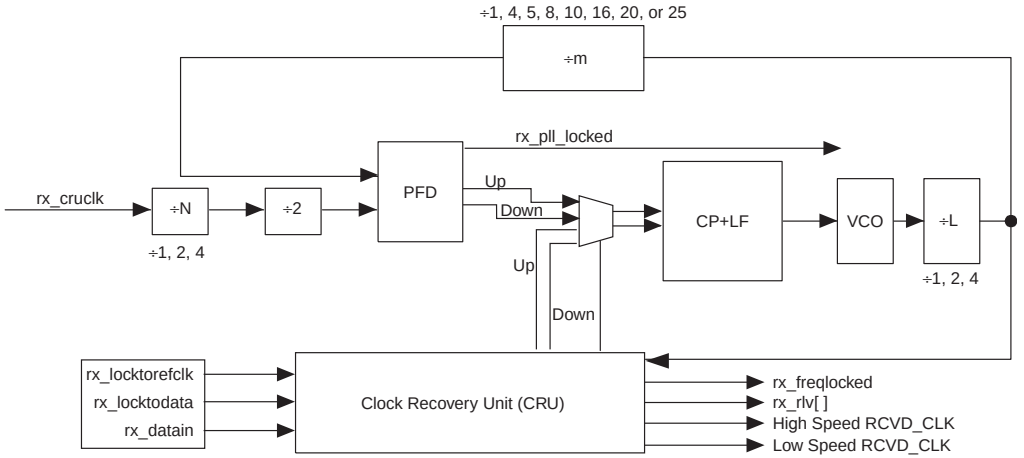
Figure 2–15. Frequency Response



Receiver PLL and CRU

Each transceiver block has four receiver PLLs, lock detectors, signal detectors, run length checkers, and CRU units, each of which is dedicated to a receive channel. If the receive channel associated with a particular receiver PLL or CRU is not used, the receiver PLL and CRU are powered down for the channel. Figure 2–16 shows the receiver PLL and CRU circuits.

Figure 2–16. Receiver PLL and CRU



The receiver PLLs and CRUs can support frequencies up to 6.375 Gbps. The input clock frequency is limited to the full clock range of 50 to 622 MHz but only when using `REFCLK0` or `REFCLK1`. An optional `RX_PLL_LOCKED` port is available to indicate whether the PLL is locked to the reference clock. The receiver PLL has a programmable loop bandwidth which can be set to low, medium, or high. The Quartus II software can statically set the loop bandwidth parameter.

All the parameters listed are programmable in the Quartus II software. The receiver PLL has the following features:

- Operates from 600 Mbps to 6.375 Gbps.
- Uses a reference clock between 50 MHz and 622.08 MHz.
- Programmable bandwidth settings: low, medium, and high.
- Programmable `rx_locktorefclk` (forces the receiver PLL to lock to the reference clock) and `rx_locktodata` (forces the receiver PLL to lock to the data).
- The voltage-controlled oscillator (VCO) operates at half rate and has two modes. These modes are for low or high frequency operation and provide optimized phase-noise performance.
- Programmable frequency multiplication *W* of 1, 4, 5, 8, 10, 16, 20, and 25. Not all settings are supported for any particular frequency.
- Two lock indication signals are provided. They are found in PFD mode (lock-to-reference clock), and PD (lock-to-data).

Control and Status Signals

The rx_enapatternalign signal is the FPGA control signal that enables word alignment in non-automatic modes. The rx_enapatternalign signal is not used in automatic modes (PCI Express, XAUI, GIGE, CPRI, and Serial RapidIO).

In manual alignment mode, after the rx_enapatternalign signal is activated, the rx_syncstatus signal goes high for one parallel clock cycle to indicate that the alignment pattern has been detected and the word boundary has been locked. If the rx_enapatternalign is deactivated, the rx_syncstatus signal acts as a re-synchronization signal to signify that the alignment pattern has been detected but not locked on a different word boundary.

When using the synchronization state machine, the rx_syncstatus signal indicates the link status. If the rx_syncstatus signal is high, link synchronization is achieved. If the rx_syncstatus signal is low, synchronization has not yet been achieved, or there were enough code group errors to lose synchronization.

In some modes, the rx_enapatternalign signal can be configured to operate as a rising edge signal.

For more information on manual alignment modes, refer to the *Stratix II GX Device Handbook*, volume 2.

When the rx_enapatternalign signal is sensitive to the rising edge, each rising edge triggers a new boundary alignment search, clearing the rx_syncstatus signal.

The rx_patterndetect signal pulses high during a new alignment, and also whenever the alignment pattern occurs on the current word boundary.

SONET/SDH

In all the SONET/SDH modes, you can configure the word aligner to either align to A1A2 or A1A1A2A2 patterns. Once the pattern is found, the word boundary is aligned and the word aligner asserts the rx_patterndetect signal for one clock cycle.

Applications and Protocols Supported with Stratix II GX Devices

Each Stratix II GX transceiver block is designed to operate at any serial bit rate from 600 Mbps to 6.375 Gbps per channel. The wide data rate range allows Stratix II GX transceivers to support a wide variety of standards and protocols, such as PCI Express, GIGE, SONET/SDH, SDI, OIF-CEI, and XAUI. Stratix II GX devices are ideal for many high-speed communication applications, such as high-speed backplanes, chip-to-chip bridges, and high-speed serial communications links.

Example Applications Support for Stratix II GX

Stratix II GX devices can be used for many applications, including:

- Traffic management with various levels of quality of service (QoS) and integrated serial backplane interconnect
- Multi-port single-protocol switching (for example, PCI Express, GIGE, XAUI switch, or SONET/SDH)

Logic Array Blocks

Each logic array block (LAB) consists of eight adaptive logic modules (ALMs), carry chains, shared arithmetic chains, LAB control signals, local interconnects, and register chain connection lines. The local interconnect transfers signals between ALMs in the same LAB. Register chain connections transfer the output of an ALM register to the adjacent ALM register in a LAB. The Quartus II Compiler places associated logic in a LAB or adjacent LABs, allowing the use of local, shared arithmetic chain, and register chain connections for performance and area efficiency. Table 2–17 shows Stratix II GX device resources. Figure 2–32 shows the Stratix II GX LAB structure.

Table 2–17. Stratix II GX Device Resources

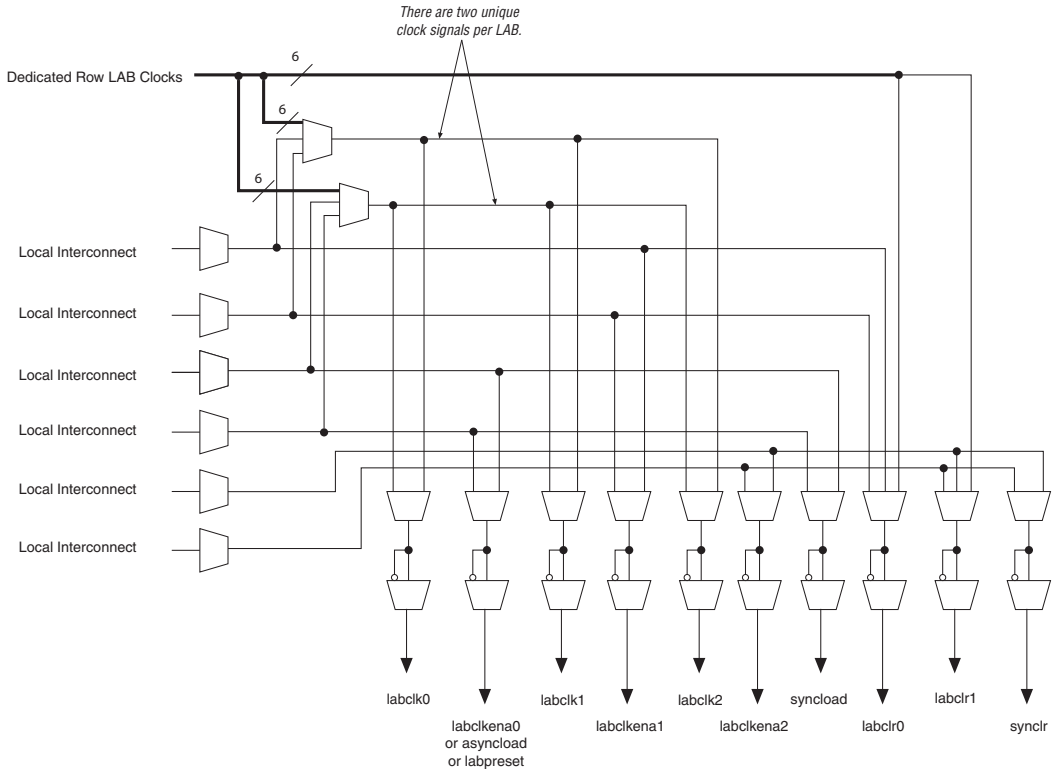
Device	M512 RAM Columns/Blocks	M4K RAM Columns/Blocks	M-RAM Blocks	DSP Block Columns/Blocks	LAB Columns	LAB Rows
EP2SGX30	6/202	4/144	1	2/16	49	36
EP2SGX60	7/329	5/255	2	3/36	62	51
EP2SGX90	8/488	6/408	4	3/48	71	68
EP2SGX130	9/699	7/609	6	3/63	81	87

load acts as a preset when the asynchronous load data input is tied high. When the asynchronous load/preset signal is used, the `labclkena0` signal is no longer available.

The LAB row clocks `[5..0]` and LAB local interconnect generate the LAB-wide control signals. The MultiTrack™ interconnects have inherently low skew. This low skew allows the MultiTrack interconnects to distribute clock and control signals in addition to data.

Figure 2–34 shows the LAB control signal generation circuit.

Figure 2–34. LAB-Wide Control Signals



Modes of Operation

The adder, subtractor, and accumulate functions of a DSP block have four modes of operation:

- Simple multiplier
- Multiply-accumulator
- Two-multipliers adder
- Four-multipliers adder

Table 2–22 shows the different number of multipliers possible in each DSP block mode according to size. These modes allow the DSP blocks to implement numerous applications for DSP including FFTs, complex FIR, FIR, 2D FIR filters, equalizers, IIR, correlators, matrix multiplication, and many other functions. The DSP blocks also support mixed modes and mixed multiplier sizes in the same block. For example, half of one DSP block can implement one 18 × 18-bit multiplier in multiply-accumulator mode, while the other half of the DSP block implements four 9 × 9-bit multipliers in simple multiplier mode.

Table 2–22. Multiplier Size and Configurations per DSP Block

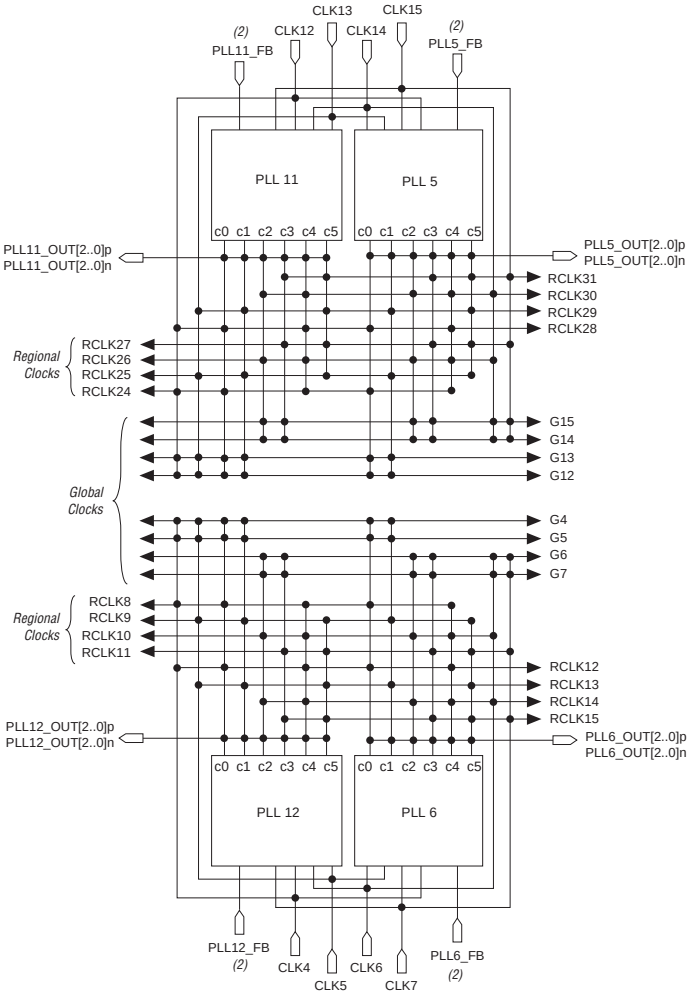
DSP Block Mode	9 × 9	18 × 18	36 × 36
Multiplier	Eight multipliers with eight product outputs	Four multipliers with four product outputs	One multiplier with one product output
Multiply-accumulator	—	Two 52-bit multiply-accumulate blocks	—
Two-multipliers adder	Four two-multiplier adder (two 9 × 9 complex multiply)	Two two-multiplier adder (one 18 × 18 complex multiply)	—
Four-multipliers adder	Two four-multiplier adder	One four-multiplier adder	—

DSP Block Interface

The Stratix II GX device DSP block input registers can generate a shift register that can cascade down in the same DSP block column. Dedicated connections between DSP blocks provide fast connections between the shift register inputs to cascade the shift register chains. You can cascade registers within multiple DSP blocks for 9 × 9- or 18 × 18-bit FIR filters larger than four taps, with additional adder stages implemented in ALMs. If the DSP block is configured as 36 × 36 bits, the adder, subtractor, or accumulator stages are implemented in ALMs. Each DSP block can route the shift register chain out of the block to cascade multiple columns of DSP blocks.

Figure 2–73 shows the global and regional clocking from enhanced PLL outputs and top and bottom CLK pins.

Figure 2–73. Global and Regional Clock Connections from Top and Bottom Clock Pins and Enhanced PLL Outputs *Notes (1), (2)*

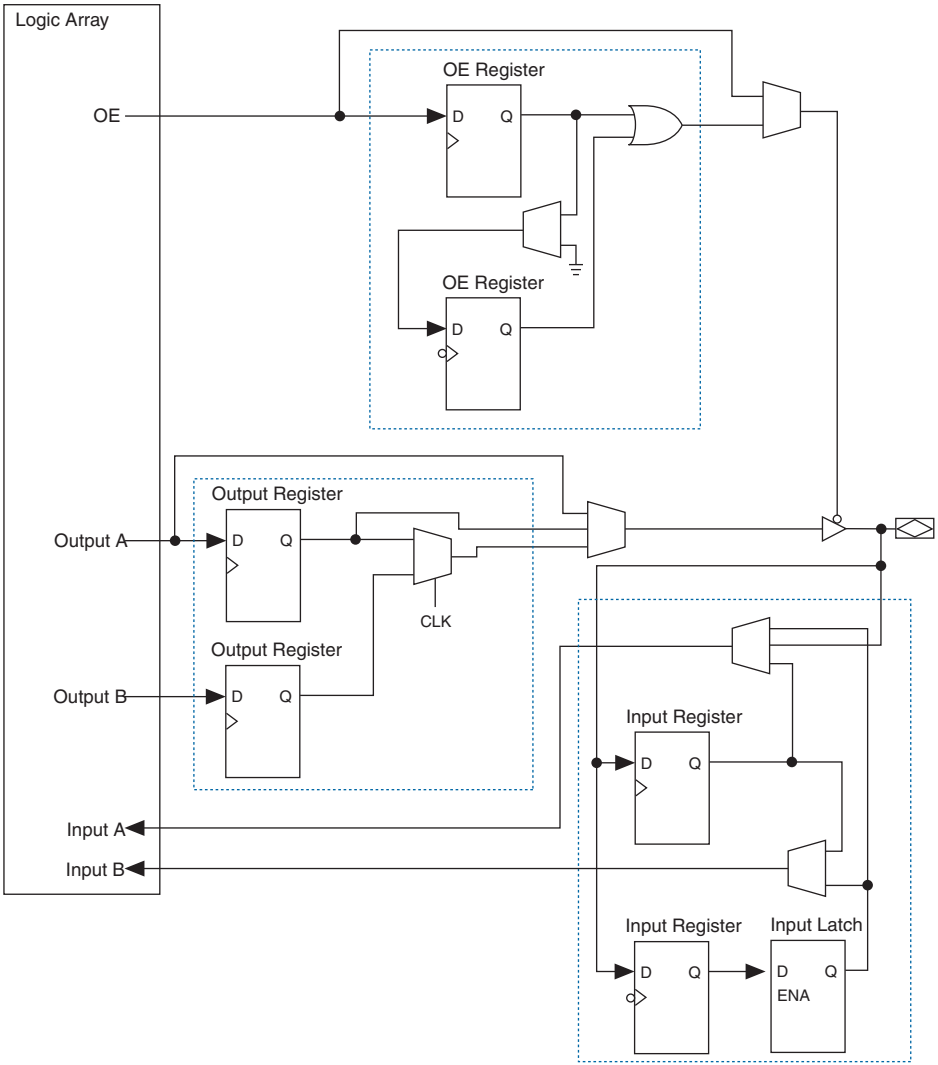


Notes to Figure 2–73:

(1) EP2SGX30C/D and EP2SGX60C/D devices only have two enhanced PLLs (5 and 6), but the connectivity from these two PLLs to the global and regional clock networks remains the same as shown.

(2) If the design uses the feedback input, you will lose one (or two, if FBIN is differential) external clock output pin.

Figure 2–76. Stratix II GX IOE Structure



The IOEs are located in I/O blocks around the periphery of the Stratix II GX device. There are up to four IOEs per row I/O block and four IOEs per column I/O block. The row I/O blocks drive row, column, or direct link interconnects. The column I/O blocks drive column interconnects.

A path in which a pin directly drives a register can require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinational logic may not require the delay. Programmable delays exist for decreasing input-pin-to-logic-array and IOE input register delays. The Quartus II Compiler can program these delays to automatically minimize setup time while providing a zero hold time. Programmable delays can increase the register-to-pin delays for output and/or output enable registers. Programmable delays are no longer required to ensure zero hold times for logic array register-to-IOE register transfers. The Quartus II Compiler can create the zero hold time for these transfers. Table 2–30 shows the programmable delays for Stratix II GX devices.

Table 2–30. Stratix II GX Programmable Delay Chain

Programmable Delays	Quartus II Logic Option
Input pin to logic array delay	Input delay from pin to internal cells
Input pin to input register delay	Input delay from pin to input register
Output pin delay	Delay from output register to output pin
Output enable register t_{CO} delay	Delay to output enable pin

The IOE registers in Stratix II GX devices share the same source for clear or preset. You can program preset or clear for each individual IOE. You can also program the registers to power up high or low after configuration is complete. If programmed to power up low, an asynchronous clear can control the registers. If programmed to power up high, an asynchronous preset can control the registers. This feature prevents the inadvertent activation of another device's active-low input upon power-up. If one register in an IOE uses a preset or clear signal, all registers in the IOE must use that same signal if they require preset or clear. Additionally, a synchronous reset signal is available for the IOE registers.

Double Data Rate I/O Pins

Stratix II GX devices have six registers in the IOE, which support DDR interfacing by clocking data on both positive and negative clock edges. The IOEs in Stratix II GX devices support DDR inputs, DDR outputs, and bidirectional DDR modes. When using the IOE for DDR inputs, the two input registers clock double rate input data on alternating edges. An input latch is also used in the IOE for DDR input acquisition. The latch holds the data that is present during the clock high times, allowing both bits of data to be synchronous with the same clock edge (either rising or falling). Figure 2–82 shows an IOE configured for DDR input. Figure 2–83 shows the DDR input timing diagram.

Table 3–1. Stratix II GX JTAG Instructions

JTAG Instruction	Instruction Code	Description
SAMPLE/PRELOAD	00 0000 0101	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation and permits an initial data pattern to be output at the device pins. Also used by the SignalTap II embedded logic analyzer.
EXTEST *(1)*	00 0000 1111	Allows the external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	11 1111 1111	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	00 0000 0111	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	00 0000 0110	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
HIGHZ *(1)*	00 0000 1011	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins.
CLAMP *(1)*	00 0000 1010	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding the I/O pins to a state defined by the data in the boundary-scan register.
ICR instructions		Used when configuring a Stratix II GX device via the JTAG port with a USB-Blaster™, MasterBlaster™, ByteBlasterMV™, or ByteBlaster II download cable, or when using a **.jam** or **.jbc** via an embedded processor or JRunner.
PULSE_NCONFIG	00 0000 0001	Emulates pulsing the nCONFIG pin low to trigger reconfiguration even though the physical pin is unaffected.
CONFIG_IO *(2)*	00 0000 1101	Allows configuration of I/O standards through the JTAG chain for JTAG testing. Can be executed before, during, or after configuration. Stops configuration if executed during configuration. Once issued, the CONFIG_IO instruction holds nSTATUS low to reset the configuration device. nSTATUS is held low until the IOE configuration register is loaded and the TAP controller state machine transitions to the UPDATE_DR state.
SignalTap II instructions		Monitors internal device operation with the SignalTap II embedded logic analyzer.

Notes to Table 3–1:

(1) Bus hold and weak pull-up resistor features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.

(2) For more information on using the CONFIG_IO instruction, refer to the *MorphIO: An I/O Reconfiguration Solution for Altera Devices White Paper.*

Table 4–6. Stratix II GX Transceiver Block AC Specification (Part 3 of 6)

Symbol / Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
reconfig_clk clock frequency		2.5	-	50	2.5	-	50	2.5	-	50	MHz
Transceiver block minimum power-down pulse width		100	-	-	100	-	-	100	-	-	ns
Receiver											
Data rate		600	-	6375	600	-	5000	600	-	4250	Mbps
Absolute V_{MAX} for a receiver pin *(1)*		-	-	2.0	-	-	2.0	-	-	2.0	V
Absolute V_{MIN} for a receiver pin		-0.4	-	-	-0.4	-	-	-0.4	-	-	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p)	V_{CM} = 0.85 V	-	-	3.3	-	-	3.3	-	-	3.3	V
Minimum peak-to-peak differential input voltage V_{ID} (diff p-p)	V_{CM} = 0.85 V DC Gain = ≥ 3 dB	160	-	-	160	-	-	160	-	-	mV
V_{ICM}	V_{ICM} = 0.85 V setting	850±10%			850±10%			850±10%			mV
	V_{ICM} = 1.2 V setting *(11)*	1200±10%			1200±10%			1200±10%			mV
On-chip termination resistors	100 Ω setting	100±15%			100±15%			100±15%			Ω
	120 Ω setting	120±15%			120±15%			120±15%			Ω
	150 Ω setting	150±15%			150±15%			150±15%			Ω
Bandwidth at 6.375 Gbps	BW = Low	-	20	-	-	-	-	-	-	-	MHz
	BW = Med	-	35	-	-	-	-	-	-	-	MHz
	BW = High	-	45	-	-	-	-	-	-	-	MHz

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 4 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Sinusoidal jitter FC-1	Fc/25000	> 1.5			> 1.5			> 1.5			UI
	Fc/1667	> 0.1			> 0.1			> 0.1			UI
Deterministic jitter FC-2	Pattern = CJTPAT No Equalization DC Gain = 0 dB	> 0.33			> 0.33			> 0.33			UI
Random jitter FC-2	Pattern = CJTPAT No Equalization DC Gain = 0 dB	> 0.29			> 0.29			> 0.29			UI
Sinusoidal jitter FC-2	Fc/25000	> 1.5			> 1.5			> 1.5			UI
	Fc/1667	> 0.1			> 0.1			> 0.1			UI
Deterministic jitter FC-4	Pattern = CJTPAT No Equalization DC Gain = 0 dB	> 0.33			> 0.33			> 0.33			UI
Random jitter FC-4	Pattern = CJTPAT No Equalization DC Gain = 0 dB	> 0.29			> 0.29			> 0.29			UI
Sinusoidal jitter FC-4	Fc/25000	> 1.5			> 1.5			> 1.5			UI
	Fc/1667	> 0.1			> 0.1			> 0.1			UI
XAUI Transmit Jitter Generation *(9)*											
Total jitter at 3.125 Gbps	REFCLK = 156.25 MHz Pattern = CJPAT V_{OD} = 1200 mV No Pre-emphasis	-	-	0.3	-	-	0.3	-	-	0.3	UI
Deterministic jitter at 3.125 Gbps	REFCLK = 156.25 MHz Pattern = CJPAT V_{OD} = 1200 mV No Pre-emphasis	-	-	0.17	-	-	0.17	-	-	0.17	UI
XAUI Receiver Jitter Tolerance *(9)*											
Total jitter	Pattern = CJPAT No Equalization DC Gain = 3 dB	> 0.65			> 0.65			> 0.65			UI
Deterministic jitter	Pattern = CJPAT No Equalization DC Gain = 3 dB	> 0.37			> 0.37			> 0.37			UI

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 16 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SDI Transmitter Jitter Generation *(16)*											
Alignment Jitter (peak-to-peak)	Data Rate = 1.485 Gbps (HD) REFCLK = 74.25 MHz Pattern = ColorBar Vod = 800 mV No Pre-emphasis Low-Frequency Roll-Off = 100 KHz		0.2			0.2			0.2		UI
	Data Rate = 2.97 Gbps (3G) REFCLK = 148.5 MHz Pattern = ColorBar Vod = 800 mV No Pre-emphasis Low-Frequency Roll-Off = 100 KHz		0.3			0.3			0.3		UI

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 19 of 19)											
Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	

Notes to Table 4–19:

(1) Dedicated REFCLK pins were used to drive the input reference clocks.
(2) Jitter numbers specified are valid for the stated conditions only.
(3) Refer to the protocol characterization documents for detailed information.
(4) HiGig configuration is available in a -3 speed grade only. For more information, refer to the *Stratix II GX Transceiver Architecture Overview* chapter in volume 2 of the *Stratix II GX Device Handbook*.
(5) Stratix II GX transceivers meet CEI jitter generation specification of 0.3 UI for a V_{OD} range of 400 mV to 1000 mV.
(6) The Sinusoidal Jitter Tolerance Mask is defined only for low voltage (LV) variant of CPRI.
(7) The jitter numbers for SONET/SDH are compliant to the GR-253-CORE Issue 3 Specification.
(8) The jitter numbers for Fibre Channel are compliant to the FC-PI-4 Specification revision 6.10.
(9) The jitter numbers for XAUI are compliant to the IEEE802.3ae-2002 Specification.
(10) The jitter numbers for PCI Express are compliant to the PCIe Base Specification 2.0.
(11) The jitter numbers for Serial RapidIO are compliant to the RapidIO Specification 1.3.
(12) The jitter numbers for GIGE are compliant to the IEEE802.3-2002 Specification.
(13) The jitter numbers for HiGig are compliant to the IEEE802.3ae-2002 Specification.
(14) The jitter numbers for (OIF) CEI are compliant to the OIF-CEI-02.0 Specification.
(15) The jitter numbers for CPRI are compliant to the CPRI Specification V2.1.
(16) The HD-SDI and 3G-SDI jitter numbers are compliant to the SMPTE292M and SMPTE424M Specifications.
(17) The Fibre Channel transmitter jitter generation numbers are compliant to the specification at β_T interoperability point.
(18) The Fibre Channel receiver jitter tolerance numbers are compliant to the specification at β_R interoperability point.

Table 4–20 provides information on recommended input clock jitter for each mode.

Table 4–20. Recommended Input Clock Jitter (Part 1 of 2)						
Mode	Reference Clock (MHz)	Vectron LVPECL XO Type/Model	Frequency Range (MHz)	RMS Jitter (12 kHz to 20 MHz) (ps)	Period Jitter (Peak to Peak) (ps)	Phase Noise at 1 MHz (dB c/Hz)
PCI-E	100	VCC6-Q/R	10 to 270	0.3	23	-149.9957
(OIF) CEI PHY	156.25	VCC6-Q/R	10 to 270	0.3	23	-146.2169
	622.08	VCC6-Q	270 to 800	2	30	Not available
GIGE	62.5	VCC6-Q/R	10 to 270	0.3	23	-149.9957
	125	VCC6-Q/R	10 to 270	0.3	23	-146.9957
XAUI	156.25	VCC6-Q/R	10 to 270	0.3	23	-146.2169

Table 4–35. SSTL-18 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.71	1.8	1.89	V
V_{REF}	Reference voltage		0.855	0.9	0.945	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{IH} (DC)	High-level DC input voltage		V_{REF} + 0.125			V
V_{IL} (DC)	Low-level DC input voltage				V_{REF} – 0.125	V
V_{IH} (AC)	High-level AC input voltage		V_{REF} + 0.25			V
V_{IL} (AC)	Low-level AC input voltage				V_{REF} – 0.25	V
V_{OH}	High-level output voltage	I_{OH} = –6.7 mA *(1)*	V_{TT} + 0.475			V
V_{OL}	Low-level output voltage	I_{OL} = 6.7 mA *(1)*			V_{TT} – 0.475	V

Note to Table 4–35:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Table 4–36. SSTL-18 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.71	1.8	1.89	V
V_{REF}	Reference voltage		0.855	0.9	0.945	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{IH} (DC)	High-level DC input voltage		V_{REF} + 0.125			V
V_{IL} (DC)	Low-level DC input voltage				V_{REF} – 0.125	V
V_{IH} (AC)	High-level AC input voltage		V_{REF} + 0.25			V
V_{IL} (AC)	Low-level AC input voltage				V_{REF} – 0.25	V
V_{OH}	High-level output voltage	I_{OH} = –13.4 mA *(1)*	V_{CCIO} – 0.28			V
V_{OL}	Low-level output voltage	I_{OL} = 13.4 mA *(1)*			0.28	V

Note to Table 4–36:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Table 4–59. M512 Block Internal Timing Microparameters (Part 1 of 2)

Symbol	Parameter	-3 Speed Grade (2)		-3 Speed Grade (3)		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{M512RC}	Synchronous read cycle time	2089	2318	2089	2433	2089	2587	2089	3104	ps
$t_{M512WERESU}$	Write or read enable setup time before clock	22		23		24		29		ps
$t_{M512WEREH}$	Write or read enable hold time after clock	203		213		226		272		ps
$t_{M512DATASU}$	Data setup time before clock	22		23		24		29		ps
$t_{M512DATAH}$	Data hold time after clock	203		213		226		272		ps
$t_{M512WADDRSU}$	Write address setup time before clock	22		23		24		29		ps
$t_{M512WADDRH}$	Write address hold time after clock	203		213		226		272		ps
$t_{M512RADDRSU}$	Read address setup time before clock	22		23		24		29		ps
$t_{M512RADDRH}$	Read address hold time after clock	203		213		226		272		ps
$t_{M512DATACO1}$	Clock-to-output delay when using output registers	298	478	298	501	298	533	298	640	ps
$t_{M512DATACO2}$	Clock-to-output delay without output registers	2102	2345	2102	2461	2102	2616	2102	3141	ps
$t_{M512CLKL}$	Minimum clock low time	1315		1380		1468		1762		ps
$t_{M512CLKH}$	Minimum clock high time	1315		1380		1468		1762		ps

Table 4–81. Stratix II GX IOE Programmable Delay on Row Pins Note (1)													
Parameter	Paths Affected	Available Settings	Minimum Timing		-3 Speed Grade		-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		Unit
			Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	
Input delay from pin to internal cells	Pad to I/O dataout to logic array	8	0	1782	0	2876	0	3020	0	3212	0	3853	ps
Input delay from pin to input register	Pad to I/O input register	64	0	2054	0	3270	0	3434	0	3652	0	4381	ps
Delay from output register to output pin	I/O output register to pad	2	0	332	0	500	0	525	0	559	0	670	ps
Output enable pin delay	t_{XZ}, t_{ZX}	2	0	320	0	483	0	507	0	539	0	647	ps

(1) The incremental values for the settings are generally linear. For the exact delay associated with each setting, use the latest version of the Quartus II software.

Default Capacitive Loading of Different I/O Standards

See Table 4–82 for default capacitive loading of different I/O standards.

Table 4–82. Default Loading of Different I/O Standards for Stratix II GX Devices (Part 1 of 2)		
I/O Standard	Capacitive Load	Unit
LVTTL	0	pF
LVCMOS	0	pF
2.5 V	0	pF
1.8 V	0	pF
1.5 V	0	pF
PCI	10	pF
PCI-X	10	pF
SSTL-2 Class I	0	pF
SSTL-2 Class II	0	pF

Table 4–111. Fast PLL Specifications (Part 2 of 2)					
Name	**Description**	**Min**	**Typ**	**Max**	**Unit**
f_{VCO}	Upper VCO frequency range for –3 and –4 speed grades	300		1,040	MHz
	Upper VCO frequency range for –5 speed grades	300		840	MHz
	Lower VCO frequency range for –3 and –4 speed grades	150		520	MHz
	Lower VCO frequency range for –5 speed grades	150		420	MHz
f_{OUT}	PLL output frequency to GCLK or RCLK	4.6875		550	MHz
	PLL output frequency to LVDS or DPA clock	150		1,040	MHz
f_{OUT_EXT}	PLL clock output frequency to regular I/O	4.6875		*(1)*	MHz
$t_{CONFIGPLL}$	Time required to reconfigure scan chains for fast PLLs		$75/f_{SCANCLK}$		ns
f_{CLBW}	PLL closed-loop bandwidth	1.16	5	28	MHz
t_{LOCK}	Time required for the PLL to lock from the time it is enabled or the end of the device configuration		0.03	1	ms
t_{PLL_PSERR}	Accuracy of PLL phase shift			±30	ps
t_{ARESET}	Minimum pulse width on areset signal.	10			ns
$t_{ARESET\_RECONFIG}$	Minimum pulse width on the areset signal when using PLL reconfiguration. Reset the PLL after scandone goes high.	500			ns

(1) This is limited by the I/O f_{MAX}. See Tables 4–91 through 4–95 for the maximum.

External Memory Interface Specifications

Tables 4–112 through 4–116 contain Stratix II GX device specifications for the dedicated circuitry used for interfacing with external memory devices.

Table 4–112. DLL Frequency Range Specifications (Part 1 of 2)		
Frequency Mode	**Frequency Range (MHz)**	**Resolution (Degrees)**
0	100 to 175	30
1	150 to 230	22.5
2	200 to 350 (–3 speed grade)	30
	200 to 310 (–4 and –5 speed grade)	30

Table 4–118. Document Revision History (Part 4 of 5)

Date and Document Version	Changes Made	Summary of Changes
June 2006, v4.0	• Updated Table 6–5. • Updated Table 6–6. • Updated all values in Table 6–7. • Added Tables 6–8 and 6–9. • Added Figures 6–1 through 6–4. • Updated Table 6–18. • Updated Tables 6–85 through 6–96. • Added Table 6–80, Stratix II GX Maximum Output Clock Rate for Dedicated Clock Pins. • Updated Table 6–100. • In "I/O Timing Measurement Methodology" section, updated Table 6–42. • In "Internal Timing Parameters" section, updated Tables 6–43 through 6–48. • In "Stratix II GX Clock Timing Parameters" section, updated Tables 6–50 through 6–65. • In "IOE Programmable Delay" section, updated Tables 6–67 and 6–68. • In "I/O Delays" section, updated Tables 6–71 through 6–74. • In "Maximum Input & Output Clock Toggle Rate" section, updated Tables 6–75 through 6–83. • In "DCD Measurement Techniques" section, updated Tables 6–85 through 6–92. • In "High-Speed I/O Specifications" section, updated Tables 6–94 through 6–96. • In "External Memory Interface Specifications" section, updated Table 6–100.	• Removed rows for V_{ID}, V_{OD}, V_{ICM}, and V_{OCM} from Table 6–5. • Updated values for rx, tx, and `refclkb` in Table 6–6. • Removed table containing 1.2-V PCML I/O information. That information is in Table 6–7. • Added values to Table 6–100.