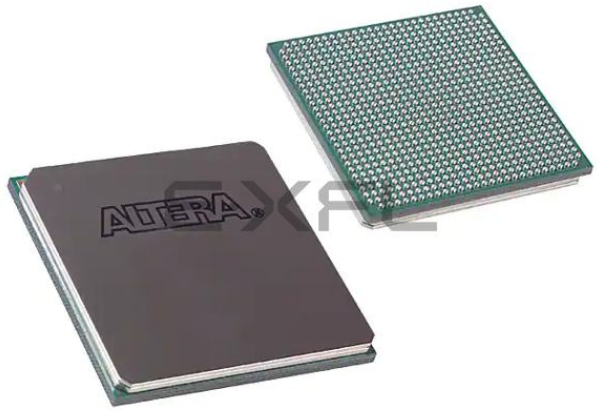

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3022
Number of Logic Elements/Cells	60440
Total RAM Bits	2544192
Number of I/O	364
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	780-BBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2sgx60cf780c3n

This module detects word boundaries for the 8B/10B-based protocols, SONET, 16-bit, and 20-bit proprietary protocols. This module is also used to align to specific programmable patterns in PRBS7/23 test mode.

Pattern Detection

The programmable pattern detection logic can be programmed to align word boundaries using a single 7-, 8-, 10-, 16-, 20, or 32-bit pattern. The pattern detector can either do an exact match, or match the exact pattern and the complement of a given pattern. Once the programmed pattern is found, the data stream is aligned to have the pattern on the LSB portion of the data output bus.

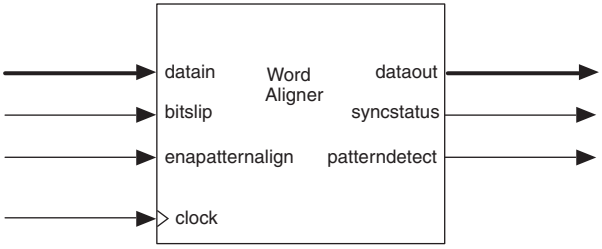
XAUI, GIGE, PCI Express, and Serial RapidIO standards have embedded state machines for symbol boundary synchronization. These standards use K28.5 as their 10-bit programmed comma pattern. Each of these standards uses different algorithms before signaling symbol boundary acquisition to the FPGA.

The pattern detection logic searches from the LSB to the most significant bit (MSB). If multiple patterns are found within the search window, the pattern in the lower portion of the data stream (corresponding to the pattern received earlier) is aligned and the rest of the matching patterns are ignored.

Once a pattern is detected and the data bus is aligned, the word boundary is locked. The two detection status signals (`rx_syncstatus` and `rx_patterndetect`) indicate that an alignment is complete.

Figure 2–18 is a block diagram of the word aligner.

Figure 2–18. Word Aligner



GIGE Mode

In GIGE mode, the rate matcher adheres to the specifications in clause 36 of the IEEE 802.3 documentation for idle additions or removals. The rate matcher performs clock compensation only on /I2/ ordered sets, composed of a /K28.5/+ followed by a /D16.2/-. The rate matcher does not perform clock compensation on any other ordered set combinations. An /I2/ is added or deleted automatically based on the number of words in the FIFO buffer. A K28.4 is given at the control and data ports when the FIFO buffer is in an overflow or underflow condition.

XAUI Mode

In XAUI mode, the rate matcher adheres to clause 48 of the IEEE 802.3ae specification for clock rate compensation. The rate matcher performs clock compensation on columns of /R/ (/K28.0/), denoted by //R//. An //R// is added or deleted automatically based on the number of words in the FIFO buffer.

PCI Express Mode

PCI Express mode operates at a data rate of 2.5 Gbps, and supports lane widths of ×1, ×2, ×4, and ×8. The rate matcher can support up to ± 300-PPM differences between the upstream transmitter and the receiver. The rate matcher looks for the skip ordered sets (SOS), which usually consist of a /K28.5/ comma followed by three /K28.0/ skip characters. The rate matcher deletes or inserts skip characters when necessary to prevent the rate matching FIFO buffer from overflowing or underflowing.

The Stratix II GX rate matcher in PCI Express mode has FIFO overflow and underflow protection. In the event of a FIFO overflow, the rate matcher deletes any data after the overflow condition to prevent FIFO pointer corruption until the rate matcher is not full. In an underflow condition, the rate matcher inserts 9'h1FE (/K30.7/) until the FIFO is not empty. These measures ensure that the FIFO can gracefully exit the overflow and underflow condition without requiring a FIFO reset.

8B/10B Decoder

The 8B/10B decoder (Figure 2–21) is part of the Stratix II GX transceiver digital blocks (PCS) and lies in the receiver path between the rate matcher and the byte deserializer blocks. The 8B/10B decoder operates in single-width and double-width modes, and can be bypassed if the 8B/10B decoding is not necessary. In single-width mode, the 8B/10B decoder restores the 8-bit data + 1-bit control identifier from the 10-bit code. In double-width mode, there are two 8B/10B decoders in parallel, which restores the 16-bit (2 × 8-bit) data + 2-bit (2 × 1-bit) control identifier from the 20-bit (2 × 10-bit) code. This 8B/10B decoder conforms to the IEEE 802.3 1998 edition standards.

When the FIFO pointers initialize, the receiver domain clock must remain phase locked to receiver FPGA clock.

After resetting the receiver FIFO buffer, writing to the receiver FIFO buffer begins and continues on each parallel clock. The phase compensation FIFO buffer is eight words deep for PIPE mode and four words deep for all other modes.

Loopback Modes

The Stratix II GX transceiver has built-in loopback modes for debugging and testing. The loopback modes are configured in the Stratix II GX ALT2GXB megafunction in the Quartus II software. The available loopback modes are:

- Serial loopback
- Parallel loopback
- Reverse serial loopback
- Reverse serial loopback (pre-CDR)
- PCI Express PIPE reverse parallel loopback (available only in PIPE mode)

Serial Loopback

The serial loopback mode exercises all the transceiver logic, except for the input buffer. Serial loopback is available for all non-PIPE modes. The loopback function is dynamically enabled through the `rx_seriallpbken` port on a channel-by-channel basis.

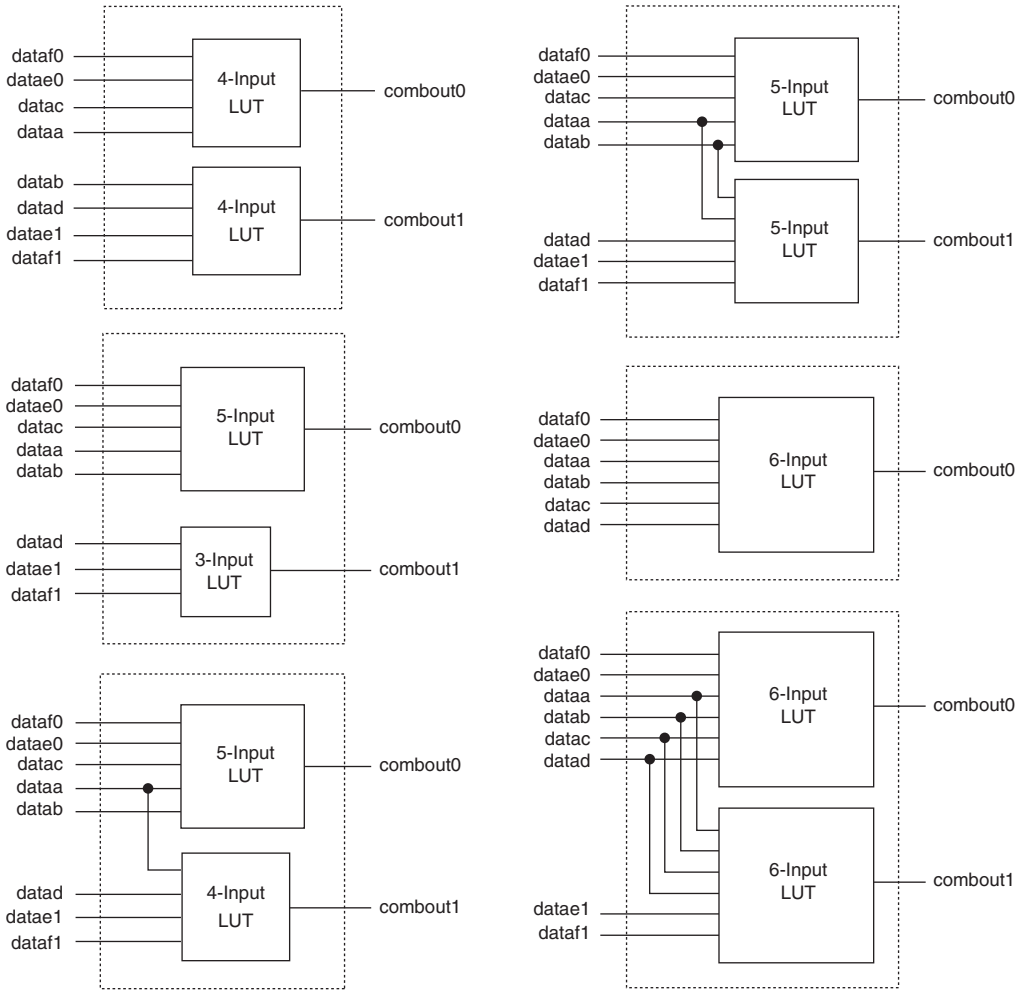
In serial loopback mode, the data on the transmit side is sent by the PLD. A separate mode is available in the ALT2GXB megafunction under Basic protocol mode, in which PRBS data is generated and verified internally in the transceiver. The PRBS patterns available in this mode are shown in Table 2–10.

Table 2–10 shows the BIST data output and verifier alignment pattern.

Table 2–10. BIST Data Output and Verifier Alignment Pattern

Pattern	Polynomial	Parallel Data Width			
		8-Bit	10-Bit	16-Bit	20-Bit
PRBS-7	×7 + ×6 + 1				✓
PRBS-10	×10 + ×7 + 1		✓		

Figure 2–37. ALM in Normal Mode *Note (1)*



Note to Figure 2–37:

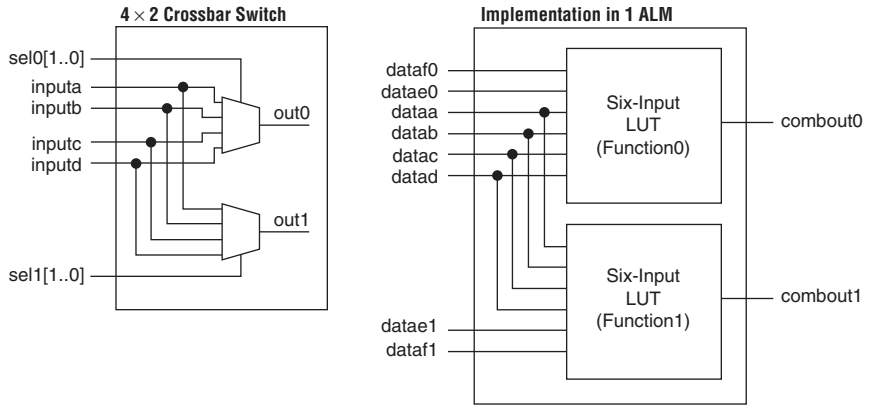
(1) Combinations of functions with less inputs than those shown are also supported. For example, combinations of functions with the following number of inputs are supported: 4 and 3, 3 and 3, 3 and 2, 5 and 2, etc.

The normal mode provides complete backward compatibility with four-input LUT architectures. Two independent functions of four inputs or less can be implemented in one Stratix II GX ALM. In addition, a five-input function and an independent three-input function can be implemented without sharing inputs.

To pack two five-input functions into one ALM, the functions must have at least two common inputs. The common inputs are dataa and datab. The combination of a four-input function with a five-input function requires one common input (either dataa or datab).

To implement two six-input functions in one ALM, four inputs must be shared and the combinational function must be the same. For example, a 4 × 2 crossbar switch (two 4-to-1 multiplexers with common inputs and unique select lines) can be implemented in one ALM, as shown in Figure 2–38. The shared inputs are dataa, datab, datac, and datad, while the unique select lines are datae0 and dataf0 for function0, and datae1 and dataf1 for function1. This crossbar switch consumes four LUTs in a four-input LUT-based architecture.

Figure 2–38. 4 × 2 Crossbar Switch Example



In a sparsely used device, functions that could be placed into one ALM can be implemented in separate ALMs. The Quartus II Compiler spreads a design out to achieve the best possible performance. As a device begins to fill up, the Quartus II software automatically utilizes the full potential of the Stratix II GX ALM. The Quartus II Compiler automatically searches for functions of common inputs or completely independent functions to be placed into one ALM and to make efficient use of the device resources. In addition, you can manually control resource usage by setting location assignments. Any six-input function can be implemented utilizing inputs dataa, datab, datac, datad, and either datae0 and dataf0 or datae1 and dataf1. If datae0 and dataf0 are utilized, the output is driven to register0, and/or register0 is bypassed and the data drives out to the interconnect using the top set of output drivers (see Figure 2–39). If datae1 and dataf1 are utilized, the output drives to register1 and/or bypasses register1 and drives to the interconnect

The RAM blocks in Stratix II GX devices have local interconnects to allow ALMs and interconnects to drive into RAM blocks. The M512 RAM block local interconnect is driven by the R4, C4, and direct link interconnects from adjacent LABs. The M512 RAM blocks can communicate with LABs on either the left or right side through these row interconnects or with LAB columns on the left or right side with the column interconnects. The M512 RAM block has up to 16 direct link input connections from the left adjacent LABs and another 16 from the right adjacent LAB. M512 RAM outputs can also connect to left and right LABs through direct link interconnect. The M512 RAM block has equal opportunity for access and performance to and from LABs on either its left or right side. Figure 2–50 shows the M512 RAM block to logic array interface.

Figure 2–50. M512 RAM Block LAB Row Interface

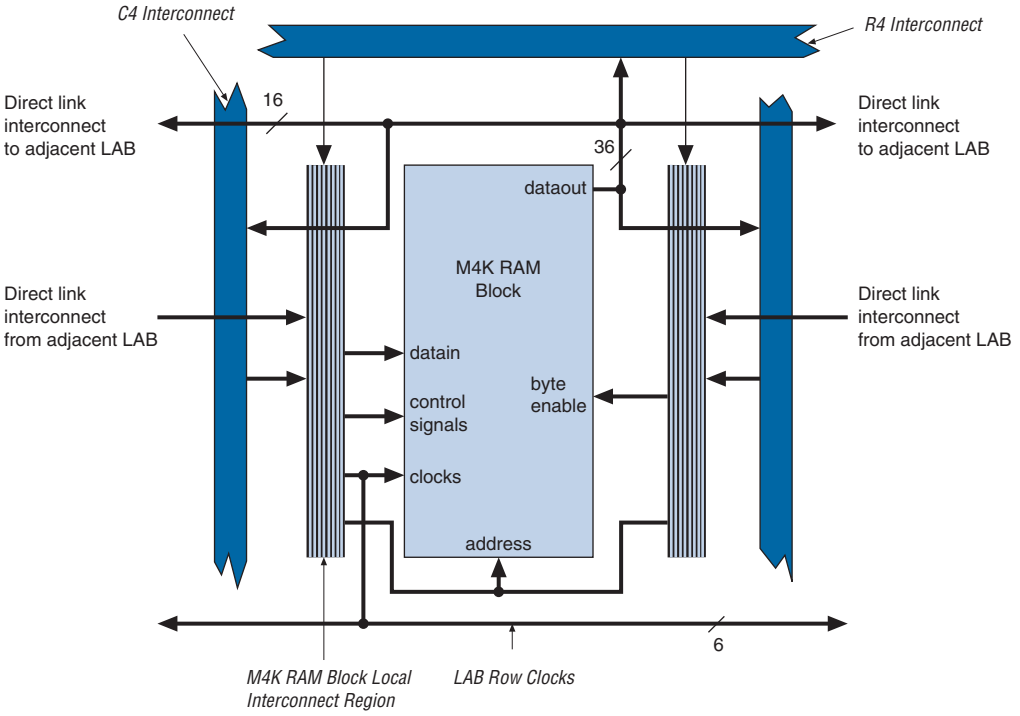
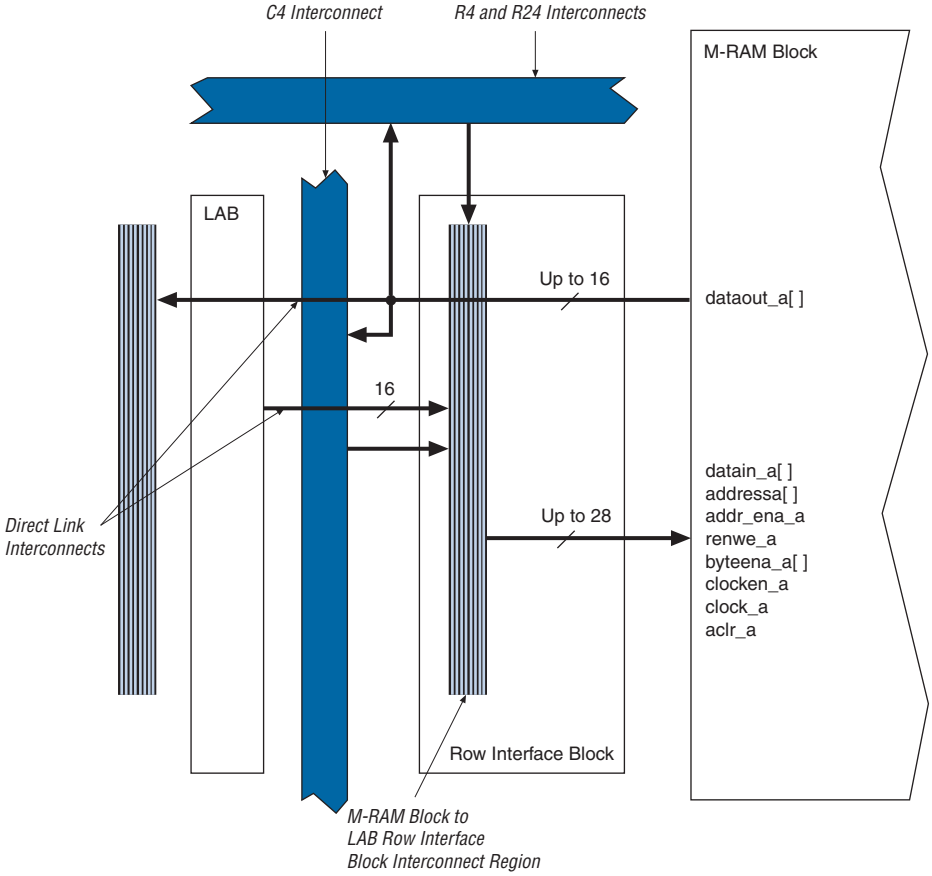


Figure 2–56. M-RAM Row Unit Interface to Interconnect

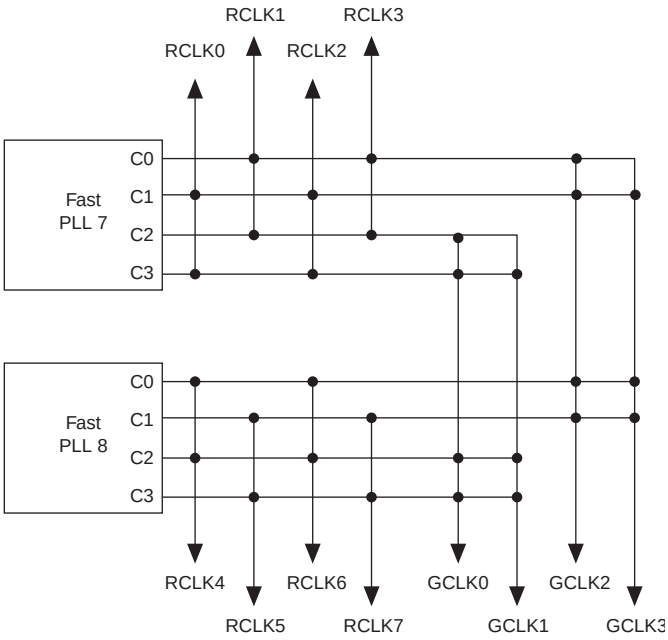


The Stratix II GX clock networks can be disabled (powered down) by both static and dynamic approaches. When a clock net is powered down, all the logic fed by the clock net is in an off-state, thereby reducing the overall power consumption of the device. The global and regional clock networks can be powered down statically through a setting in the configuration file (**.sof** or **.pof**). Clock networks that are not used are automatically powered down through configuration bit settings in the configuration file generated by the Quartus II software. The dynamic clock enable and disable feature allows the internal logic to control power up and down synchronously on GCLK and RCLK nets and PLL_OUT pins. This function is independent of the PLL and is applied directly on the clock network or PLL_OUT pin, as shown in Figures 2–67 through 2–69.

Enhanced and Fast PLLs

Stratix II GX devices provide robust clock management and synthesis using up to four enhanced PLLs and four fast PLLs. These PLLs increase performance and provide advanced clock interfacing and clock frequency synthesis. With features such as clock switchover, spread spectrum clocking, reconfigurable bandwidth, phase control, and reconfigurable phase shifting, the Stratix II GX device's enhanced PLLs provide you with complete control of clocks and system timing. The fast PLLs provide general purpose clocking with multiplication and phase shifting as well as high-speed outputs for high-speed differential I/O support. Enhanced and fast PLLs work together with the Stratix II GX high-speed I/O and advanced clock architecture to provide significant improvements in system performance and bandwidth.

Figure 2–72. Global and Regional Clock Connections from Corner Clock Pins and Fast PLL Outputs Notes (1), (2)



Notes to Figure 2–72:

(1) The global or regional clocks in a fast PLL's quadrant can drive the fast PLL input. A dedicated clock input pin or other PLL must drive the global or regional source. The source cannot be driven by internally generated logic before driving the fast PLL.

(2) EP2SGX30C/D and EP2SGX60C/D devices only have two fast PLLs (1 and 2); they do not contain corner fast PLLs.

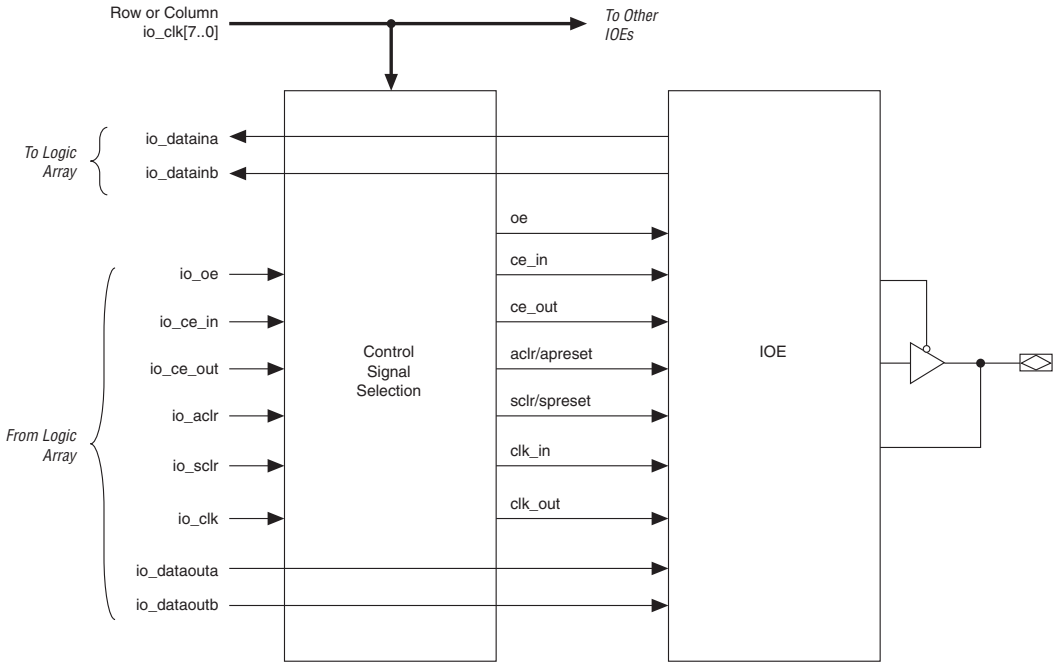
Table 2–27. Global and Regional Clock Connections from Left Side Clock Pins and Fast PLL Outputs (Part 1 of 3)

Left Side Global and Regional Clock Network Connectivity	CLK0	CLK1	CLK2	CLK3	RCLK0	RCLK1	RCLK2	RCLK3	RCLK4	RCLK5	RCLK6	RCLK7
Clock pins												
CLK0p	✓	✓			✓				✓			
CLK1p	✓	✓				✓				✓		
CLK2p			✓	✓			✓				✓	
CLK3p			✓	✓				✓				✓

There are 32 control and data signals that feed each row or column I/O block. These control and data signals are driven from the logic array. The row or column IOE clocks, `io_clk[7..0]`, provide a dedicated routing resource for low-skew, high-speed clocks. I/O clocks are generated from global or regional clocks. Refer to "PLLs and Clock Networks" on page 2–89 for more information.

Figure 2–79 illustrates the signal paths through the I/O block.

Figure 2–79. Signal Path Through the I/O Block



Each IOE contains its own control signal selection for the following control signals: `oe`, `ce_in`, `ce_out`, `aclr/apreset`, `sclr/spreset`, `clk_in`, and `clk_out`. Figure 2–80 illustrates the control signal selection.

considerable flexibility for frequency synthesis, allowing real-time variation of the PLL frequency and delay. The rest of the device is functional while reconfiguring the PLL.

See the *PLLs in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook* for more information on Stratix II GX PLLs.

Temperature Sensing Diode (TSD)

Stratix II GX devices include a diode-connected transistor for use as a temperature sensor in power management. This diode is used with an external digital thermometer device. These devices steer bias current through the Stratix II GX diode, measuring forward voltage and converting this reading to temperature in the form of an 8-bit signed number (7 bits plus 1 sign bit). The external device's output represents the junction temperature of the Stratix II GX device and can be used for intelligent power management.

The diode requires two pins (`tempdiodep` and `tempdioden`) on the Stratix II GX device to connect to the external temperature-sensing device, as shown in Figure 3–1. The temperature sensing diode is a passive element and therefore can be used before the Stratix II GX device is powered.

Figure 3–1. External Temperature-Sensing Diode

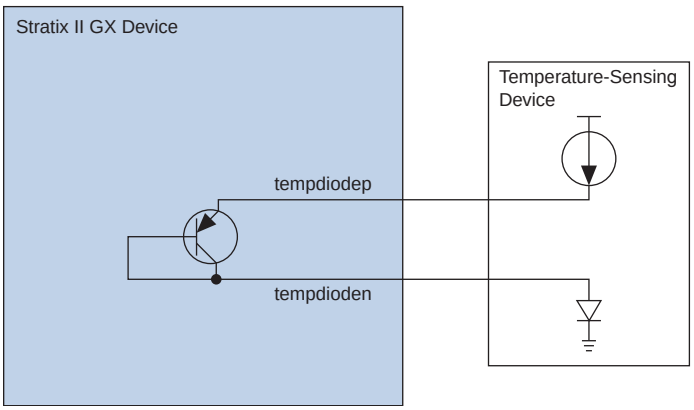


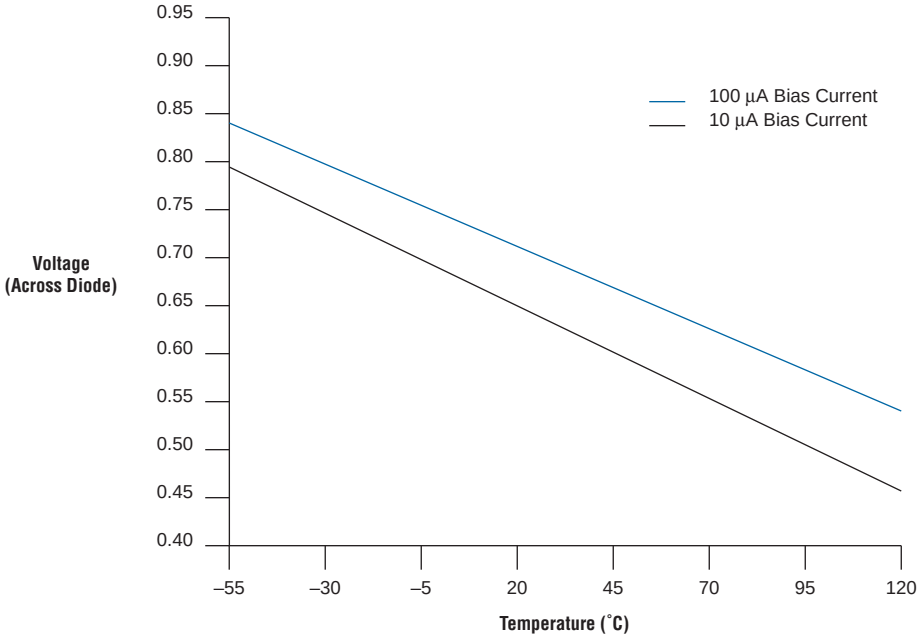
Table 3–5 shows the specifications for bias voltage and current of the Stratix II GX temperature sensing diode.

Table 3–5. Temperature-Sensing Diode Electrical Characteristics

Parameter	Minimum	Typical	Maximum	Unit
IBIAS high	80	100	120	µA
IBIAS low	8	10	12	µA
VBP - VBN	0.3		0.9	V
VBN		0.7		V
Series resistance			3	Ω

The temperature-sensing diode works for the entire operating range shown in Figure 3–2.

Figure 3–2. Temperature Versus Temperature-Sensing Diode Voltage



The temperature sensing diode is a very sensitive circuit which can be influenced by noise coupled from other traces on the board, and possibly within the device package itself, depending on device usage. The interfacing device registers temperature based on millivolts of difference as seen at the TSD. Switching I/O near the TSD pins can affect the temperature reading. Altera recommends you take temperature readings during periods of no activity in the device (for example, standby mode where no clocks are toggling in the device), such as when the nearby I/Os are at a DC state, and disable clock networks in the device.

Automated Single Event Upset (SEU) Detection

Stratix II GX devices offer on-chip circuitry for automated checking of single event upset (SEU) detection. Some applications that require the device to operate error free at high elevations or in close proximity to Earth's North or South Pole will require periodic checks to ensure continued data integrity. The error detection cyclic redundancy check (CRC) feature controlled by the **Device & Pin Options** dialog box in the Quartus II software uses a 32-bit CRC circuit to ensure data reliability and is one of the best options for mitigating SEU.

You can implement the error detection CRC feature with existing circuitry in Stratix II GX devices, eliminating the need for external logic. Stratix II GX devices compute CRC during configuration and checks the computed-CRC against an automatically computed CRC during normal operation. The `CRC_ERROR` pin reports a soft error when configuration SRAM data is corrupted, triggering device reconfiguration.

Custom-Built Circuitry

Dedicated circuitry is built into Stratix II GX devices to automatically perform error detection. This circuitry constantly checks for errors in the configuration SRAM cells while the device is in user mode. You can monitor one external pin for the error and use it to trigger a reconfiguration cycle. You can select the desired time between checks by adjusting a built-in clock divider.

Software Interface

Beginning with version 4.1 of the Quartus II software, you can turn on the automated error detection CRC feature in the **Device & Pin Options** dialog box. This dialog box allows you to enable the feature and set the internal frequency of the CRC between 400 kHz to 50 MHz. This controls the rate that the CRC circuitry verifies the internal configuration SRAM bits in the Stratix II GX FPGA.

For more information on CRC, refer to *AN 357: Error Detection Using CRC in Altera FPGA Devices*.

Table 4–6. Stratix II GX Transceiver Block AC Specification (Part 3 of 6)

Symbol / Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
reconfig_clk clock frequency		2.5	-	50	2.5	-	50	2.5	-	50	MHz
Transceiver block minimum power-down pulse width		100	-	-	100	-	-	100	-	-	ns
Receiver											
Data rate		600	-	6375	600	-	5000	600	-	4250	Mbps
Absolute V_{MAX} for a receiver pin *(1)*		-	-	2.0	-	-	2.0	-	-	2.0	V
Absolute V_{MIN} for a receiver pin		-0.4	-	-	-0.4	-	-	-0.4	-	-	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p)	V_{CM} = 0.85 V	-	-	3.3	-	-	3.3	-	-	3.3	V
Minimum peak-to-peak differential input voltage V_{ID} (diff p-p)	V_{CM} = 0.85 V DC Gain = ≥ 3 dB	160	-	-	160	-	-	160	-	-	mV
V_{ICM}	V_{ICM} = 0.85 V setting	850±10%			850±10%			850±10%			mV
	V_{ICM} = 1.2 V setting *(11)*	1200±10%			1200±10%			1200±10%			mV
On-chip termination resistors	100 Ω setting	100±15%			100±15%			100±15%			Ω
	120 Ω setting	120±15%			120±15%			120±15%			Ω
	150 Ω setting	150±15%			150±15%			150±15%			Ω
Bandwidth at 6.375 Gbps	BW = Low	-	20	-	-	-	-	-	-	-	MHz
	BW = Med	-	35	-	-	-	-	-	-	-	MHz
	BW = High	-	45	-	-	-	-	-	-	-	MHz

Table 4–27. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO} *(1)*	Output supply voltage		1.71	1.89	V
V_{IH}	High-level input voltage		0.65 × V_{CCIO}	2.25	V
V_{IL}	Low-level input voltage		–0.3	0.35 × V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OH} = –2 mA *(2)*	V_{CCIO} – 0.45		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA *(2)*		0.45	V

Notes to Table 4–27:

(1) The Stratix II GX device V_{CCIO} voltage level support of 1.8 to 5% is narrower than defined in the Normal Range of the EIA/JEDEC standard.

(2) This specification is supported across all the programmable drive settings available for this I/O standard as shown in *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Table 4–28. 1.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO} *(1)*	Output supply voltage		1.425	1.575	V
V_{IH}	High-level input voltage		0.65 V_{CCIO}	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.35 V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OH} = –2 mA *(2)*	0.75 V_{CCIO}		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA *(2)*		0.25 V_{CCIO}	V

Notes to Table 4–28:

(1) The Stratix II GX device V_{CCIO} voltage level support of 1.5 to 5% is narrower than defined in the Normal Range of the EIA/JEDEC standard.

(2) This specification is supported across all the programmable drive settings available for this I/O standard as shown in *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Table 4–58. DSP Block Internal Timing Microparameters (Part 2 of 2)

Symbol	Parameter	-3 Speed Grade (1)		-3 Speed Grade (2)		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{INREG2PIPE9}$	Input register to DSP block pipeline register in 9 × 9-bit mode	1312	2030	1312	2131	1312	2266	1312	2720	ps
$t_{INREG2PIPE18}$	Input register to DSP block pipeline register in 18 × 18-bit mode	1302	2010	1302	2110	1302	2244	1302	2693	ps
$t_{INREG2PIPE36}$	Input register to DSP block pipeline register in 36 × 36-bit mode	1302	2010	1302	2110	1302	2244	1302	2693	ps
$t_{PIPE2OUTREG2ADD}$	DSP block pipeline register to output register delay in two-multipliers adder mode	924	1450	924	1522	924	1618	924	1943	ps
$t_{PIPE2OUTREG4ADD}$	DSP block pipeline register to output register delay in four-multipliers adder mode	1134	1850	1134	1942	1134	2065	1134	2479	ps
t_{PD9}	Combinational input to output delay for 9 × 9	2100	2880	2100	3024	2100	3214	2100	3859	ps
t_{PD18}	Combinational input to output delay for 18 × 18	2110	2990	2110	3139	2110	3337	2110	4006	ps
t_{PD36}	Combinational input to output delay for 36 × 36	2939	4450	2939	4672	2939	4967	2939	5962	ps
t_{CLR}	Minimum clear pulse width	2212		2322		2469		2964		ps
t_{CLKL}	Minimum clock low time	1190		1249		1328		1594		ps
t_{CLKH}	Minimum clock high time	1190		1249		1328		1594		ps

(1) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
(2) This column refers to –3 speed grades for EP2SGX130 devices.

Table 4–60. M4K Block Internal Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	-3 Speed Grade *(2)*		-3 Speed Grade *(3)*		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{M4KDATABH}$	B port data hold time after clock	203		213		226		272		ps
$t_{M4KRADDRBSU}$	B port address setup time before clock	22		23		24		29		ps
$t_{M4KRADDRBH}$	B port address hold time after clock	203		213		226		272		ps
$t_{M4KDATACO1}$	Clock-to-output delay when using output registers	334	524	334	549	334	584	334	701	ps
$t_{M4KDATACO2}$	Clock-to-output delay without output registers	1616	2453	1616	2574	1616	2737	1616	3286	ps
$t_{M4KCLKH}$	Minimum clock high time	1250		1312		1395		1675		ps
$t_{M4KCLKL}$	Minimum clock low time	1250		1312		1395		1675		ps
t_{M4KCLR}	Minimum clear pulse width	144		151		160		192		ps

(1) The M512 block f_{MAX} obtained using the Quartus II software does not necessarily equal to 1/TM4KRC.
(2) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
(3) This column refers to –3 speed grades for EP2SGX130 devices.

Table 4–61. M-RAM Block Internal Timing Microparameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	-3 Speed Grade *(2)*		-3 Speed Grade *(3)*		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{MEGARC}	Synchronous read cycle time	1866	2774	1866	2911	1866	3096	1866	3716	ps
$t_{MEGAWERESU}$	Write or read enable setup time before clock	144		151		160		192		ps
$t_{MEGAWEREH}$	Write or read enable hold time after clock	39		40		43		52		ps

Table 4–77. EP2SGX130 Column Pins Regional Clock Timing Parameters

Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.815	1.834	3.218	3.417	4.087	ns
t_{COUT}	1.650	1.669	3.218	3.417	4.087	ns
t_{PLLCIN}	0.116	0.134	0.349	0.364	0.426	ns
$t_{PLLCOUT}$	-0.049	-0.031	0.361	0.378	0.444	ns

Table 4–78. EP2SGX130 Row Pins Regional Clock Timing Parameters

Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.544	1.560	3.195	3.395	4.060	ns
t_{COUT}	1.549	1.565	3.195	3.395	4.060	ns
t_{PLLCIN}	-0.149	-0.132	0.34	0.356	0.417	ns
$t_{PLLCOUT}$	-0.144	-0.127	0.342	0.356	0.417	ns

Clock Network Skew Adders

The Quartus II software models skew within dedicated clock networks such as global and regional clocks. Therefore, the intra-clock network skew adder is not specified. Table 4–79 specifies the intra-clock skew between any two clock networks driving any registers in the Stratix II GX device.

Table 4–79. Clock Network Specifications (Part 1 of 2)

Name	Description	Min	Typ	Max	Unit
Clock skew adder EP2SGX30 *(1)*	Inter-clock network, same side			±50	ps
	Inter-clock network, entire chip			±100	ps
Clock skew adder EP2SGX60 *(1)*	Inter-clock network, same side			±50	ps
	Inter-clock network, entire chip			±100	ps
Clock skew adder EP2SGX90 *(1)*	Inter-clock network, same side			±55	ps
	Inter-clock network, entire chip			±110	ps

Table 4–85. Stratix II GX I/O Input Delay for Row Pins (Part 3 of 3)

I/O Standard	Parameter	Fast Corner Industrial/ Commercial	-3 Speed Grade *(2)*	-3 Speed Grade *(3)*	-4 Speed Grade	-5 Speed Grade	Unit
Differential SSTL-18 Class I	t_{PI}	605	960	1006	1070	1285	ps
	t_{PCOUT}	266	433	454	483	580	ps
Differential SSTL-18 Class II	t_{PI}	605	960	1006	1070	1285	ps
	t_{PCOUT}	266	433	454	483	580	ps
1.8-V differential HSTL Class I	t_{PI}	605	960	1006	1070	1285	ps
	t_{PCOUT}	266	433	454	483	580	ps
1.8-V differential HSTL Class II	t_{PI}	605	960	1006	1070	1285	ps
	t_{PCOUT}	266	433	454	483	580	ps
1.5-V differential HSTL Class I	t_{PI}	631	1056	1107	1177	1413	ps
	t_{PCOUT}	292	529	555	590	708	ps
1.5-V differential HSTL Class II	t_{PI}	631	1056	1107	1177	1413	ps
	t_{PCOUT}	292	529	555	590	708	ps

(1) The parameters are only available on the left side of the device.
(2) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
(3) This column refers to –3 speed grades for EP2SGX130 devices.

Table 4–115. DQS Bus Clock Skew Adder Specifications (t_{DQS}_CLOCK_SKEW_ADDER)	
Mode	**DQS Clock Skew Adder (ps)** *(1)*
4 DQ per DQS	40
9 DQ per DQS	70
18 DQ per DQS	75
36 DQ per DQS	95

(1) This skew specification is the absolute maximum and minimum skew. For example, skew on a 40 DQ group is 40 ps or 20 ps.

Table 4–116. DQS Phase Offset Delay Per Stage (ps) *Notes (1), (2), (3)*				
Speed Grade	**Positive Offset**		**Negative Offset**	
	Min	**Max**	**Min**	**Max**
-3	10	15	8	11
-4	10	15	8	11
-5	10	16	8	12

(1) The delay settings are linear.
(2) The valid settings for phase offset are -32 to +31.
(3) The typical value equals the average of the minimum and maximum values.

JTAG Timing Specifications

Figure 4–14 shows the timing requirements for the JTAG signals