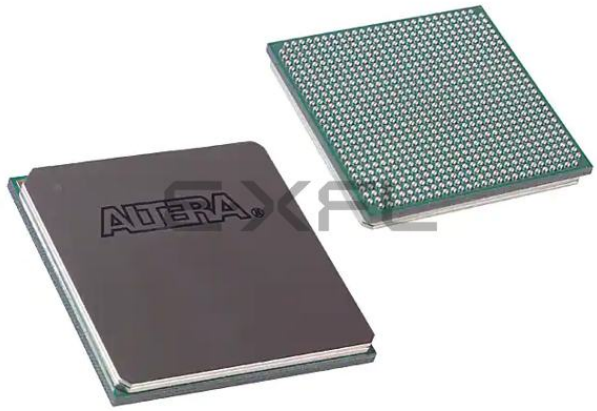

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3022
Number of Logic Elements/Cells	60440
Total RAM Bits	2544192
Number of I/O	364
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	780-BBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2sgx60df780c4

1. Introduction

SIIGX51001-1.6

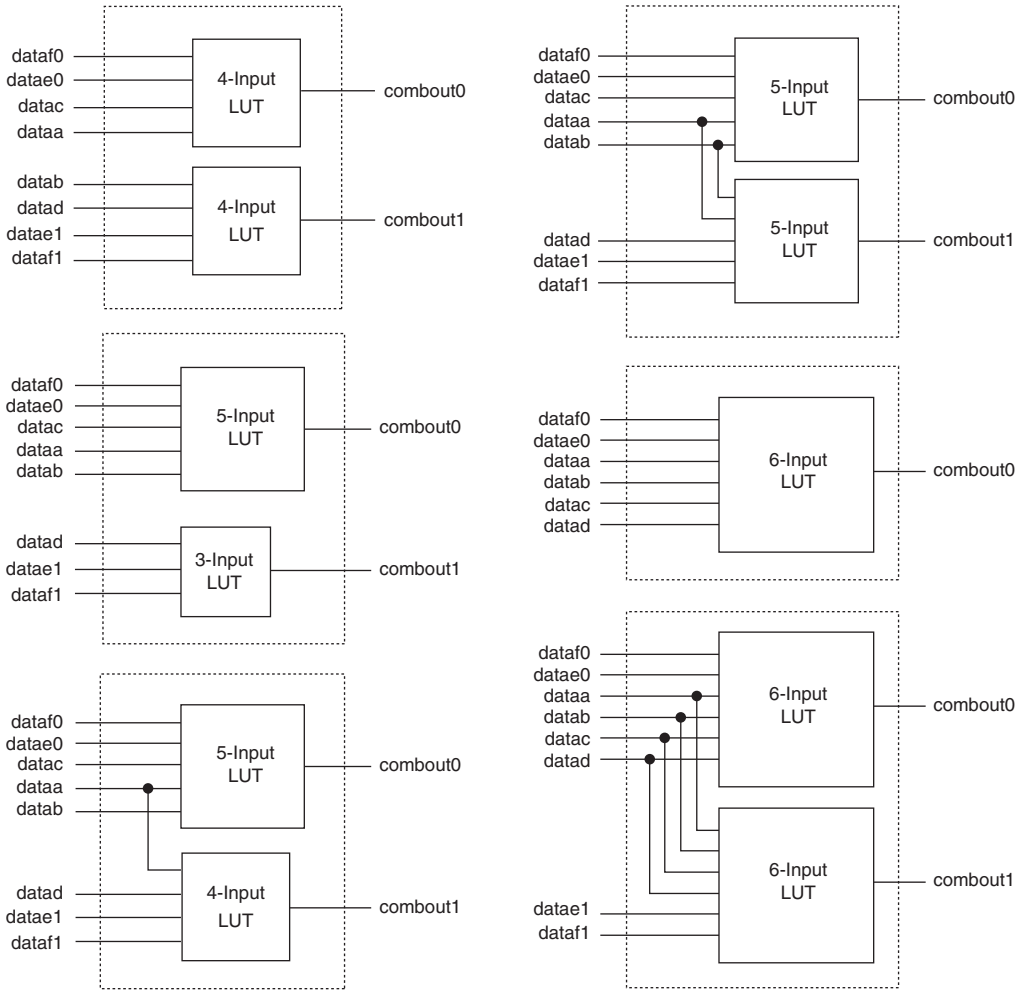
The Stratix® II GX family of devices is Altera's third generation of FPGAs to combine high-speed serial transceivers with a scalable, high-performance logic array. Stratix II GX devices include 4 to 20 high-speed transceiver channels, each incorporating clock and data recovery unit (CRU) technology and embedded SERDES capability at data rates of up to 6.375 gigabits per second (Gbps). The transceivers are grouped into four-channel transceiver blocks and are designed for low power consumption and small die size. The Stratix II GX FPGA technology is built upon the Stratix II architecture and offers a 1.2-V logic array with unmatched performance, flexibility, and time-to-market capabilities. This scalable, high-performance architecture makes Stratix II GX devices ideal for high-speed backplane interface, chip-to-chip, and communications protocol-bridging applications.

Features

This section lists the Stratix II GX device features.

- Main device features:
  - TriMatrix memory consisting of three RAM block sizes to implement true dual-port memory and first-in first-out (FIFO) buffers with performance up to 550 MHz
  - Up to 16 global clock networks with up to 32 regional clock networks per device region
  - High-speed DSP blocks provide dedicated implementation of multipliers (at up to 450 MHz), multiply-accumulate functions, and finite impulse response (FIR) filters
  - Up to four enhanced PLLs per device provide spread spectrum, programmable bandwidth, clock switch-over, real-time PLL reconfiguration, and advanced multiplication and phase shifting
  - Support for numerous single-ended and differential I/O standards
  - High-speed source-synchronous differential I/O support on up to 71 channels
  - Support for source-synchronous bus standards, including SPI-4 Phase 2 (POS-PHY Level 4), SFI-4.1, XSBI, UTOPIA IV, NPSI, and CSIX-L1
  - Support for high-speed external memory, including quad data rate (QDR and QDRII) SRAM, double data rate (DDR and DDR2) SDRAM, and single data rate (SDR) SDRAM

Figure 2–37. ALM in Normal Mode *Note (1)*



Note to Figure 2–37:

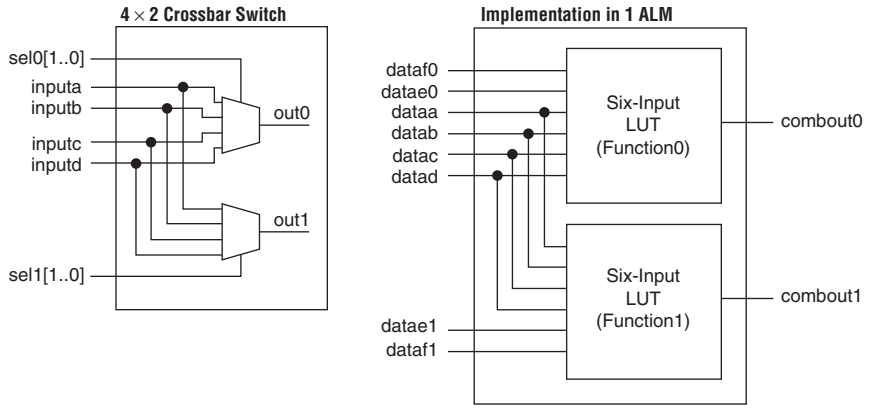
(1) Combinations of functions with less inputs than those shown are also supported. For example, combinations of functions with the following number of inputs are supported: 4 and 3, 3 and 3, 3 and 2, 5 and 2, etc.

The normal mode provides complete backward compatibility with four-input LUT architectures. Two independent functions of four inputs or less can be implemented in one Stratix II GX ALM. In addition, a five-input function and an independent three-input function can be implemented without sharing inputs.

To pack two five-input functions into one ALM, the functions must have at least two common inputs. The common inputs are dataa and datab. The combination of a four-input function with a five-input function requires one common input (either dataa or datab).

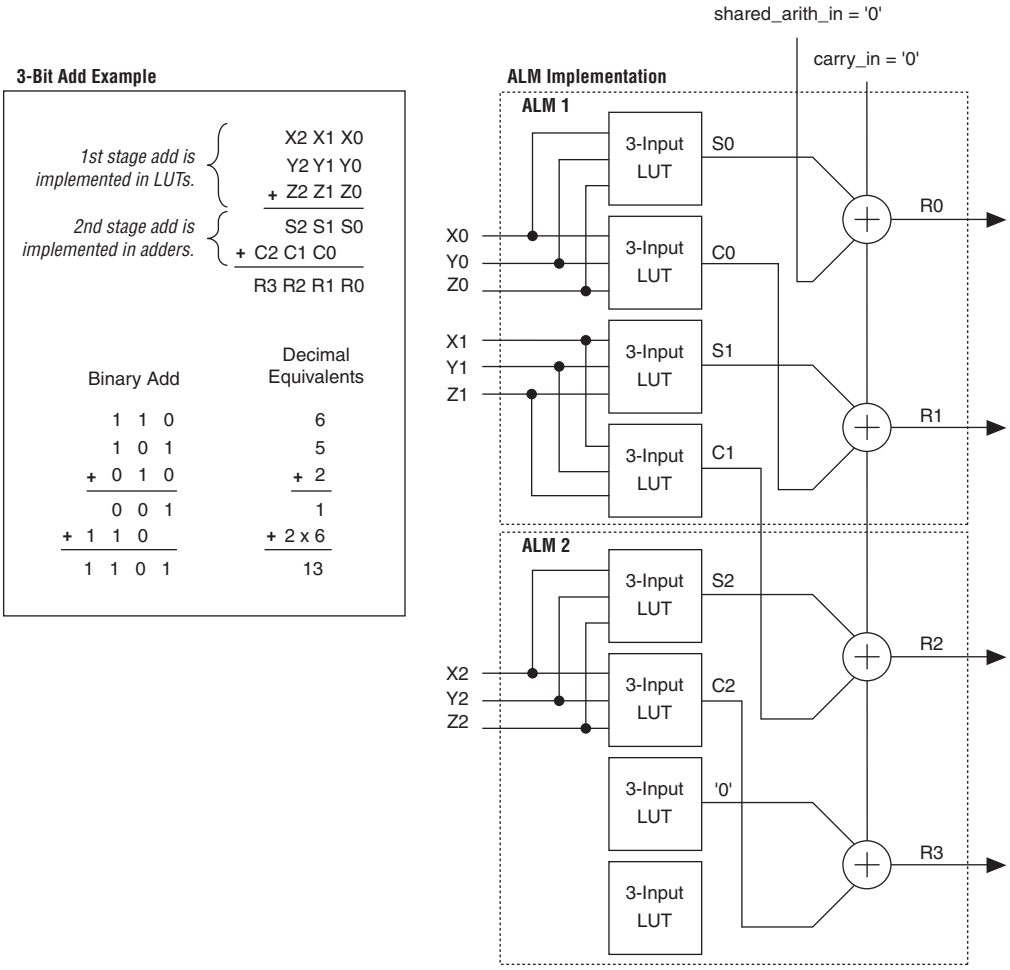
To implement two six-input functions in one ALM, four inputs must be shared and the combinational function must be the same. For example, a 4 × 2 crossbar switch (two 4-to-1 multiplexers with common inputs and unique select lines) can be implemented in one ALM, as shown in Figure 2–38. The shared inputs are dataa, datab, datac, and datad, while the unique select lines are datae0 and dataf0 for function0, and datae1 and dataf1 for function1. This crossbar switch consumes four LUTs in a four-input LUT-based architecture.

Figure 2–38. 4 × 2 Crossbar Switch Example



In a sparsely used device, functions that could be placed into one ALM can be implemented in separate ALMs. The Quartus II Compiler spreads a design out to achieve the best possible performance. As a device begins to fill up, the Quartus II software automatically utilizes the full potential of the Stratix II GX ALM. The Quartus II Compiler automatically searches for functions of common inputs or completely independent functions to be placed into one ALM and to make efficient use of the device resources. In addition, you can manually control resource usage by setting location assignments. Any six-input function can be implemented utilizing inputs dataa, datab, datac, datad, and either datae0 and dataf0 or datae1 and dataf1. If datae0 and dataf0 are utilized, the output is driven to register0, and/or register0 is bypassed and the data drives out to the interconnect using the top set of output drivers (see Figure 2–39). If datae1 and dataf1 are utilized, the output drives to register1 and/or bypasses register1 and drives to the interconnect

Figure 2–44. Example of a 3-Bit Add Utilizing Shared Arithmetic Mode



Shared Arithmetic Chain

In addition to the dedicated carry chain routing, the shared arithmetic chain available in shared arithmetic mode allows the ALM to implement a three-input add, which significantly reduces the resources necessary to implement large adder trees or correlator functions. The shared arithmetic chains can begin in either the first or fifth ALM in a LAB. The Quartus II Compiler automatically links LABs to create shared arithmetic chains longer than 16 (8 ALMs in arithmetic or shared arithmetic mode). For enhanced fitting, a long shared arithmetic chain runs vertically

The connections to the global and regional clocks from the top clock pins and enhanced PLL outputs are shown in Table 2–28. The connections to the clocks from the bottom clock pins are shown in Table 2–29.

Table 2–28. Global and Regional Clock Connections from Top Clock Pins and Enhanced PLL Outputs (Part 1 of 2)

Top Side Global and Regional Clock Network Connectivity	DLLCLK	CLK12	CLK13	CLK14	CLK15	RCLK24	RCLK25	RCLK26	RCLK27	RCLK28	RCLK29	RCLK30	RCLK31
Clock pins													
CLK12p	✓	✓	✓			✓				✓			
CLK13p	✓	✓	✓				✓				✓		
CLK14p	✓			✓	✓			✓				✓	
CLK15p	✓			✓	✓				✓				✓
CLK12n		✓				✓				✓			
CLK13n			✓				✓				✓		
CLK14n				✓				✓				✓	
CLK15n					✓				✓				✓
Drivers from internal logic													
GCLKDRV0		✓											
GCLKDRV1			✓										
GCLKDRV2				✓									
GCLKDRV3					✓								
RCLKDRV0						✓				✓			
RCLKDRV1							✓				✓		
RCLKDRV2								✓				✓	
RCLKDRV3									✓				✓
RCLKDRV4						✓				✓			
RCLKDRV5							✓				✓		
RCLKDRV6								✓				✓	
RCLKDRV7									✓				✓
Enhanced PLL5 outputs													
c0	✓	✓	✓			✓				✓			
c1	✓	✓	✓				✓				✓		

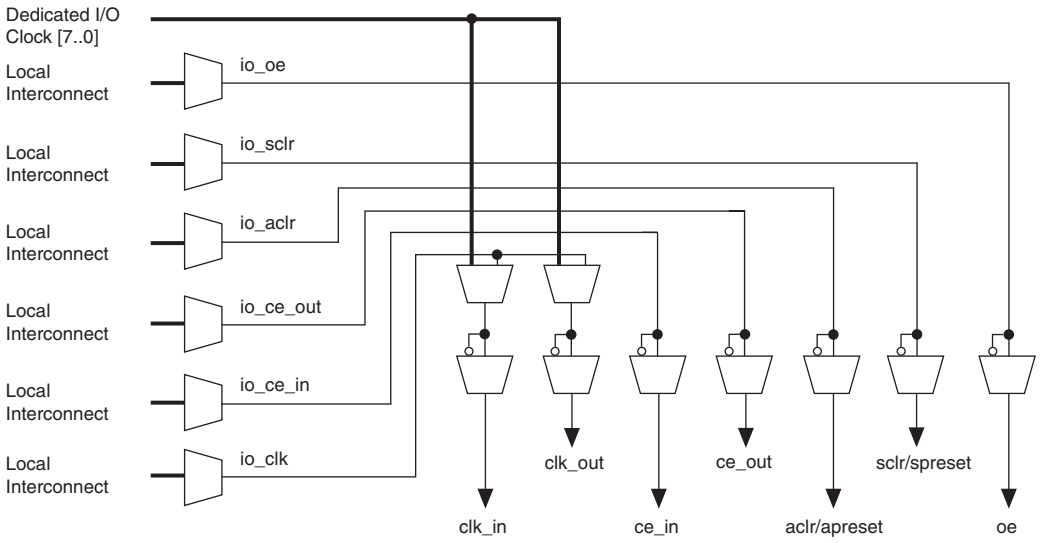
Table 2–28. Global and Regional Clock Connections from Top Clock Pins and Enhanced PLL Outputs (Part 2 of 2)

Top Side Global and Regional Clock Network Connectivity	DLLCLK	CLK12	CLK13	CLK14	CLK15	RCLK24	RCLK25	RCLK26	RCLK27	RCLK28	RCLK29	RCLK30	RCLK31
c2	✓			✓	✓			✓				✓	
c3	✓			✓	✓				✓				✓
c4	✓					✓		✓		✓		✓	
c5	✓						✓		✓		✓		✓
Enhanced PLL 11 outputs													
c0		✓	✓			✓				✓			
c1		✓	✓				✓				✓		
c2				✓	✓			✓				✓	
c3				✓	✓				✓				✓
c4						✓		✓		✓		✓	
c5							✓		✓		✓		✓

Table 2–29. Global and Regional Clock Connections from Bottom Clock Pins and Enhanced PLL Outputs (Part 1 of 2)

Bottom Side Global and Regional Clock Network Connectivity	DLLCLK	CLK4	CLK5	CLK6	CLK7	RCLK8	RCLK9	RCLK10	RCLK11	RCLK12	RCLK13	RCLK14	RCLK15
Clock pins													
CLK4p	✓	✓	✓			✓				✓			
CLK5p	✓	✓	✓				✓				✓		
CLK6p	✓			✓	✓			✓				✓	
CLK7p	✓			✓	✓				✓				✓
CLK4n		✓				✓				✓			
CLK5n			✓				✓				✓		
CLK6n				✓				✓				✓	
CLK7n					✓				✓				✓
Drivers from internal logic													
GCLKDRV0		✓											
GCLKDRV1			✓										

Figure 2–80. Control Signal Selection per IOE *Note (1)*



Note to Figure 2–80:

(1) Control signals `ce_in`, `ce_out`, `aclr/apreset`, `sclr/spreset`, and `oe` can be global signals even though their control selection multiplexers are not directly fed by the `ioe_clk[7..0]` signals. The `ioe_clk` signals can drive the I/O local interconnect, which then drives the control selection multiplexers.

In normal bidirectional operation, you can use the input register for input data requiring fast setup times. The input register can have its own clock input and clock enable separate from the OE and output registers. The output register can be used for data requiring fast clock-to-output performance. You can use the OE register for fast clock-to-output enable timing. The OE and output register share the same clock source and the same clock enable source from local interconnect in the associated LAB, dedicated I/O clocks, and the column and row interconnects. Figure 2–81 shows the IOE in bidirectional configuration.

The bus-hold circuitry also pulls undriven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. You can select this feature individually for each I/O pin. The bus-hold output drives no higher than V_{CCIO} to prevent overdriving signals. If the bus-hold feature is enabled, the programmable pull-up option cannot be used. Disable the bus-hold feature when the I/O pin has been configured for differential signals.

The bus-hold circuitry uses a resistor with a nominal resistance (RBH) of approximately 7 kΩ to pull the signal level to the last-driven state.

Refer to the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II GX Device Handbook* for the specific sustaining current driven through this resistor and overdrive current used to identify the next-driven input level. This information is provided for each V_{CCIO} voltage level.

The bus-hold circuitry is active only after configuration. When going into user mode, the bus-hold circuit captures the value on the pin present at the end of configuration.

Programmable Pull-Up Resistor

Each Stratix II GX device I/O pin provides an optional programmable pull-up resistor during user mode. If you enable this feature for an I/O pin, the pull-up resistor (typically 25 kΩ) holds the output to the V_{CCIO} level of the output pin's bank.

Programmable pull-up resistors are only supported on user I/O pins and are not supported on dedicated configuration pins, JTAG pins, or dedicated clock pins.

Advanced I/O Standard Support

The Stratix II GX device IOEs support the following I/O standards:

- 3.3-V LVTTL/LVCMOS
- 2.5-V LVTTL/LVCMOS
- 1.8-V LVTTL/LVCMOS
- 1.5-V LVCMOS
- 3.3-V PCI
- 3.3-V PCI-X mode 1
- LVDS
- LVPECL (on input and output clocks only)
- Differential 1.5-V HSTL class I and II
- Differential 1.8-V HSTL class I and II
- Differential SSTL-18 class I and II

Table 2–42. Document Revision History (Part 2 of 6)

Date and Document Version	Changes Made	Summary of Changes
February 2007 v2.0	Added Chapter 02 “Stratix II GX Transceivers” to the beginning of Chapter 03 “Stratix II GX Architecture”. • Changed chapter number to Chapter 02.	Combined Chapter 02 “Stratix II GX Transceivers” and Chapter 03 “Stratix II GX Architecture” in the new Chapter 02 “Stratix II GX Architecture”
	Added the “Document Revision History” section to this chapter.	
	Moved the “Stratix II GX Transceiver Clocking” section to after the “Receiver Path” section.	

Table 2–42. Document Revision History (Part 5 of 6)

Date and Document Version	Changes Made	Summary of Changes
Previous Chapter 02 changes: June 2006, v1.2	• Updated notes 1 and 2 in Figure 2–1. • Updated "Byte Serializer" section. • Updated Tables 2–4, 2–7, and 2–16. • Updated "Programmable Output Driver" section. • Updated Figure 2–12. • Updated "Programmable Pre-Emphasis" section. • Added Table 2–11. • Added "Dynamic Reconfiguration" section. • Added "Calibration Block" section. • Updated "Programmable Equalizer" section, including addition of Figure 2–18.	Updated input frequency range in Table 2–4.
Previous Chapter 02 changes: April 2006, v1.1	• Updated Figure 2–3. • Updated Figure 2–7. • Updated Table 2–4. • Updated "Transmit Buffer" section.	Updated input frequency range in Table 2–4.
Previous Chapter 02 changes: October 2005 v1.0	Added chapter to the *Stratix II GX Device Handbook*.	
Previous Chapter 03 changes: August 2006, v1.4	• Updated Table 3–18 with note.	
Previous Chapter 03 changes: June 2006, v1.3	• Updated note 2 in Figure 3–41. • Updated column title in Table 3–21.	
Previous Chapter 03 changes: April 2006, v1.2	• Updated note 1 in Table 3–9. • Updated note 1 in Figure 3–40. • Updated note 2 in Figure 3–41. • Updated Table 3–16. • Updated Figure 3–56. • Updated Tables 3–19 through 3–22. • Updated Tables 3–25 and 3–26. • Updated "Fast PLL & Channel Layout" section.	Added 1,152-pin FineLine BGA package information for EP2SGX60 device in Table 3–16.

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 4 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Sinusoidal jitter FC-1	Fc/25000	> 1.5			> 1.5			> 1.5			UI
	Fc/1667	> 0.1			> 0.1			> 0.1			UI
Deterministic jitter FC-2	Pattern = CJTPAT No Equalization DC Gain = 0 dB	> 0.33			> 0.33			> 0.33			UI
Random jitter FC-2	Pattern = CJTPAT No Equalization DC Gain = 0 dB	> 0.29			> 0.29			> 0.29			UI
Sinusoidal jitter FC-2	Fc/25000	> 1.5			> 1.5			> 1.5			UI
	Fc/1667	> 0.1			> 0.1			> 0.1			UI
Deterministic jitter FC-4	Pattern = CJTPAT No Equalization DC Gain = 0 dB	> 0.33			> 0.33			> 0.33			UI
Random jitter FC-4	Pattern = CJTPAT No Equalization DC Gain = 0 dB	> 0.29			> 0.29			> 0.29			UI
Sinusoidal jitter FC-4	Fc/25000	> 1.5			> 1.5			> 1.5			UI
	Fc/1667	> 0.1			> 0.1			> 0.1			UI
XAUI Transmit Jitter Generation *(9)*											
Total jitter at 3.125 Gbps	REFCLK = 156.25 MHz Pattern = CJPAT V_{OD} = 1200 mV No Pre-emphasis	-	-	0.3	-	-	0.3	-	-	0.3	UI
Deterministic jitter at 3.125 Gbps	REFCLK = 156.25 MHz Pattern = CJPAT V_{OD} = 1200 mV No Pre-emphasis	-	-	0.17	-	-	0.17	-	-	0.17	UI
XAUI Receiver Jitter Tolerance *(9)*											
Total jitter	Pattern = CJPAT No Equalization DC Gain = 3 dB	> 0.65			> 0.65			> 0.65			UI
Deterministic jitter	Pattern = CJPAT No Equalization DC Gain = 3 dB	> 0.37			> 0.37			> 0.37			UI

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 10 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Sinusoidal Jitter Tolerance (peak-to-peak)	Jitter Frequency = 1.875 MHz Data Rate = 3.75 Gbps REFCLK = 187.5 MHz Pattern = CJPAT No Equalization DC Gain = 3 dB	> 0.1			-			-			UI
	Jitter Frequency = 20 MHz Data Rate = 3.75 Gbps REFCLK = 187.5 MHz Pattern = CJPAT No Equalization DC Gain = 3 dB	> 0.1			-			-			UI
(OIF) CEI Transmitter Jitter Generation *(14)*											
Total Jitter (peak-to-peak)	Data Rate = 6.375 Gbps REFCLK = 318.75 MHz Pattern = PRBS15 Vod=1000 mV *(5)* No Pre-emphasis BER = 10^{-12}			0.3			N/A			N/A	UI
(OIF) CEI Receiver Jitter Tolerance *(14)*											
Deterministic Jitter Tolerance (peak-to-peak)	Data Rate = 6.375 Gbps Pattern = PRBS31 Equalizer Setting = 15 DC Gain = 0 dB BER = 10^{-12}	> 0.675			N/A			N/A			UI

Figure 4–10. Measurement Setup for t_{zx}

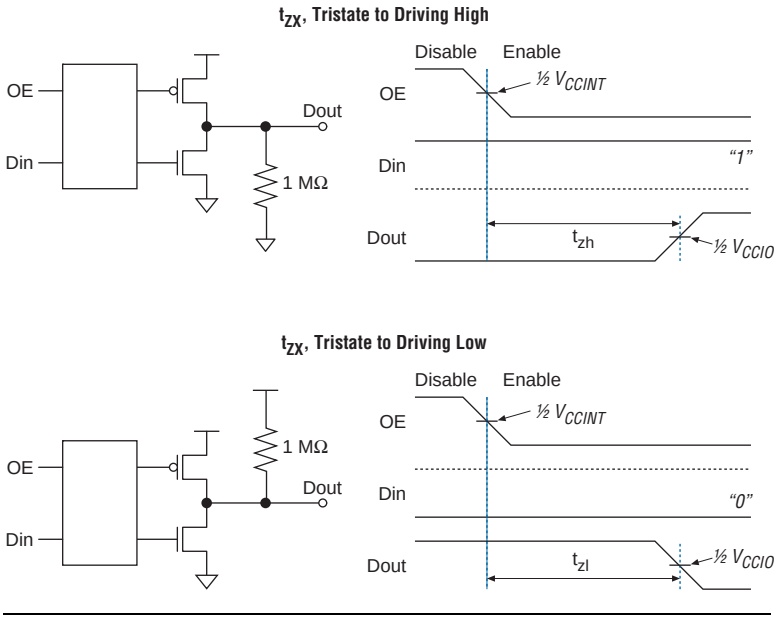


Table 4–54 specifies the input timing measurement setup.

Table 4–54. Timing Measurement Methodology for Input Pins (Part 1 of 2) *Notes (1), (2), (3), (4)*

I/O Standard	Measurement Conditions			Measurement Point
	V_{CCIO} (V)	V_{REF} (V)	Edge Rate (ns)	VMEAS (V)
LVTTL *(5)*	3.135		3.135	1.5675
LVCMOS *(5)*	3.135		3.135	1.5675
2.5 V *(5)*	2.375		2.375	1.1875
1.8 V *(5)*	1.710		1.710	0.855
1.5 V *(5)*	1.425		1.425	0.7125
PCI *(6)*	2.970		2.970	1.485
PCI-X *(6)*	2.970		2.970	1.485
SSTL-2 Class I	2.325	1.163	2.325	1.1625
SSTL-2 Class II	2.325	1.163	2.325	1.1625
SSTL-18 Class I	1.660	0.830	1.660	0.83
SSTL-18 Class II	1.660	0.830	1.660	0.83
1.8-V HSTL Class I	1.660	0.830	1.660	0.83

Table 4–92 shows the maximum output clock toggle rates for Stratix II GX device row pins.

Table 4–92. Stratix II GX Maximum Output Clock Rate for Row Pins (Part 1 of 2)

I/O Standard	Drive Strength	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
LVTTL	4 mA	270	225	210	MHz
	8 mA	435	355	325	MHz
	12 mA *(1)*	580	475	420	MHz
LVCMOS	4 mA	290	250	230	MHz
	8 mA	565	480	440	MHz
	12 mA *(1)*	350	350	297	MHz
2.5 V	4 mA	230	194	180	MHz
	8 mA	430	380	380	MHz
	12 mA *(1)*	630	575	550	MHz
1.8 V	2 mA	120	109	104	MHz
	4 mA	285	250	230	MHz
	6 mA	450	390	360	MHz
	8 mA *(1)*	660	570	520	MHz
1.5 V	2 mA	244	200	180	MHz
	4 mA *(1)*	470	370	325	MHz
SSTL-2 Class I	8 mA	400	300	300	MHz
	12 mA *(1)*	400	400	350	MHz
SSTL-2 Class II	16 mA	350	350	300	MHz
	20 mA *(1)*	350	350	297	MHz
SSTL-18 Class I	4 mA	200	150	150	MHz
	6 mA	350	250	200	MHz
	8 mA	450	300	300	MHz
	10 mA	500	400	400	MHz
	12 mA *(1)*	350	350	297	MHz
1.8-V HSTL Class I	4 mA	300	300	300	MHz
	6 mA	500	450	450	MHz
	8 mA	650	600	600	MHz
	10 mA	700	650	600	MHz
	12 mA *(1)*	700	700	650	MHz
1.5-V HSTL Class I	4 mA	350	300	300	MHz
	6 mA	500	500	450	MHz
	8 mA *(1)*	700	650	600	MHz

Table 4–96. Stratix II GX Maximum Output Clock Rate for Dedicated Clock Pins (Series Termination) (Part 2 of 2)

I/O Standard	Drive Strength	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
SSTL-18 Class II	OCT_25_OHMS	550	500	450	MHz
1.5-V HSTL Class I	OCT_50_OHMS	600	550	500	MHz
1.8-V HSTL Class I	OCT_50_OHMS	650	600	600	MHz
1.8-V HSTL Class II	OCT_25_OHMS	500	500	450	MHz
DIfferential SSTL-2 Class I	OCT_50_OHMS	600	500	500	MHz
DIfferential SSTL-2 Class II	OCT_25_OHMS	600	550	500	MHz
DIfferential SSTL-18 Class I	OCT_50_OHMS	560	400	350	MHz
DIfferential SSTL-18 Class II	OCT_25_OHMS	550	500	450	MHz
1.8-V differential HSTL Class I	OCT_50_OHMS	650	600	600	MHz
1.8-V differential HSTL Class II	OCT_25_OHMS	500	500	450	MHz
1.5-V differential HSTL Class I	OCT_50_OHMS	600	550	500	MHz

Table 4–97 specifies the derating factors for the output clock toggle rate for a non 0 pF load.

Table 4–97. Maximum Output Clock Toggle Rate Derating Factors (Part 1 of 5)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate Derating Factors (ps/pF)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		-3	-4	-5	-3	-4	-5	-3	-4	-5
3.3-V LVTTL	4 mA	478	510	510	478	510	510	466	510	510
	8 mA	260	333	333	260	333	333	291	333	333
	12 mA	213	247	247	213	247	247	211	247	247
	16 mA	136	197	197	-	-	-	166	197	197
	20 mA	138	187	187	-	-	-	154	187	187
	24 mA	134	177	177	-	-	-	143	177	177

Table 4–110. Enhanced PLL Specifications (Part 2 of 2)					
Name	**Description**	**Min**	**Typ**	**Max**	**Unit**
f_{VCO}	PLL VCO operating range for –3 and –4 speed grade devices	300		1,040	MHz
	PLL VCO operating range for –5 speed grade devices	300		840	MHz
f_{SS}	Spread-spectrum modulation frequency	100		500	kHz
% spread	Percent down spread for a given clock frequency	0.4	0.5	0.6	%
t_{PLL_PSERR}	Accuracy of PLL phase shift			±30	ps
t_{ARESET}	Minimum pulse width on `areset` signal.	10			ns
$t_{ARESET\_RECONFIG}$	Minimum pulse width on the `areset` signal when using PLL reconfiguration. Reset the PLL after `scandone` goes high.	500			ns
$t_{RECONFIGWAIT}$	The time required for the wait after the reconfiguration is done and the areset is applied.			2	us

(1) This is limited by the I/O f_{MAX}. See Tables 4–91 through 4–95 for the maximum.
(2) If the counter cascading feature of the PLL is utilized, there is no minimum output clock frequency.

Table 4–111. Fast PLL Specifications (Part 1 of 2)					
Name	**Description**	**Min**	**Typ**	**Max**	**Unit**
f_{IN}	Input clock frequency (for -3 and -4 speed grade devices)	16		717	MHz
	Input clock frequency (for -5 speed grade devices)	16		640	MHz
f_{INPFD}	Input frequency to the PFD	16		500	MHz
f_{INDUTY}	Input clock duty cycle	40		60	%
$t_{INJITTER}$	Input clock jitter tolerance in terms of period jitter. Bandwidth ≤2 MHz		0.5		ns (p-p)
	Input clock jitter tolerance in terms of period jitter. Bandwidth > 0.2 MHz		1.0		ns (p-p)

Table 4–115. DQS Bus Clock Skew Adder Specifications (t_{DQS}_CLOCK_SKEW_ADDER)	
Mode	**DQS Clock Skew Adder (ps)** *(1)*
4 DQ per DQS	40
9 DQ per DQS	70
18 DQ per DQS	75
36 DQ per DQS	95

(1) This skew specification is the absolute maximum and minimum skew. For example, skew on a 40 DQ group is 40 ps or 20 ps.

Table 4–116. DQS Phase Offset Delay Per Stage (ps) *Notes (1), (2), (3)*				
Speed Grade	**Positive Offset**		**Negative Offset**	
	Min	**Max**	**Min**	**Max**
-3	10	15	8	11
-4	10	15	8	11
-5	10	16	8	12

(1) The delay settings are linear.
(2) The valid settings for phase offset are -32 to +31.
(3) The typical value equals the average of the minimum and maximum values.

JTAG Timing Specifications

Figure 4–14 shows the timing requirements for the JTAG signals

Document Revision History

Table 6–105 shows the revision history for this chapter.

Table 4–118. Document Revision History (Part 1 of 5)

Date and Document Version	Changes Made	Summary of Changes
June 2009 v4.6	Replaced Table 4–31 Updated: • Table 4–5 • Table 4–6 • Table 4–7 • Table 4–8 • Table 4–9 • Table 4–10 • Table 4–11 • Table 4–12 • Table 4–13 • Table 4–14 • Table 4–15 • Table 4–16 • Table 4–17 • Table 4–18 • Table 4–20 • Table 4–50 • Table 4–95 • Table 4–105 • Table 4–110 • Table 4–111	
October 2007 v4.5	Updated: • Table 4–3 • Table 4–6 • Table 4–16 • Table 4–19 • Table 4–20 • Table 4–21 • Table 4–22 • Table 4–55 • Table 4–106 • Table 4–107 • Table 4–108 • Table 4–109 • Table 4–112	
	Updated title only in Tables 4–88 and 4–89.	
	Minor text edits.	

Table 4–118. Document Revision History (Part 5 of 5)		
Date and Document Version	**Changes Made**	**Summary of Changes**
April 2006, v3.0	• Updated Table 6–3. • Updated Table 6–5. • Updated Table 6–7. • Added Table 6–42. • Updated "Internal Timing Parameters" section (Tables 6–43 through 6–48). • Updated "Stratix II GX Clock Timing Parameters" section (Tables 6–49 through 6–65). • Updated "IOE Programmable Delay" section (Tables 6–67 and 6–68) • Updated "I/O Delays" section (Tables 6–71 through 6–74. • Updated "Maximum Input & Output Clock Toggle Rate" section. Replaced tables 6-73 and 6-74 with Tables 6–75 through 6–83. Input and output clock rates for row, column, and dedicated clock pins are now in separate tables.	
February 2006, v2.1	• Updated Tables 6–4 and 6–5. • Updated Tables 6–49 through 6–65 (removed column designations for industrial/commercial and removed industrial numbers).	
December 2005, v2.0	Updated timing numbers.	
October 2005 v1.1	• Updated Table 6–7. • Updated Table 6–38. • Updated 3.3-V PCML information and notes to Tables 6–73 through 6–76. • Minor textual changes throughout the document.	
October 2005 v1.0	Added chapter to the *Stratix II GX Device Handbook*.	