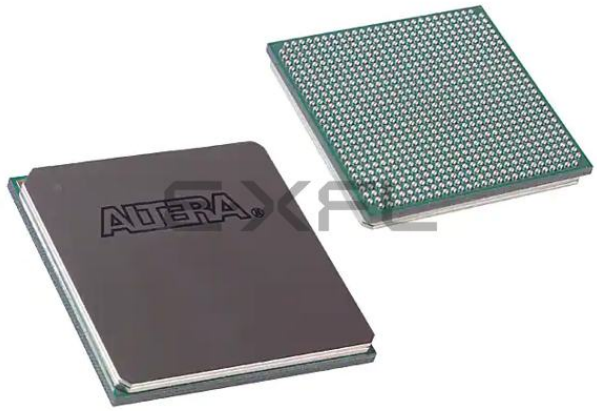

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3022
Number of Logic Elements/Cells	60440
Total RAM Bits	2544192
Number of I/O	364
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	780-BBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2sgx60df780c5

Control and Status Signals

The rx_enapatternalign signal is the FPGA control signal that enables word alignment in non-automatic modes. The rx_enapatternalign signal is not used in automatic modes (PCI Express, XAUI, GIGE, CPRI, and Serial RapidIO).

In manual alignment mode, after the rx_enapatternalign signal is activated, the rx_syncstatus signal goes high for one parallel clock cycle to indicate that the alignment pattern has been detected and the word boundary has been locked. If the rx_enapatternalign is deactivated, the rx_syncstatus signal acts as a re-synchronization signal to signify that the alignment pattern has been detected but not locked on a different word boundary.

When using the synchronization state machine, the rx_syncstatus signal indicates the link status. If the rx_syncstatus signal is high, link synchronization is achieved. If the rx_syncstatus signal is low, synchronization has not yet been achieved, or there were enough code group errors to lose synchronization.

In some modes, the rx_enapatternalign signal can be configured to operate as a rising edge signal.

For more information on manual alignment modes, refer to the *Stratix II GX Device Handbook*, volume 2.

When the rx_enapatternalign signal is sensitive to the rising edge, each rising edge triggers a new boundary alignment search, clearing the rx_syncstatus signal.

The rx_patterndetect signal pulses high during a new alignment, and also whenever the alignment pattern occurs on the current word boundary.

SONET/SDH

In all the SONET/SDH modes, you can configure the word aligner to either align to A1A2 or A1A1A2A2 patterns. Once the pattern is found, the word boundary is aligned and the word aligner asserts the rx_patterndetect signal for one clock cycle.

When the FIFO pointers initialize, the receiver domain clock must remain phase locked to receiver FPGA clock.

After resetting the receiver FIFO buffer, writing to the receiver FIFO buffer begins and continues on each parallel clock. The phase compensation FIFO buffer is eight words deep for PIPE mode and four words deep for all other modes.

Loopback Modes

The Stratix II GX transceiver has built-in loopback modes for debugging and testing. The loopback modes are configured in the Stratix II GX ALT2GXB megafunction in the Quartus II software. The available loopback modes are:

- Serial loopback
- Parallel loopback
- Reverse serial loopback
- Reverse serial loopback (pre-CDR)
- PCI Express PIPE reverse parallel loopback (available only in PIPE mode)

Serial Loopback

The serial loopback mode exercises all the transceiver logic, except for the input buffer. Serial loopback is available for all non-PIPE modes. The loopback function is dynamically enabled through the `rx_seriallpbken` port on a channel-by-channel basis.

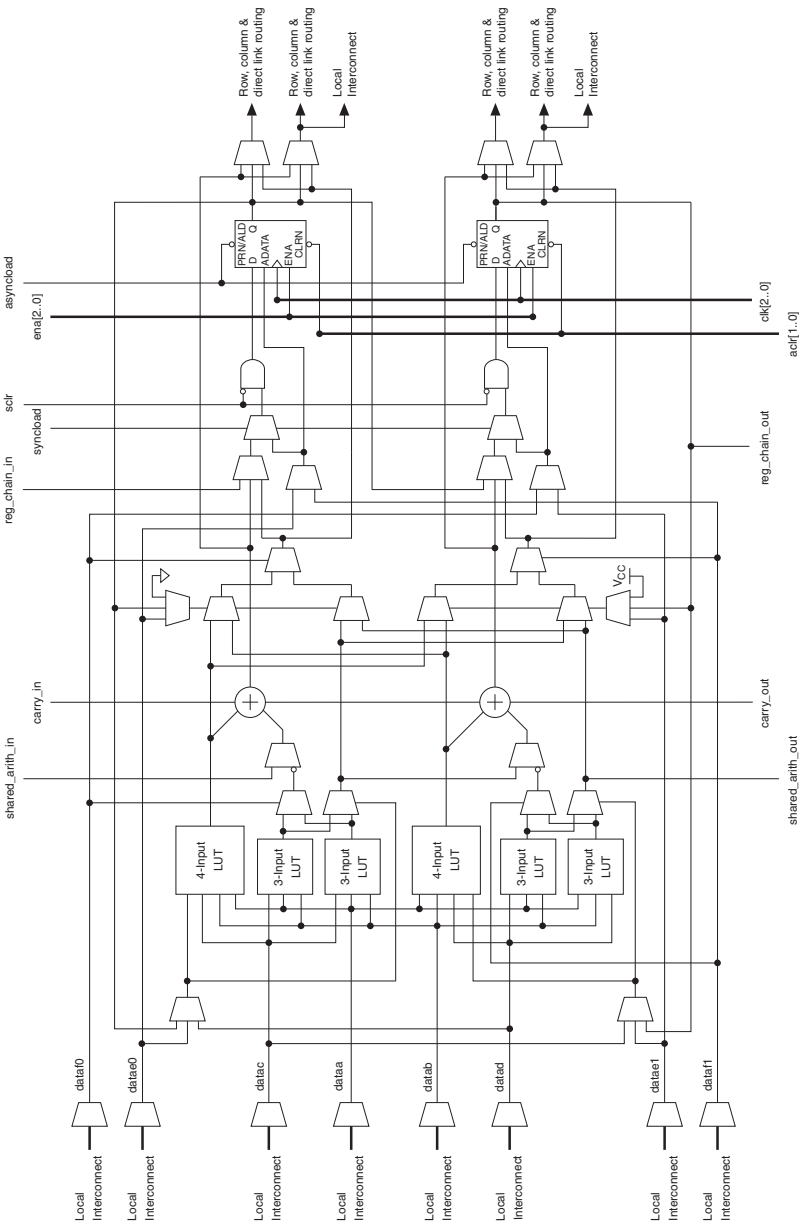
In serial loopback mode, the data on the transmit side is sent by the PLD. A separate mode is available in the ALT2GXB megafunction under Basic protocol mode, in which PRBS data is generated and verified internally in the transceiver. The PRBS patterns available in this mode are shown in Table 2–10.

Table 2–10 shows the BIST data output and verifier alignment pattern.

Table 2–10. BIST Data Output and Verifier Alignment Pattern

Pattern	Polynomial	Parallel Data Width			
		8-Bit	10-Bit	16-Bit	20-Bit
PRBS-7	×7 + ×6 + 1				✓
PRBS-10	×10 + ×7 + 1		✓		

Figure 2–36. Stratix II GX ALM Details



Carry Chain

The carry chain provides a fast carry function between the dedicated adders in arithmetic or shared arithmetic mode. Carry chains can begin in either the first ALM or the fifth ALM in a LAB. The final carry-out signal is routed to an ALM, where it is fed to local, row, or column interconnects.

The Quartus II Compiler automatically creates carry chain logic during compilation, or you can create it manually during design entry. Parameterized functions, such as LPM functions, automatically take advantage of carry chains for the appropriate functions. The Quartus II Compiler creates carry chains longer than 16 (8 ALMs in arithmetic or shared arithmetic mode) by linking LABs together automatically. For enhanced fitting, a long carry chain runs vertically, allowing fast horizontal connections to TriMatrix memory and DSP blocks. A carry chain can continue as far as a full column. To avoid routing congestion in one small area of the device when a high fan-in arithmetic function is implemented, the LAB can support carry chains that only utilize either the top half or the bottom half of the LAB before connecting to the next LAB. The other half of the ALMs in the LAB is available for implementing narrower fan-in functions in normal mode. Carry chains that use the top four ALMs in the first LAB will carry into the top half of the ALMs in the next LAB within the column. Carry chains that use the bottom four ALMs in the first LAB will carry into the bottom half of the ALMs in the next LAB within the column. Every other column of the LABs are top-half bypassable, while the other LAB columns are bottom-half bypassable. Refer to "MultiTrack Interconnect" on page 2–63 for more information on carry chain interconnect.

Shared Arithmetic Mode

In shared arithmetic mode, the ALM can implement a three-input add. In this mode, the ALM is configured with four 4-input LUTs. Each LUT either computes the sum of three inputs or the carry of three inputs. The output of the carry computation is fed to the next adder (either to `adder1` in the same ALM or to `adder0` of the next ALM in the LAB) using a dedicated connection called the shared arithmetic chain. This shared arithmetic chain can significantly improve the performance of an adder tree by reducing the number of summation stages required to implement an adder tree. Figure 2–43 shows the ALM in shared arithmetic mode.

Table 2–19. TriMatrix Memory Features (Part 2 of 2)

Memory Feature	M512 RAM Block (32 × 18 Bits)	M4K RAM Block (128 × 36 Bits)	M-RAM Block (4K × 144 Bits)
Simple dual-port memory mixed width support	✓	✓	✓
True dual-port memory mixed width support		✓	✓
Power-up conditions	Outputs cleared	Outputs cleared	Outputs unknown
Register clears	Output registers	Output registers	Output registers
Mixed-port read-during-write	Unknown output/old data	Unknown output/old data	Unknown output
Configurations	512 × 1 256 × 2 128 × 4 64 × 8 64 × 9 32 × 16 32 × 18	4K × 1 2K × 2 1K × 4 512 × 8 512 × 9 256 × 16 256 × 18 128 × 32 128 × 36	64K × 8 64K × 9 32K × 16 32K × 18 16K × 32 16K × 36 8K × 64 8K × 72 4K × 128 4K × 144

Note to Table 2–19:
(1) Violating the setup or hold time on the memory block address registers could corrupt memory contents. This applies to both read and write operations.

TriMatrix memory provides three different memory sizes for efficient application support. The Quartus II software automatically partitions the user-defined memory into the embedded memory blocks using the most efficient size combinations. You can also manually assign the memory to a specific block size or a mixture of block sizes.

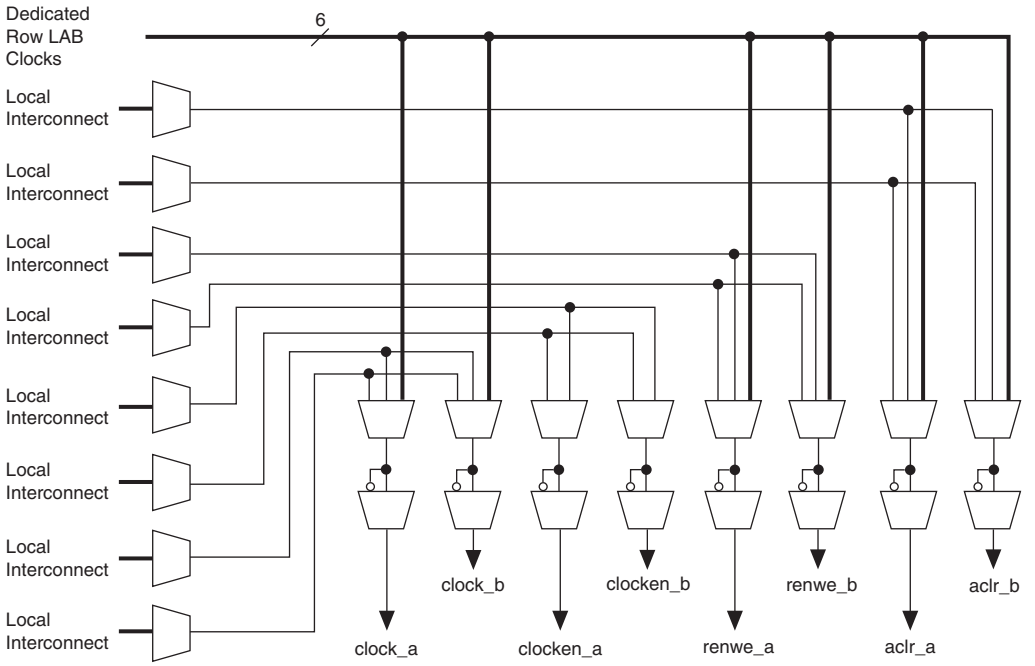
M512 RAM Block

The M512 RAM block is a simple dual-port memory block and is useful for implementing small FIFO buffers, DSP, and clock domain transfer applications. Each block contains 576 RAM bits (including parity bits). M512 RAM blocks can be configured in the following modes:

- Simple dual-port RAM
- Single-port RAM
- FIFO
- ROM
- Shift register

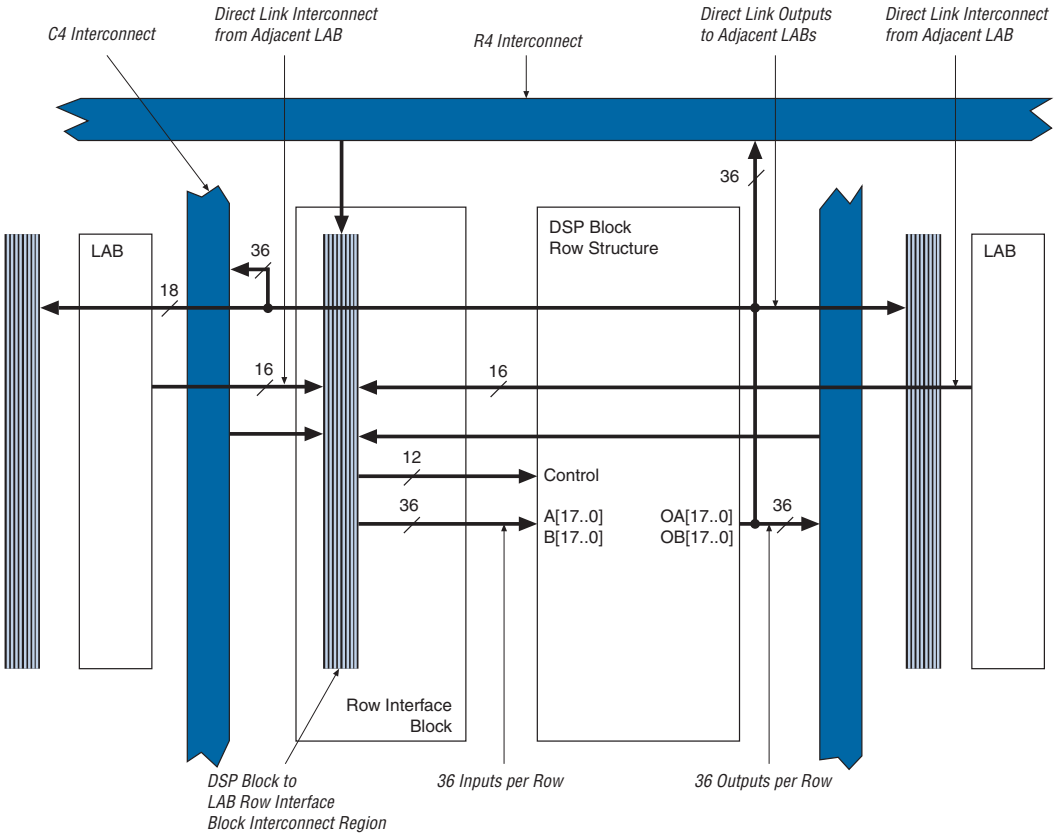
When configured as RAM or ROM, you can use an initialization file to pre-load the memory contents.

Figure 2–51. M4K RAM Block Control Signals



The R4, C4, and direct link interconnects from adjacent LABs drive the M4K RAM block local interconnect. The M4K RAM blocks can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 16 direct link input connections to the M4K RAM block are possible from the left adjacent LABs and another 16 possible from the right adjacent LAB. M4K RAM block outputs can also connect to left and right LABs through direct link interconnect. Figure 2–52 shows the M4K RAM block to logic array interface.

Figure 2–60. DSP Block Interface to Interconnect

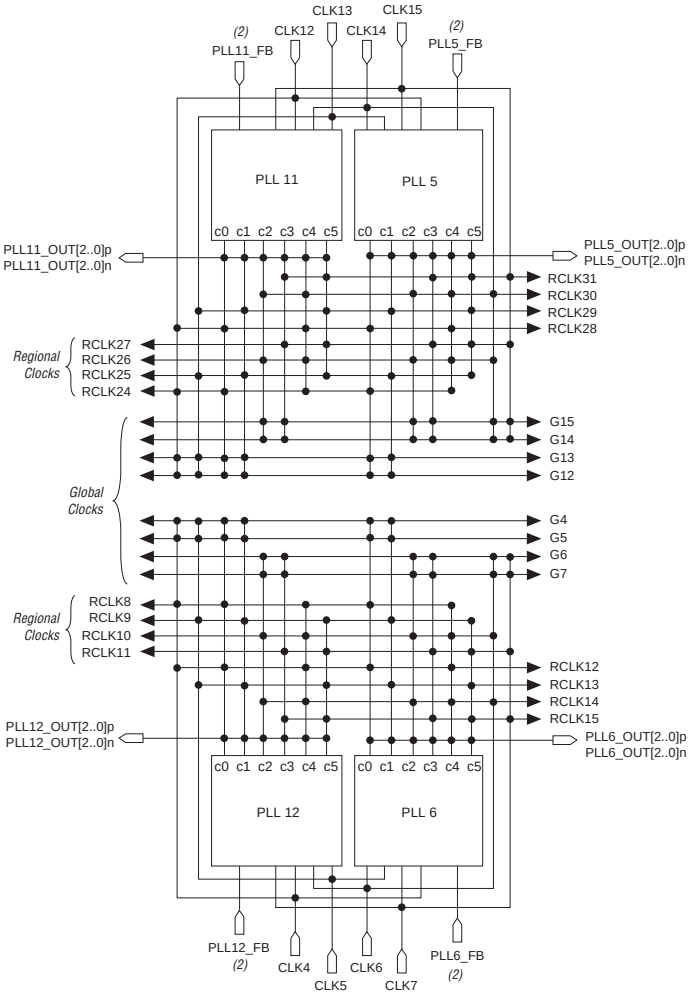


A bus of 44 control signals feeds the entire DSP block. These signals include clocks, asynchronous clears, clock enables, signed and unsigned control signals, addition and subtraction control signals, rounding and saturation control signals, and accumulator synchronous loads. The clock signals are routed from LAB row clocks and are generated from specific LAB rows at the DSP block interface. The LAB row source for control signals, data inputs, and outputs is shown in Table 2–23.

Refer to the *DSP Blocks in Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook* for more information on DSP blocks.

Figure 2–73 shows the global and regional clocking from enhanced PLL outputs and top and bottom CLK pins.

Figure 2–73. Global and Regional Clock Connections from Top and Bottom Clock Pins and Enhanced PLL Outputs *Notes (1), (2)*



Notes to Figure 2–73:

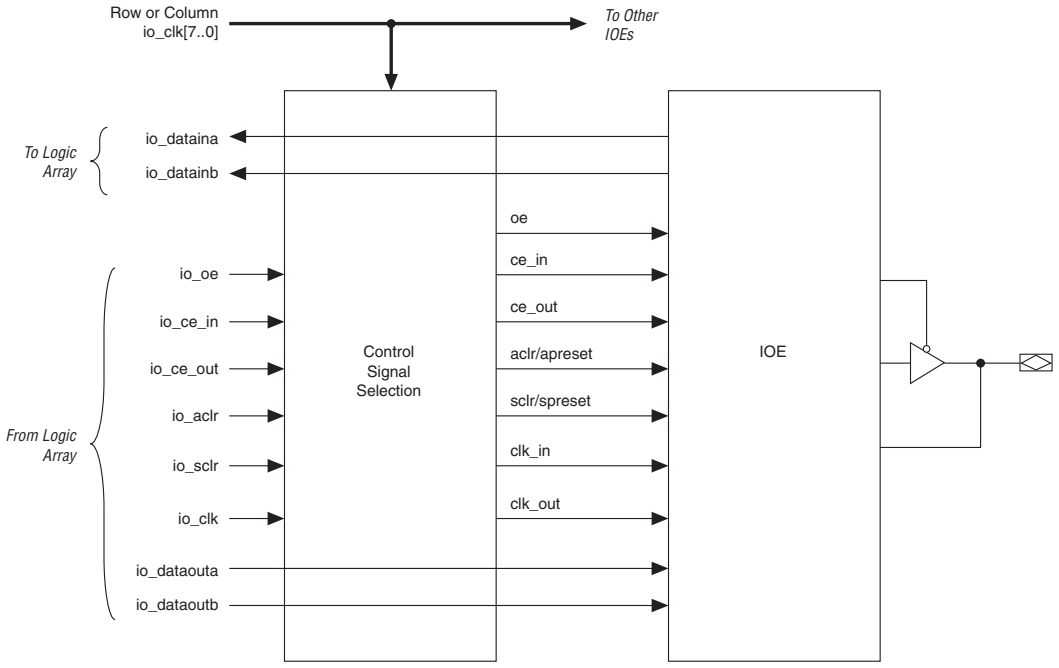
(1) EP2SGX30C/D and EP2SGX60C/D devices only have two enhanced PLLs (5 and 6), but the connectivity from these two PLLs to the global and regional clock networks remains the same as shown.

(2) If the design uses the feedback input, you will lose one (or two, if FBIN is differential) external clock output pin.

There are 32 control and data signals that feed each row or column I/O block. These control and data signals are driven from the logic array. The row or column IOE clocks, `io_clk[7..0]`, provide a dedicated routing resource for low-skew, high-speed clocks. I/O clocks are generated from global or regional clocks. Refer to "PLLs and Clock Networks" on page 2–89 for more information.

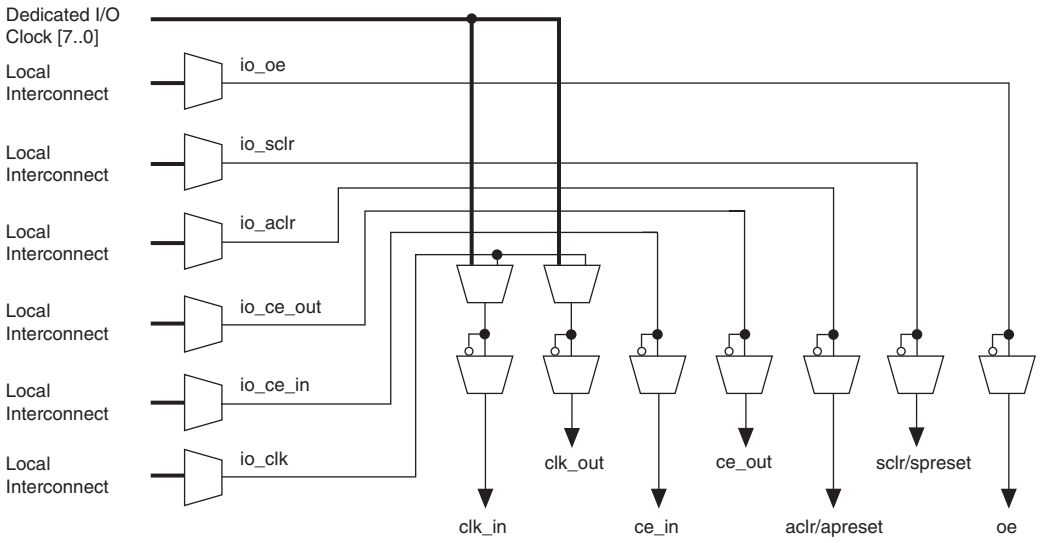
Figure 2–79 illustrates the signal paths through the I/O block.

Figure 2–79. Signal Path Through the I/O Block



Each IOE contains its own control signal selection for the following control signals: `oe`, `ce_in`, `ce_out`, `aclr/apreset`, `sclr/spreset`, `clk_in`, and `clk_out`. Figure 2–80 illustrates the control signal selection.

Figure 2–80. Control Signal Selection per IOE *Note (1)*

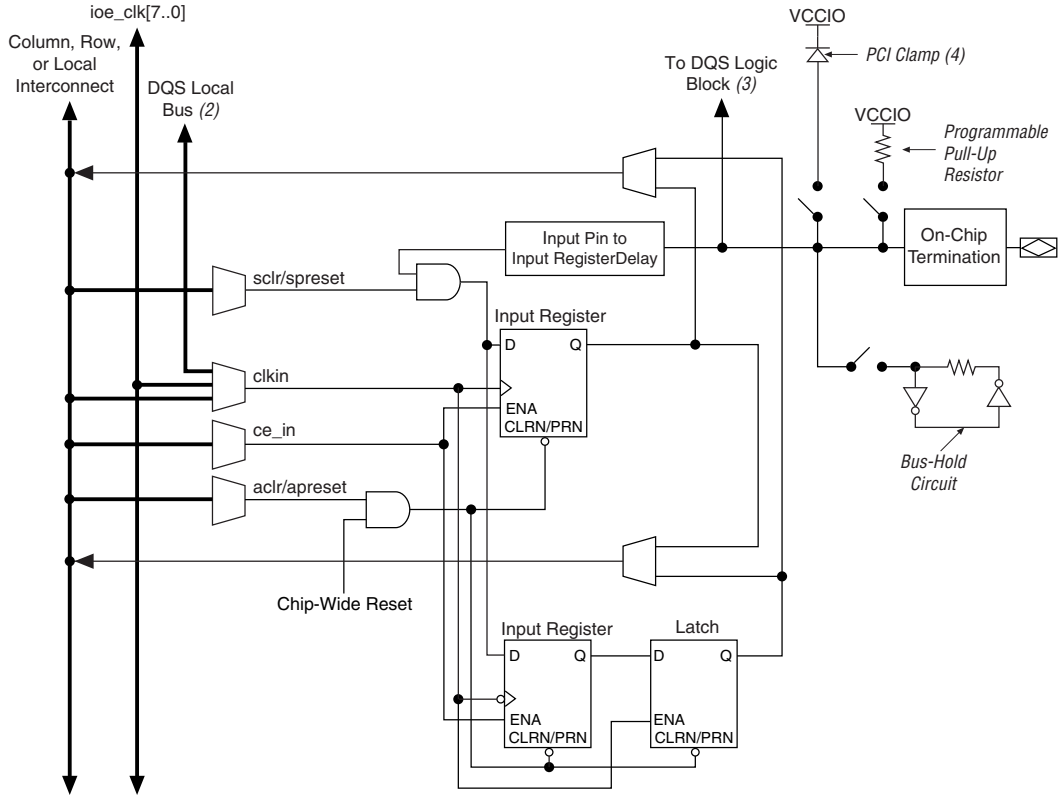


Note to Figure 2–80:

(1) Control signals `ce_in`, `ce_out`, `aclr/apreset`, `sclr/spreset`, and `oe` can be global signals even though their control selection multiplexers are not directly fed by the `ioe_clk[7..0]` signals. The `ioe_clk` signals can drive the I/O local interconnect, which then drives the control selection multiplexers.

In normal bidirectional operation, you can use the input register for input data requiring fast setup times. The input register can have its own clock input and clock enable separate from the OE and output registers. The output register can be used for data requiring fast clock-to-output performance. You can use the OE register for fast clock-to-output enable timing. The OE and output register share the same clock source and the same clock enable source from local interconnect in the associated LAB, dedicated I/O clocks, and the column and row interconnects. Figure 2–81 shows the IOE in bidirectional configuration.

Figure 2–82. Stratix II GX IOE in DDR Input I/O Configuration *Note (1)*



Notes to Figure 2–82:

(1) All input signals to the IOE can be inverted at the IOE.
(2) This signal connection is only allowed on dedicated DQ function pins.
(3) This signal is for dedicated DQS function pins only.
(4) The optional PCI clamp is only available on column I/O pins.

memory, and transmit this compressed bitstream to Stratix II GX FPGAs. During configuration, the Stratix II GX FPGA decompresses the bitstream in real time and programs its SRAM cells. Stratix II GX FPGAs support decompression in the FPP (when using a MAX II device or microprocessor and flash memory), AS, and PS configuration schemes. Decompression is not supported in the PPA configuration scheme nor in JTAG-based configuration.

Remote System Upgrades

Shortened design cycles, evolving standards, and system deployments in remote locations are difficult challenges faced by system designers. Stratix II GX devices can help effectively deal with these challenges with their inherent re programmability and dedicated circuitry to perform remote system updates. Remote system updates help deliver feature enhancements and bug fixes without costly recalls, reducing time to market, and extending product life.

Stratix II GX FPGAs feature dedicated remote system upgrade circuitry to facilitate remote system updates. Soft logic (Nios processor or user logic) implemented in the Stratix II GX device can download a new configuration image from a remote location, store it in configuration memory, and direct the dedicated remote system upgrade circuitry to initiate a reconfiguration cycle. The dedicated circuitry performs error detection during and after the configuration process, recovers from any error condition by reverting back to a safe configuration image, and provides error status information. This dedicated remote system upgrade circuitry avoids system downtime and is the critical component for successful remote system upgrades.

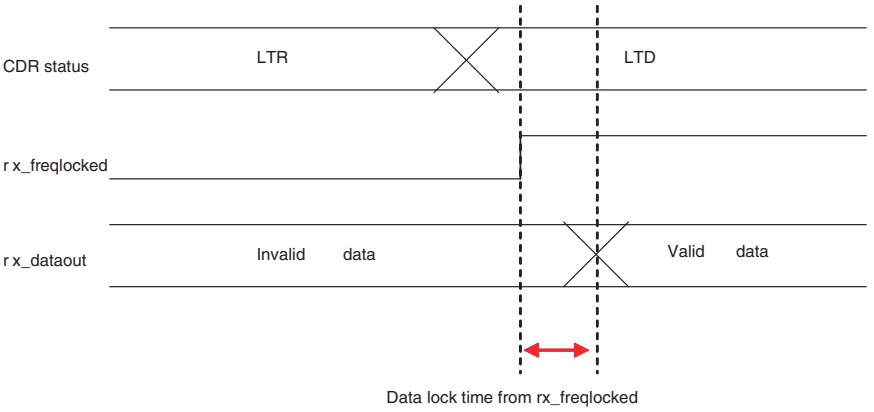
Remote system configuration is supported in the following Stratix II GX configuration schemes: FPP, AS, PS, and PPA. Remote system configuration can also be implemented in conjunction with Stratix II GX features such as real-time decompression of configuration data and design security using AES for secure and efficient field upgrades.

Refer to the *Remote System Upgrades with Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook* for more information about remote configuration in Stratix II GX devices.

Configuring Stratix II GX FPGAs with JRunner

The JRunner™ software driver configures Altera FPGAs, including Stratix II GX FPGAs, through the ByteBlaster II or ByteBlasterMV cables in JTAG mode. The programming input file supported is in Raw Binary File (**.rbf**) format. JRunner also requires a Chain Description File (**.cdf**)

Figure 4–2. Lock Time Parameters for Automatic Mode



Figures 4–3 and 4–4 show differential receiver input and transmitter output waveforms, respectively.

Figure 4–3. Receiver Input Waveform

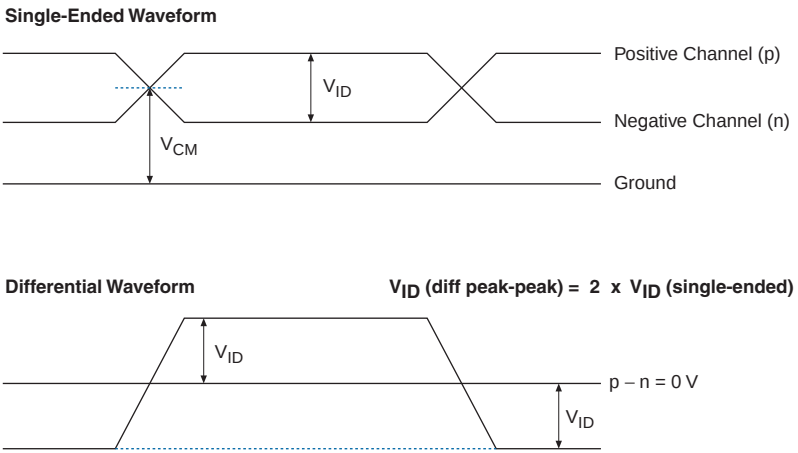


Table 4–44. 1.5-V HSTL Class I and II Differential Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage		1.425	1.5	1.575	V
V_{DIF} (DC)	DC input differential voltage		0.2			V
V_{CM} (DC)	DC common mode input voltage		0.68		0.9	V
V_{DIF} (AC)	AC differential input voltage		0.4			V
V_{OX} (AC)	AC differential cross point voltage		0.68		0.9	V

Table 4–45. 1.8-V HSTL Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.71	1.80	1.89	V
V_{REF}	Input reference voltage		0.85	0.90	0.95	V
V_{TT}	Termination voltage		0.85	0.90	0.95	V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 8 mA *(1)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OH} = –8 mA *(1)*			0.4	V

Note to Table 4–45:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Final timing numbers are based on actual device operation and testing. These numbers reflect the actual performance of the device under worst-case voltage and junction temperature conditions.

Table 4–52. Stratix II GX Device Timing Model Status

Device	Preliminary	Final
EP2SGX30		✓
EP2SGX60		✓
EP2SGX90		✓
EP2SGX130		✓

I/O Timing Measurement Methodology

Different I/O standards require different baseline loading techniques for reporting timing delays. Altera characterizes timing delays with the required termination for each I/O standard and with 0 pF (except for PCI and PCI-X which use 10 pF) loading and the timing is specified up to the output pin of the FPGA device. The Quartus II software calculates the I/O timing for each I/O standard with a default baseline loading as specified by the I/O standards.

The following measurements are made during device characterization. Altera measures clock-to-output delays (t_{CO}) at worst-case process, minimum voltage, and maximum temperature (PVT) for default loading conditions shown in Table 4–53. Use the following equations to calculate clock pin to output pin timing for Stratix II GX devices.

t_{CO} from clock pin to I/O pin = delay from clock pad to I/O output register + IOE output register clock-to-output delay + delay from output register to output pin + I/O output delay

t_{xz}/t_{zx} from clock pin to I/O pin = delay from clock pad to I/O output register + IOE output register clock-to-output delay + delay from output register to output pin + I/O output delay + output enable pin delay

Simulation using IBIS models is required to determine the delays on the PCB traces in addition to the output pin delay timing reported by the Quartus II software and the timing model in the device handbook.

1. Simulate the output driver of choice into the generalized test setup, using values from Table 4–53.
2. Record the time to V_{MEAS}.

Table 4–55. Stratix II GX Performance Notes (Part 2 of 3) *Note (1)*

Applications		Resources Used			Performance				
		ALUTs	TriMatrix Memory Blocks	DSP Blocks	-3 Speed Grade (2)	-3 Speed Grade (3)	-4 Speed Grade	-5 Speed Grade	Units
TriMatrix Memory MegaRAM block	Single port RAM 4K x 144bit	0	1	0	349.65	333.33	313.47	261.09	MHz
	Simple dual-port RAM 4K x 144bit	0	1	0	420.16	400.0	375.93	313.47	MHz
	True dual-port RAM 4K x 144 bit	0	1	0	349.65	333.33	313.47	261.09	MHz
	Single port RAM 8K x 72 bit	0	1	0	354.6	337.83	317.46	263.85	MHz
	Simple dual-port RAM 8K x 72 bit	0	1	0	420.16	400.0	375.93	313.47	MHz
	True dual-port RAM 8K x 72 bit	0	1	0	349.65	333.33	313.47	261.09	MHz
	Single port RAM 16K x 36 bit	0	1	0	364.96	347.22	325.73	271.73	MHz
	Simple dual-port RAM 16K x 36 bit	0	1	0	420.16	400.0	375.93	313.47	MHz
	True dual-port RAM 16K x 36 bit	0	1	0	359.71	342.46	322.58	268.09	MHz
	Single port RAM 32K x 18 bit	0	1	0	364.96	347.22	325.73	271.73	MHz
	Simple dual-port RAM 32K x 18 bit	0	1	0	420.16	400.0	375.93	313.47	MHz
	True dual-port RAM 32K x 18 bit	0	1	0	359.71	342.46	322.58	268.09	MHz

Internal Timing Parameters

Refer to Tables 4–56 through 4–61 for internal timing parameters.

Table 4–56. LE_FF Internal Timing Microparameters

Symbol	Parameter	-3 Speed Grade (1)		-3 Speed Grade (2)		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{SU}	LE register setup time before clock	90		95		101		121		ps
t_{H}	LE register hold time after clock	149		157		167		200		ps
t_{CO}	LE register clock-to-output delay	62	94	62	99	62	105	62	127	ps
t_{CLR}	Minimum clear pulse width	204		214		227		273		ps
t_{PRE}	Minimum preset pulse width	204		214		227		273		ps
t_{CLKL}	Minimum clock low time	612		642		683		820		ps
t_{CLKH}	Minimum clock high time	612		642		683		820		ps
t_{LUT}		170	378	170	397	170	422	170	507	
t_{ADDER}		372	619	372	650	372	691	372	829	

Notes to Table 4–56:
(1) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
(2) This column refers to –3 speed grades for EP2SGX130 devices.

Table 4–57. IOE Internal Timing Microparameters (Part 1 of 2)

Symbol	Parameter	-3 Speed Grade (1)		-3 Speed Grade (2)		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{SU}	IOE input and output register setup time before clock	122		128		136		163		ps
t_{H}	IOE input and output register hold time after clock	72		75		80		96		ps
t_{CO}	IOE input and output register clock-to-output delay	101	169	101	177	101	188	101	226	ps

Table 4–86. Stratix II GX I/O Output Delay for Column Pins (Part 6 of 7)								
I/O Standard	Drive Strength	Parameter	Fast Corner Industrial/ Commercial	-3 Speed Grade *(3)*	-3 Speed Grade *(4)*	-4 Speed Grade	-5 Speed Grade	Unit
Differential SSTL-18 Class II *(2)*	8 mA	t_{OP}	925	1597	1675	1782	1904	ps
		t_{DIP}	947	1663	1745	1856	1994	ps
	16 mA	t_{OP}	937	1578	1655	1761	1882	ps
		t_{DIP}	959	1644	1725	1835	1972	ps
	18 mA	t_{OP}	933	1585	1663	1768	1890	ps
		t_{DIP}	955	1651	1733	1842	1980	ps
	20 mA	t_{OP}	933	1583	1661	1766	1888	ps
		t_{DIP}	955	1649	1731	1840	1978	ps
1.8-V differential HSTL Class I *(2)*	4 mA	t_{OP}	956	1608	1687	1794	1943	ps
		t_{DIP}	978	1674	1757	1868	2033	ps
	6 mA	t_{OP}	962	1595	1673	1779	1928	ps
		t_{DIP}	984	1661	1743	1853	2018	ps
	8 mA	t_{OP}	940	1586	1664	1769	1917	ps
		t_{DIP}	962	1652	1734	1843	2007	ps
	10 mA	t_{OP}	944	1591	1669	1775	1923	ps
		t_{DIP}	966	1657	1739	1849	2013	ps
	12 mA	t_{OP}	936	1585	1663	1768	1916	ps
		t_{DIP}	958	1651	1733	1842	2006	ps
1.8-V differential HSTL Class II *(2)*	16 mA	t_{OP}	919	1385	1453	1545	1680	ps
		t_{DIP}	941	1451	1523	1619	1770	ps
	18 mA	t_{OP}	921	1394	1462	1555	1691	ps
		t_{DIP}	943	1460	1532	1629	1781	ps
	20 mA	t_{OP}	921	1402	1471	1564	1700	ps
		t_{DIP}	943	1468	1541	1638	1790	ps

Table 4–97. Maximum Output Clock Toggle Rate Derating Factors (Part 3 of 5)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate Derating Factors (ps/pF)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		-3	-4	-5	-3	-4	-5	-3	-4	-5
SSTL-18 Class II	8 mA	173	206	206	-	-	-	155	206	206
	16 mA	150	160	160	-	-	-	140	160	160
	18 mA	120	130	130	-	-	-	110	130	130
	20 mA	109	127	127	-	-	-	94	127	127
2.5-V SSTL-2 Class I	8 mA	364	680	680	364	680	680	350	680	680
	12 mA	163	207	207	163	207	207	188	207	207
2.5-V SSTL-2 Class II	16 mA	118	147	147	118	147	147	94	147	147
	20 mA	99	122	122	-	-	-	87	122	122
	24 mA	91	116	116	-	-	-	85	116	116
1.8-V SSTL-18 Class I	4 mA	458	570	570	458	570	570	505	570	570
	6 mA	305	380	380	305	380	380	336	380	380
	8 mA	225	282	282	225	282	282	248	282	282
	10 mA	167	220	220	167	220	220	190	220	220
	12 mA	129	175	175	-	-	-	148	175	175
1.8-V SSTL-18 Class II	8 mA	173	206	206	-	-	-	155	206	206
	16 mA	150	160	160	-	-	-	140	160	160
	18 mA	120	130	130	-	-	-	110	130	130
	20 mA	109	127	127	-	-	-	94	127	127
1.8-V HSTL Class I	4 mA	245	282	282	245	282	282	229	282	282
	6 mA	164	188	188	164	188	188	153	188	188
	8 mA	123	140	140	123	140	140	114	140	140
	10 mA	110	124	124	110	124	124	108	124	124
	12 mA	97	110	110	97	110	110	104	110	110
1.8-V HSTL Class II	16 mA	101	104	104	-	-	-	99	104	104
	18 mA	98	102	102	-	-	-	93	102	102
	20 mA	93	99	99	-	-	-	88	99	99
1.5-V HSTL Class I	4 mA	168	196	196	168	196	196	188	196	196
	6 mA	112	131	131	112	131	131	125	131	131
	8 mA	84	99	99	84	99	99	95	99	99
	10 mA	87	98	98	-	-	-	90	98	98
	12 mA	86	98	98	-	-	-	87	98	98

Table 4–118. Document Revision History (Part 3 of 5)		
Date and Document Version	**Changes Made**	**Summary of Changes**
February 2007 v4.2	Added the “Document Revision History” section to this chapter.	Added support information for the Stratix II GX device.
	Updated Table 4–5: ● Removed last three lines ● Removed note 1 ● Added new note 4	
	Deleted table 6-6.	
	Replaced Table 4–6 with all new information.	
	Added Figures 4–1 and 4–2.	
	Added Tables 4–7 through 4–19.	
	Removed Figures 6-1 through 6-4.	
	Updated Table 4–22: ● Changed R_{CONF} information.	
	Updated Table 4–52 ● SSTL-18 Class I, column 1: changed 25 to 50.	
	Updated: ● Table 4–54 ● Table 4–87 ● Table 4–91 ● Table 4–94	
	Updated Tables 4–62 through 4–77	
	Updated Tables 4–79 and 4–80 ● Added “units” column	
	Updated Tables 4–83 through 4–86 ● Changed column title to “Fast Corner Industrial/Commercial”.	
	Updated Table 4–109. ● Added a new line to the bottom of the table.	
August 2006 v4.1	Update Table 6–75, Table 6–84, and Table 6–90.	