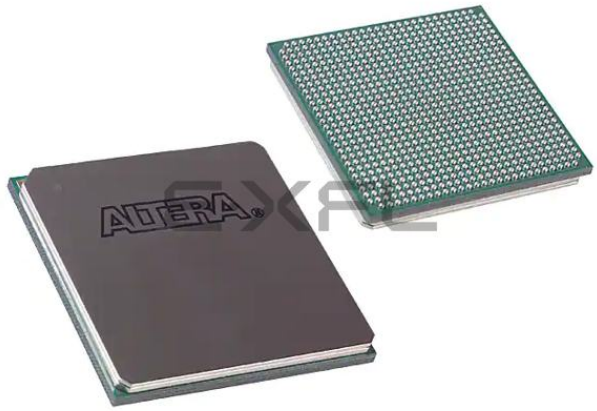

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

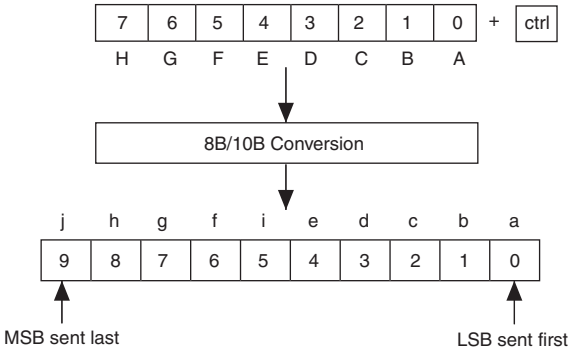
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

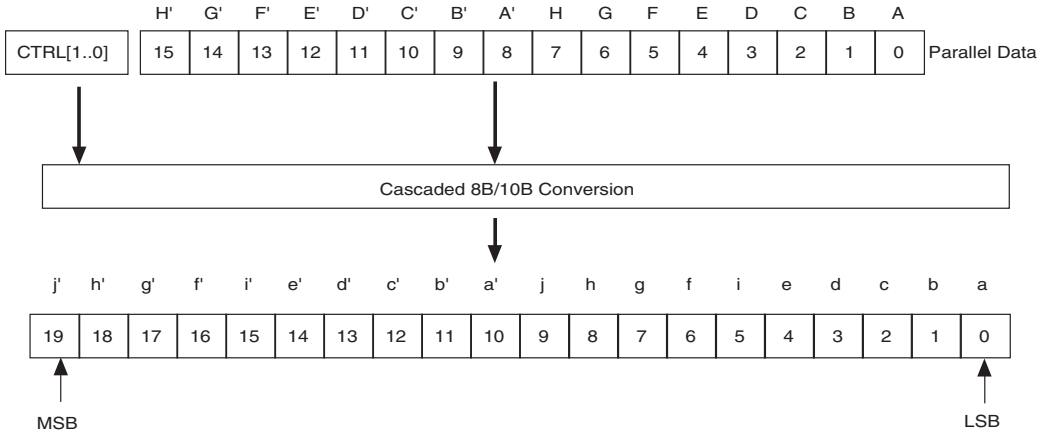
Details	
Product Status	Obsolete
Number of LABs/CLBs	3022
Number of Logic Elements/Cells	60440
Total RAM Bits	2544192
Number of I/O	364
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	780-BBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2sgx60df780i4n

Figure 2–5. 8B/10B Encoding Process



In single-width mode, the 8B/10B encoder generates a 10-bit code group from the 8-bit data and 1-bit control identifier. In double-width mode, there are two 8B/10B encoders that are cascaded together and generate a 20-bit (2 × 10-bit) code group from the 16-bit (2 × 8-bit) data + 2-bit (2 × 1-bit) control identifier. Figure 2–6 shows the 20-bit encoding process. The 8B/10B encoder conforms to the IEEE 802.3 1998 edition standards.

Figure 2–6. 16-Bit to 20-Bit Encoding Process



Upon power on or reset, the 8B/10B encoder has a negative disparity which chooses the 10-bit code from the RD-column. However, the running disparity can be changed via the `tx_forcedisp` and `tx_dispval` ports.

The dynamic reconfiguration block can dynamically reconfigure the following PMA settings:

- Pre-emphasis settings
- Equalizer and DC gain settings
- Voltage Output Differential (V_{OD}) settings

The channel reconfiguration allows you to dynamically modify the data rate, local dividers, and the functional mode of the transceiver channel.

Refer to the *Stratix II GX Device Handbook*, volume 2, for more information.

The dynamic reconfiguration block requires an input clock between 2.5 MHz and 50 MHz. The clock for the dynamic reconfiguration block is derived from a high-speed clock and divided down using a counter.

Individual Power Down and Reset for the Transmitter and Receiver

Stratix II GX transceivers offer a power saving advantage with their ability to shut off functions that are not needed. The device can individually reset the receiver and transmitter blocks and the PLLs. The Stratix II GX device can either globally or individually power down and reset the transceiver. Table 2–16 shows the connectivity between the reset signals and the Stratix II GX transceiver blocks. These reset signals can be controlled from the FPGA or pins.

Clear and Preset Logic Control

LAB-wide signals control the logic for the register's clear and load/preset signals. The ALM directly supports an asynchronous clear and preset function. The register preset is achieved through the asynchronous load of a logic high. The direct asynchronous preset does not require a NOT gate push-back technique. Stratix II GX devices support simultaneous asynchronous load/preset and clear signals. An asynchronous clear signal takes precedence if both signals are asserted simultaneously. Each LAB supports up to two clears and one load/preset signal.

In addition to the clear and load/preset ports, Stratix II GX devices provide a device-wide reset pin (DEV_CLRn) that resets all registers in the device. An option set before compilation in the Quartus II software controls this pin. This device-wide reset overrides all other control signals.

MultiTrack Interconnect

In the Stratix II GX architecture, the MultiTrack interconnect structure with DirectDrive technology provides connections between ALMs, TriMatrix memory, DSP blocks, and device I/O pins. The MultiTrack interconnect consists of continuous, performance-optimized routing lines of different lengths and speeds used for inter- and intra-design block connectivity. The Quartus II Compiler automatically places critical design paths on faster interconnects to improve design performance.

DirectDrive technology is a deterministic routing technology that ensures identical routing resource usage for any function regardless of placement in the device. The MultiTrack interconnect and DirectDrive technology simplify the integration stage of block-based designing by eliminating the re-optimization cycles that typically follow design changes and additions.

The MultiTrack interconnect consists of row and column interconnects that span fixed distances. A routing structure with fixed length resources for all devices allows predictable and repeatable performance when migrating through different device densities. Dedicated row interconnects route signals to and from LABs, DSP blocks, and TriMatrix memory in the same row.

These row resources include:

- Direct link interconnects between LABs and adjacent blocks
- R4 interconnects traversing four blocks to the right or left
- R24 row interconnects for high-speed access across the length of the device

Table 2–21 shows the number of DSP blocks in each Stratix II GX device. DSP block multipliers can optionally feed an adder/subtractor or accumulator in the block, depending on the configuration, which makes routing to ALMs easier, saves ALM routing resources, and increases performance because all connections and blocks are in the DSP block.

Table 2–21. DSP Blocks in Stratix II GX Devices *Note (1)*

Device	DSP Blocks	Total 9 × 9 Multipliers	Total 18 × 18 Multipliers	Total 36 × 36 Multipliers
EP2SGX30	16	128	64	16
EP2SGX60	36	288	144	36
EP2SGX90	48	384	192	48
EP2SGX130	63	504	252	63

Note to Table 2–21:

(1) This list only shows functions that can fit into a single DSP block. Multiple DSP blocks can support larger multiplication functions.

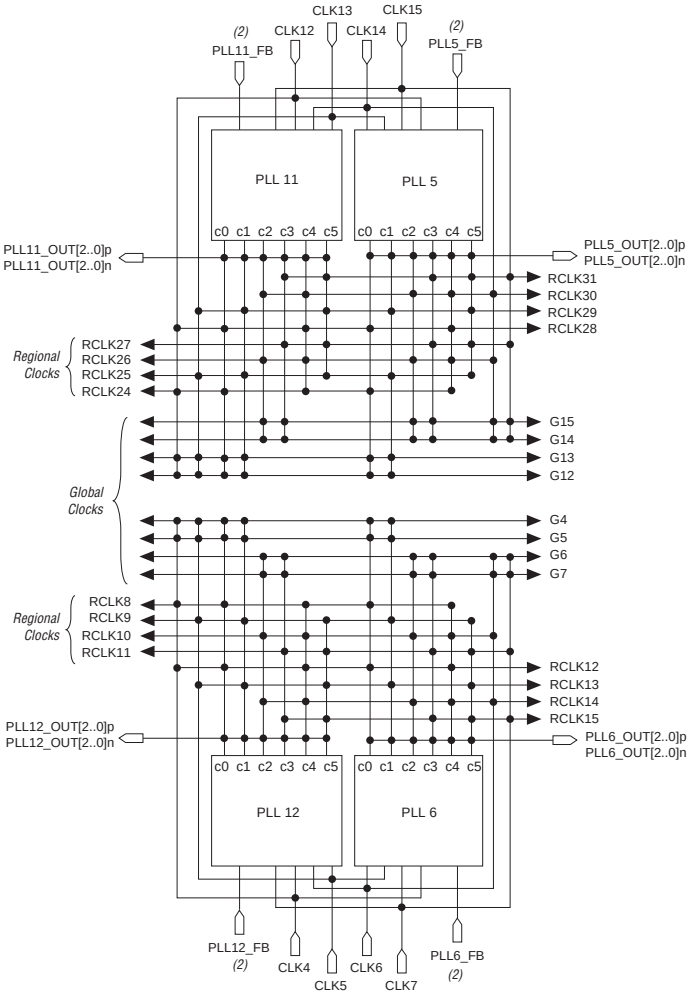
Additionally, the DSP block input registers can efficiently implement shift registers for FIR filter applications, and DSP blocks support Q1.15 format rounding and saturation. Figure 2–58 shows the top-level diagram of the DSP block configured for 18 × 18-bit multiplier mode.

Table 2–27. Global and Regional Clock Connections from Left Side Clock Pins and Fast PLL Outputs (Part 2 of 3)

Left Side Global and Regional Clock Network Connectivity	CLK0	CLK1	CLK2	CLK3	RCLK0	RCLK1	RCLK2	RCLK3	RCLK4	RCLK5	RCLK6	RCLK7
Drivers from internal logic												
GCLKDRV0	✓	✓										
GCLKDRV1	✓	✓										
GCLKDRV2			✓	✓								
GCLKDRV3			✓	✓								
RCLKDRV0					✓				✓			
RCLKDRV1						✓				✓		
RCLKDRV2							✓				✓	
RCLKDRV3								✓				✓
RCLKDRV4					✓				✓			
RCLKDRV5						✓				✓		
RCLKDRV6							✓				✓	
RCLKDRV7								✓				✓
PLL 1 outputs												
c0	✓	✓			✓		✓		✓		✓	
c1	✓	✓				✓		✓		✓		✓
c2			✓	✓	✓		✓		✓		✓	
c3			✓	✓		✓		✓		✓		✓
PLL 2 outputs												
c0	✓	✓				✓		✓		✓		✓
c1	✓	✓			✓		✓		✓		✓	
c2			✓	✓		✓		✓		✓		✓
c3			✓	✓	✓		✓		✓		✓	
PLL 7 outputs												
c0			✓	✓		✓		✓				
c1			✓	✓	✓		✓					
c2	✓	✓				✓		✓				
c3	✓	✓			✓		✓					

Figure 2–73 shows the global and regional clocking from enhanced PLL outputs and top and bottom CLK pins.

Figure 2–73. Global and Regional Clock Connections from Top and Bottom Clock Pins and Enhanced PLL Outputs *Notes (1), (2)*



Notes to Figure 2–73:

(1) EP2SGX30C/D and EP2SGX60C/D devices only have two enhanced PLLs (5 and 6), but the connectivity from these two PLLs to the global and regional clock networks remains the same as shown.

(2) If the design uses the feedback input, you will lose one (or two, if FBIN is differential) external clock output pin.

These dedicated circuits combined, with enhanced PLL clocking and phase-shift ability, provide a complete hardware solution for interfacing to high-speed memory.

For more information on external memory interfaces, refer to the *External Memory Interfaces in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook*.

Programmable Drive Strength

The output buffer for each Stratix II GX device I/O pin has a programmable drive strength control for certain I/O standards. The LVTTL, LVCMOS, SSTL, and HSTL standards have several levels of drive strength that you can control. The default setting used in the Quartus II software is the maximum current strength setting that is used to achieve maximum I/O performance. For all I/O standards, the minimum setting is the lowest drive strength that guarantees the I_{OH}/I_{OL} of the standard. Using minimum settings provides signal slew rate control to reduce system noise and signal overshoot.

Table 2–37. Supported TDO/TDI Voltage Combinations (Part 2 of 2)

Device	TDI Input Buffer Power	Stratix II GX TDO V_{CCIO} Voltage Level in I/O Bank 4				
		V_{CCIO} = 3.3 V	V_{CCIO} = 2.5 V	V_{CCIO} = 1.8 V	V_{CCIO} = 1.5 V	V_{CCIO} = 1.2 V
Non-Stratix II GX	VCC = 3.3 V	✓ (1)	✓ (2)	✓ (3)	Level shifter required	Level shifter required
	VCC = 2.5 V	✓ (1), (4)	✓ (2)	✓ (3)	Level shifter required	Level shifter required
	VCC = 1.8 V	✓ (1), (4)	✓ (2), (5)	✓	Level shifter required	Level shifter required
	VCC = 1.5 V	✓ (1), (4)	✓ (2), (5)	✓ (6)	✓	✓

Notes to Table 2–37:

(1) The TDO output buffer meets V_{OH} (MIN) = 2.4 V.
(2) The TDO output buffer meets V_{OH} (MIN) = 2.0 V.
(3) An external 250-Ω pull-up resistor is not required, but recommended if signal levels on the board are not optimal.
(4) Input buffer must be 3.3-V tolerant.
(5) Input buffer must be 2.5-V tolerant.
(6) Input buffer must be 1.8-V tolerant.

High-Speed Differential I/O with DPA Support

Stratix II GX devices contain dedicated circuitry for supporting differential standards at speeds up to 1 Gbps. The LVDS differential I/O standards are supported in the Stratix II GX device. In addition, the LVPECL I/O standard is supported on input and output clock pins on the top and bottom I/O banks.

The high-speed differential I/O circuitry supports the following high-speed I/O interconnect standards and applications:

- SPI-4 Phase 2 (POS-PHY Level 4)
- SFI-4
- Parallel RapidIO standard

There are two dedicated high-speed PLLs in the EP2SGX30 device and four dedicated high-speed PLLs in the EP2SGX60, EP2SGX90, and EP2SGX130 devices to multiply reference clocks and drive high-speed differential SERDES channels.

Tables 2–38 through 2–41 show the number of channels that each Fast PLL can clock in each of the Stratix II GX devices. In Tables 2–38 through 2–41, the first row for each transmitter or receiver provides the number of channels driven directly by the PLL. The second row below it shows the maximum channels a Fast PLL can drive if cross bank channels are used from the adjacent center Fast PLL. For example, in the 780-pin FineLine BGA EP2SGX30 device, PLL 1 can drive a maximum of

Figure 4–1 shows the lock time parameters in manual mode, Figure 4–2 shows the lock time parameters in automatic mode.

LTD = Lock to data
LTR = Lock to reference clock

Figure 4–1. Lock Time Parameters for Manual Mode

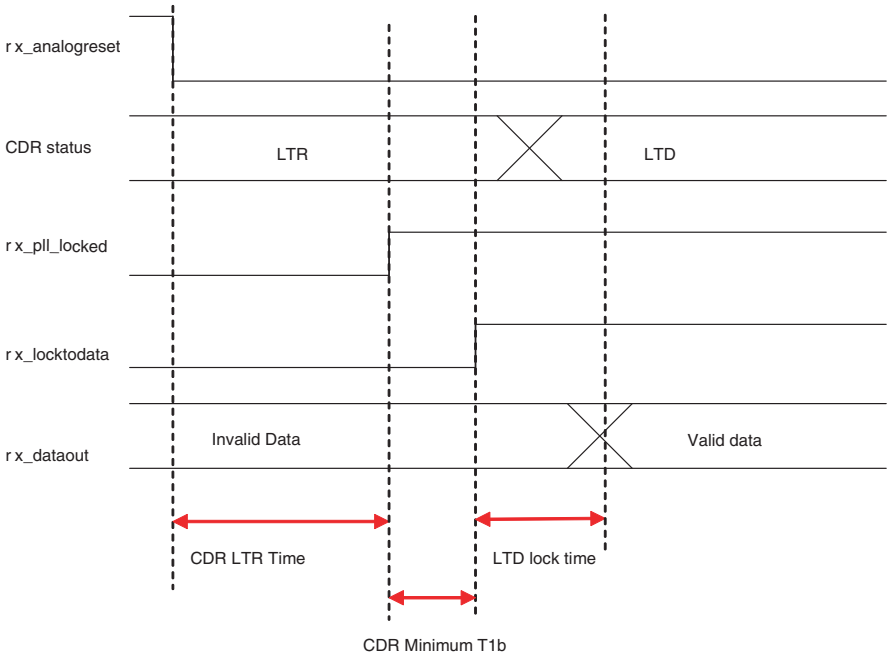


Figure 4–4. Transmitter Output Waveform

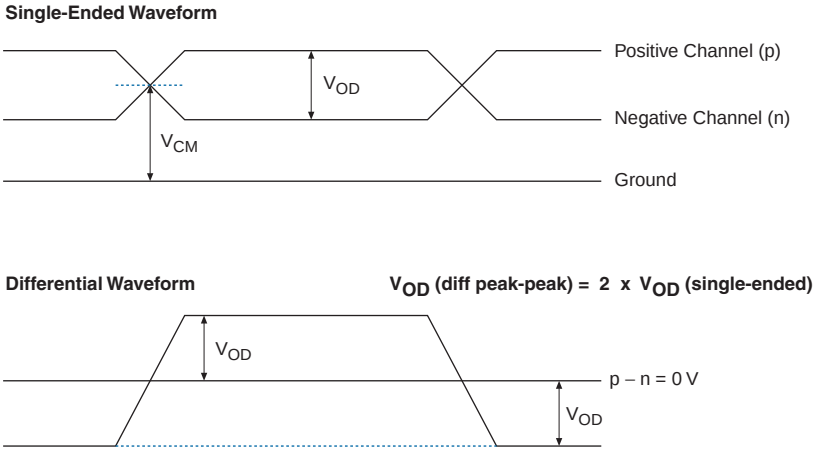
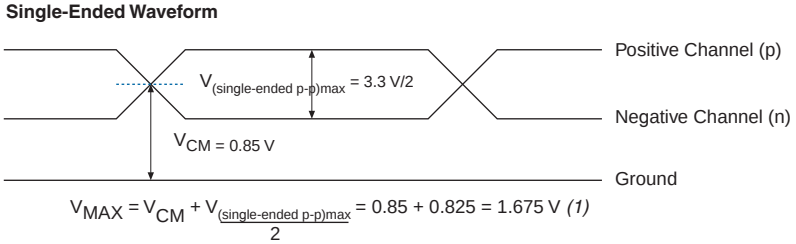


Figure 4–5. Maximum Receiver Input Pin Voltage



Note to Figure 4–5:
(1) The absolute V_{MAX} that the receiver input pins can tolerate is 2 V.

Tables 4–7 through 4–12 show the typical V_{OD} for data rates from 600 Mbps to 6.375 Gbps. The specification is for measurement at the package ball.

Table 4–7. Typical V_{OD} Setting, TX Term = 100 Ω Note (1)

V_{CCH} TX = 1.5 V	V_{OD} Setting (mV)						
	200	400	600	800	1000	1200	1400
V_{OD} Typical (mV)	220	430	625	830	1020	1200	1350

Note to Table 4–7:
(1) Applicable to data rates from 600 Mbps to 6.375 Gbps. Specification is for measurement at the package ball.

Table 4–13. Typical Pre-Emphasis (First Post-Tap), Note (1) (Part 2 of 2)

V_{CCH} TX = 1.5 V	First Post Tap Pre-Emphasis Level											
V_{OD} Setting (mV)	1	2	3	4	5	6	7	8	9	10	11	12
1400				20%	26%	33%	41%	51%	58%	67%	77%	86%

Note to Table 4–13:
(1) Applicable to data rates from 600 Mbps to 6.375 Gbps. Specification is for measurement at the package ball.

Table 4–14. Typical Pre-Emphasis (First Post-Tap), Note (1)

V_{CCH} TX = 1.5 V	First Post Tap Pre-Emphasis Level											
V_{OD} Setting (mV)	1	2	3	4	5	6	7	8	9	10	11	12
	TX Term = 120 Ω											
240	45%											
480		41%	76%	114%	166%	257%	355%					
720		23%	38%	55%	84%	108%	137%	179%	226%	280%	405%	477%
960		15%	24%	36%	47%	64%	80%	97%	122%	140%	170%	196%
1200			18%	22%	30%	41%	51%	63%	77%	86%	98%	116%

Note to Table 4–14:
(1) Applicable to data rates from 600 Mbps to 6.375 Gbps. Specification is for measurement at the package ball.

Table 4–15. Typical Pre-Emphasis (First Post-Tap), Note (1) (Part 1 of 2)

V_{CCH} TX = 1.5 V	First Post Tap Pre-Emphasis Level											
V_{OD} Setting (mV)	1	2	3	4	5	6	7	8	9	10	11	12
	TX Term = 150 Ω											
300	32%	85%										

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 10 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Sinusoidal Jitter Tolerance (peak-to-peak)	Jitter Frequency = 1.875 MHz Data Rate = 3.75 Gbps REFCLK = 187.5 MHz Pattern = CJPAT No Equalization DC Gain = 3 dB	> 0.1			-			-			UI
	Jitter Frequency = 20 MHz Data Rate = 3.75 Gbps REFCLK = 187.5 MHz Pattern = CJPAT No Equalization DC Gain = 3 dB	> 0.1			-			-			UI
(OIF) CEI Transmitter Jitter Generation *(14)*											
Total Jitter (peak-to-peak)	Data Rate = 6.375 Gbps REFCLK = 318.75 MHz Pattern = PRBS15 Vod=1000 mV *(5)* No Pre-emphasis BER = 10^{-12}			0.3			N/A			N/A	UI
(OIF) CEI Receiver Jitter Tolerance *(14)*											
Deterministic Jitter Tolerance (peak-to-peak)	Data Rate = 6.375 Gbps Pattern = PRBS31 Equalizer Setting = 15 DC Gain = 0 dB BER = 10^{-12}	> 0.675			N/A			N/A			UI

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 11 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Combined Deterministic and Random Jitter Tolerance (peak-to-peak)	Data Rate = 6.375 Gbps Pattern = PRBS31 Equalizer Setting = 15 DC Gain = 0 dB BER = 10^{-12}	> 0.988			N/A			N/A			UI
Sinusoidal Jitter Tolerance (peak-to-peak)	Jitter Frequency = 38.2 KHz Data Rate = 6.375 Gbps Pattern = PRBS31 Equalizer Setting = 15 DC Gain = 0 dB BER = 10^{-12}	> 5			N/A			N/A			UI
	Jitter Frequency = 3.82 MHz Data Rate=6.375 Gbps Pattern = PRBS31 Equalizer Setting = 15 DC Gain = 0 dB BER = 10^{-12}	> 0.05			N/A			N/A			UI
	Jitter Frequency = 20 MHz Data Rate = 6.375 Gbps Pattern = PRBS31 Equalizer Setting = 15 DC Gain = 0 dB BER = 10^{-12}	> 0.05			N/A			N/A			UI

Table 4–29. 2.5-V LVDS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage for left and right I/O banks (1, 2, 5, and 6)		2.375	2.5	2.625	V
V_{ID}	Input differential voltage swing (single-ended)		100	350	900	mV
V_{ICM}	Input common mode voltage		200	1,250	1,800	mV
V_{OD}	Output differential voltage (single-ended)	R_L = 100 Ω	250		450	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	1.125		1.375	V
R_L	Receiver differential input discrete resistor (external to Stratix II GX devices)		90	100	110	Ω

Table 4–30. 3.3-V LVDS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO} *(1)*	I/O supply voltage for top and bottom PLL banks (9, 10, 11, and 12)		3.135	3.3	3.465	V
V_{ID}	Input differential voltage swing (single-ended)		100	350	900	mV
V_{ICM}	Input common mode voltage		200	1,250	1,800	mV
V_{OD}	Output differential voltage (single-ended)	R_L = 100 Ω	250		710	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	840		1,570	mV
R_L	Receiver differential input discrete resistor (external to Stratix II GX devices)		90	100	110	Ω

Note to Table 4–30:

(1) The top and bottom clock input differential buffers in I/O banks 3, 4, 7, and 8 are powered by V_{CCINT}, not V_{CCIO}. The PLL clock output/feedback differential buffers are powered by VCC_PLL_OUT. For differential clock output/feedback operation, connect VCC_PLL_OUT to 3.3 V.

EP2SGX90 Clock Timing Parameters

Tables 4–71 through 4–74 show the maximum clock timing parameters for EP2SGX90 devices.

Table 4–71. EP2SGX90 Column Pins Global Clock Timing Parameters

Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.861	1.878	3.115	3.465	4.143	ns
t_{COUT}	1.696	1.713	2.873	3.195	3.819	ns
t_{PLLCIN}	-0.254	-0.237	0.171	0.179	0.206	ns
$t_{PLLCOUT}$	-0.419	-0.402	-0.071	-0.091	-0.118	ns

Table 4–72. EP2SGX90 Row Pins Global Clock Timing Parameters

Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.634	1.650	2.768	3.076	3.678	ns
t_{COUT}	1.639	1.655	2.764	3.072	3.673	ns
t_{PLLCIN}	-0.481	-0.465	-0.189	-0.223	-0.279	ns
$t_{PLLCOUT}$	-0.476	-0.46	-0.193	-0.227	-0.284	ns

Table 4–73. EP2SGX90 Column Pins Regional Clock Timing Parameters

Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.688	1.702	2.896	3.224	3.856	ns
t_{COUT}	1.551	1.569	2.893	3.220	3.851	ns
t_{PLLCIN}	-0.105	-0.089	0.224	0.241	0.254	ns
$t_{PLLCOUT}$	-0.27	-0.254	0.224	0.241	0.254	ns

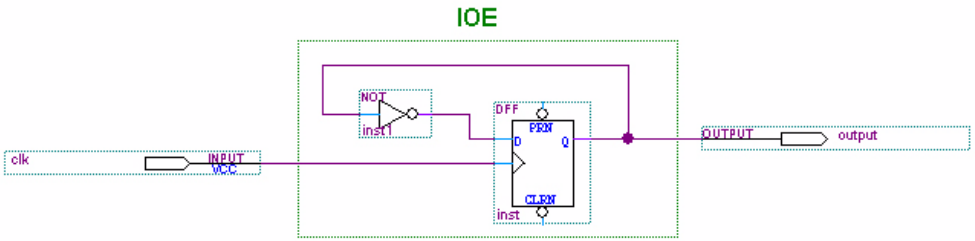
Table 4–84. Stratix II GX I/O Input Delay for Column Pins (Part 2 of 3)

I/O Standard	Parameter	Fast Corner Industrial/ Commercial	-3 Speed Grade *(2)*	-3 Speed Grade *(3)*	-4 Speed Grade	-5 Speed Grade	Unit
2.5 V	t_{PI}	717	1210	1269	1349	1619	ps
	t_{PCOUT}	438	774	812	863	1036	ps
1.8 V	t_{PI}	783	1366	1433	1523	1829	ps
	t_{PCOUT}	504	930	976	1037	1246	ps
1.5 V	t_{PI}	786	1436	1506	1602	1922	ps
	t_{PCOUT}	507	1000	1049	1116	1339	ps
LVCMOS	t_{PI}	707	1223	1282	1364	1637	ps
	t_{PCOUT}	428	787	825	878	1054	ps
SSTL-2 Class I	t_{PI}	530	818	857	912	1094	ps
	t_{PCOUT}	251	382	400	426	511	ps
SSTL-2 Class II	t_{PI}	530	818	857	912	1094	ps
	t_{PCOUT}	251	382	400	426	511	ps
SSTL-18 Class I	t_{PI}	569	898	941	1001	1201	ps
	t_{PCOUT}	290	462	484	515	618	ps
SSTL-18 Class II	t_{PI}	569	898	941	1001	1201	ps
	t_{PCOUT}	290	462	484	515	618	ps
1.5-V HSTL Class I	t_{PI}	587	993	1041	1107	1329	ps
	t_{PCOUT}	308	557	584	621	746	ps
1.5-V HSTL Class II	t_{PI}	587	993	1041	1107	1329	ps
	t_{PCOUT}	308	557	584	621	746	ps
1.8-V HSTL Class I	t_{PI}	569	898	941	1001	1201	ps
	t_{PCOUT}	290	462	484	515	618	ps
1.8-V HSTL Class II	t_{PI}	569	898	941	1001	1201	ps
	t_{PCOUT}	290	462	484	515	618	ps
PCI	t_{PI}	712	1214	1273	1354	1625	ps
	t_{PCOUT}	433	778	816	868	1042	ps
PCI-X	t_{PI}	712	1214	1273	1354	1625	ps
	t_{PCOUT}	433	778	816	868	1042	ps
Differential SSTL-2 Class I *(1)*	t_{PI}	530	818	857	912	1094	ps
	t_{PCOUT}	251	382	400	426	511	ps

Table 4–97. Maximum Output Clock Toggle Rate Derating Factors (Part 2 of 5)

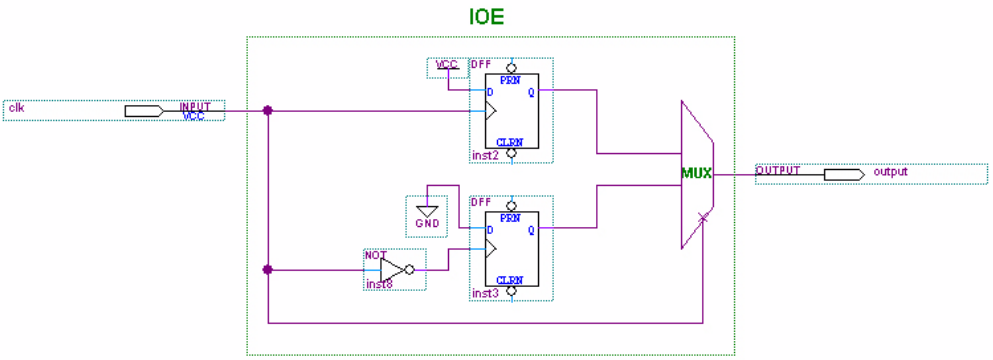
I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate Derating Factors (ps/pF)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		-3	-4	-5	-3	-4	-5	-3	-4	-5
3.3-V LVCMOS	4 mA	377	391	391	377	391	391	377	391	391
	8 mA	206	212	212	206	212	212	178	212	212
	12 mA	141	145	145	-	-	-	115	145	145
	16 mA	108	111	111	-	-	-	86	111	111
	20 mA	83	88	88	-	-	-	79	88	88
	24 mA	65	72	72	-	-	-	74	72	72
2.5-V LVTTL/ LVCMOS	4 mA	387	427	427	387	427	427	391	427	427
	8 mA	163	224	224	163	224	224	170	224	224
	12 mA	142	203	203	142	203	203	152	203	203
	16 mA	120	182	182	-	-	-	134	182	182
1.8-V LVTTL/ LVCMOS	2 mA	951	1,421	1,421	951	1,421	1,421	904	1,421	1,421
	4 mA	405	516	516	405	516	516	393	516	516
	6 mA	261	325	325	261	325	325	253	325	325
	8 mA	223	274	274	223	274	274	224	274	274
	10 mA	194	236	236	-	-	-	199	236	236
	12 mA	174	209	209	-	-	-	180	209	209
1.5-V LVTTL/ LVCMOS	2 mA	652	963	963	652	963	963	618	963	963
	4 mA	333	347	347	333	347	347	270	347	347
	6 mA	182	247	247	-	-	-	198	247	247
	8 mA	135	194	194	-	-	-	155	194	194
SSTL-2 Class I	8 mA	364	680	680	364	680	680	350	680	680
	12 mA	163	207	207	163	207	207	188	207	207
SSTL-2 Class II	16 mA	118	147	147	118	147	147	94	147	147
	20 mA	99	122	122	-	-	-	87	122	122
	24 mA	91	116	116	-	-	-	85	116	116
SSTL-18 Class I	4 mA	458	570	570	458	570	570	505	570	570
	6 mA	305	380	380	305	380	380	336	380	380
	8 mA	225	282	282	225	282	282	248	282	282
	10 mA	167	220	220	167	220	220	190	220	220
	12 mA	129	175	175	-	-	-	148	175	175

Figure 4–12. DCD Measurement Technique for Non-DDIO (Single-Data Rate) Outputs



However, when the output is a double data rate input/output (DDIO) signal, both edges of the input clock signal (positive and negative) trigger output transitions (Figure 4–13). Therefore, any distortion on the input clock and the input clock buffer affect the output DCD.

Figure 4–13. DCD Measurement Technique for DDIO (Double-Data Rate) Outputs



When an FPGA PLL generates the internal clock, the PLL output clocks the IOE block. As the PLL only monitors the positive edge of the reference clock input and internally re-creates the output clock signal, any DCD present on the reference clock is filtered out. Therefore, the DCD for a DDIO output with PLL in the clock path is better than the DCD for a DDIO output without PLL in the clock path.

Tables 4–98 through 4–105 show the maximum DCD in absolution derivation for different I/O standards on Stratix II GX devices. Examples are also provided that show how to calculate DCD as a percentage.

Table 4–98. Maximum DCD for Non-DDIO Output on Row I/O Pins

Row I/O Output Standard	Maximum DCD (ps) for Non-DDIO Output		
	-3 Devices	-4 and -5 Devices	Unit
3.3-V LVTTTL	245	275	ps
3.3-V LVCMOS	125	155	ps
2.5 V	105	135	ps
1.8 V	180	180	ps
1.5-V LVCMOS	165	195	ps
SSTL-2 Class I	115	145	ps
SSTL-2 Class II	95	125	ps
SSTL-18 Class I	55	85	ps
1.8-V HSTL Class I	80	100	ps
1.5-V HSTL Class I	85	115	ps
LVDS	55	80	ps

Here is an example for calculating the DCD as a percentage for a non-DDIO output on a row I/O on a -3 device:

If the non-DDIO output I/O standard is SSTL-2 Class II, the maximum DCD is 95 ps (see Table 4–99). If the clock frequency is 267 MHz, the clock period T is:

T = 1/ f = 1 / 267 MHz = 3.745 ns = 3,745 ps

To calculate the DCD as a percentage:

(T/2 – DCD) / T = (3,745 ps/2 – 95 ps) / 3,745 ps = 47.5% (for low boundary)

(T/2 + DCD) / T = (3,745 ps/2 + 95 ps) / 3,745 ps = 52.5% (for high boundary)