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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

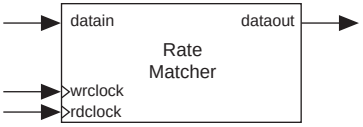
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 3022 |
| Number of Logic Elements/Cells | 60440 |
| Total RAM Bits | 2544192 |
| Number of I/O | 534 |
| Number of Gates | - |
| Voltage - Supply | 1.15V ~ 1.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 1152-BBGA |
| Supplier Device Package | 1152-FBGA (35x35) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/ep2sgx60ef1152c3n |

### *Rate Matcher*

Rate matcher is available in Basic, PCI Express, XAUI, and GIGE modes and consists of a 20-word deep FIFO buffer and a FIFO controller. Figure 2–20 shows the implementation of the rate matcher in the Stratix II GX device.

***Figure 2–20. Rate Matcher***




In a multi-crystal environment, the rate matcher compensates for up to a ± 300-PPM difference between the source and receiver clocks. Table 2–8 shows the standards supported and the PPM for the rate matcher tolerance.

***Table 2–8. Rate Matcher PPM Support*** *Note (1)*

| Standard | PPM |
|---|---|
| XAUI | ± 100 |
| PCI Express (PIPE) | ± 300 |
| GIGE | ± 100 |
| Basic Double-Width | ± 300 |

***Note to Table 2–8:***

(1) Refer to the *Stratix II GX Transceiver User Guide* for the Altera®-defined scheme.

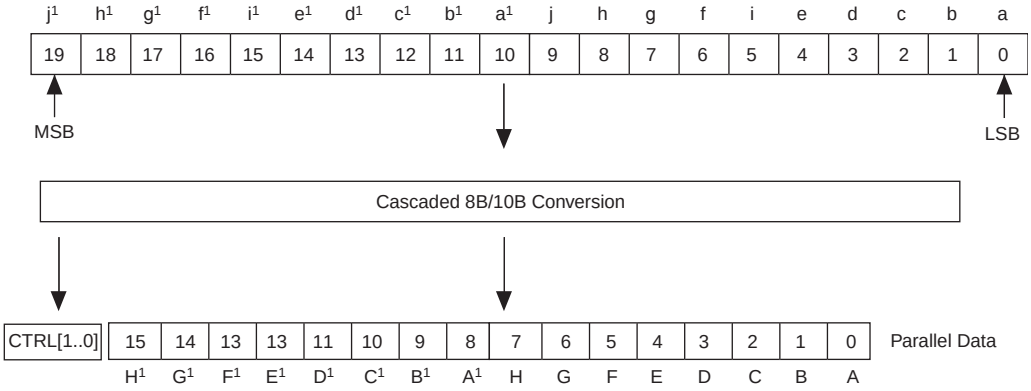
**Basic Mode**

In Basic mode, you can program the skip and control pattern for rate matching. In single-width Basic mode, there is no restriction on the deletion of a skip character in a cluster. The rate matcher deletes the skip characters as long as they are available. For insertion, the rate matcher inserts skip characters such that the number of skip characters at the output of rate matcher does not exceed five. In double-width mode, the rate matcher deletes skip character when they appear as pairs in the upper and lower bytes. There are no restrictions on the number of skip characters that are deleted. The rate matcher inserts skip characters as pairs.

asserted. All 8B/10B control signals, such as disparity error or control detect, are pipelined with the data in the Stratix II GX receiver block and are edge aligned with the data.

Figure 2–23 shows how the 20-bit code is decoded to the 16-bit data + 2-bit control indicator.

*Figure 2–23. 20-Bit to 16-Bit Decoding Process*




There are two optional error status ports available in the 8B/10B decoder, `rx_errdetect` and `rx_disperr`. These status signals are aligned with the code group in which the error occurred.

### *Receiver State Machine*

The receiver state machine operates in Basic, GIGE, PCI Express, and XAUI modes. In GIGE mode, the receiver state machine replaces invalid code groups with K30.7. In XAUI mode, the receiver state machine translates the XAUI PCS code group to the XAUI XGMII code group.

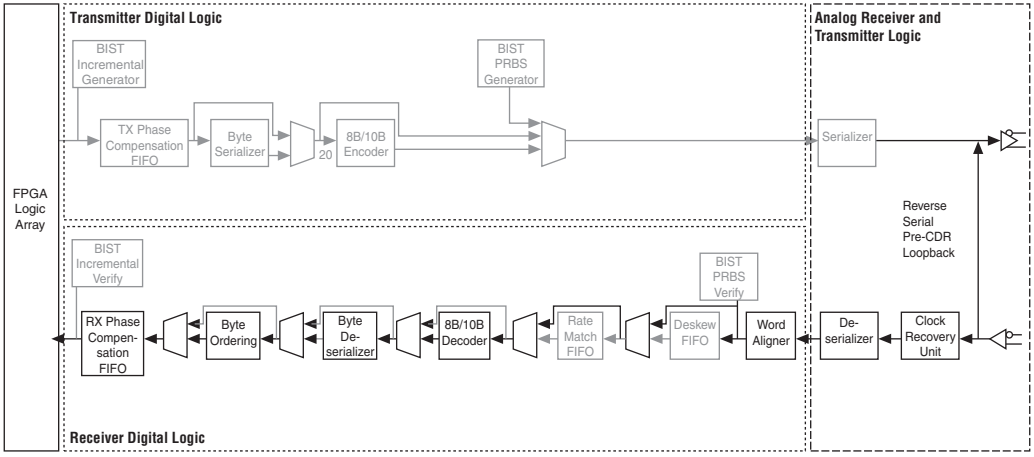
### *Byte Deserializer*

The byte deserializer widens the transceiver data path before the FPGA interface. This reduces the rate at which the received data needs to be clocked at in the FPGA logic. The byte deserializer block is available in both single- and double-width modes.

The byte deserializer converts the one- or two-byte interface into a two- or four-byte-wide data path from the transceiver to the FPGA logic (see Table 2–9). The FPGA interface has a limit of 250 MHz, so the byte deserializer is needed to widen the bus width at the FPGA interface and

Figure 2–27 show the Stratix II GX block in reverse serial pre-CDR loopback mode.

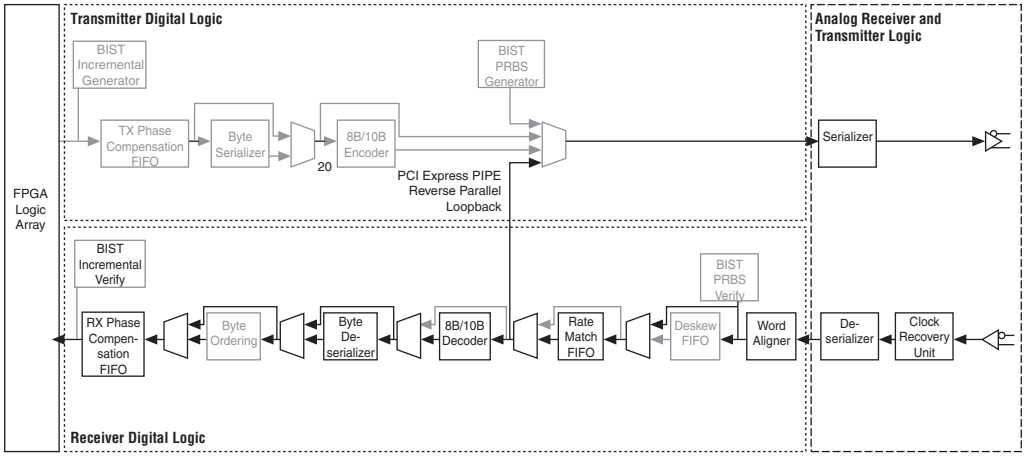
*Figure 2–27. Stratix II GX Block in Reverse Serial Pre-CDR Loopback Mode*




### *PCI Express PIPE Reverse Parallel Loopback*

This loopback mode, available only in PIPE mode, can be dynamically enabled by the `tx_detectrxloopback` port of the PIPE interface. Figure 2–28 shows the datapath for this mode.

*Figure 2–28. Stratix II GX Block in PCI Express PIPE Reverse Parallel Loopback Mode*



Figures 2–57 shows one of the columns with surrounding LAB rows.

*Figure 2–57. DSP Blocks Arranged in Columns*

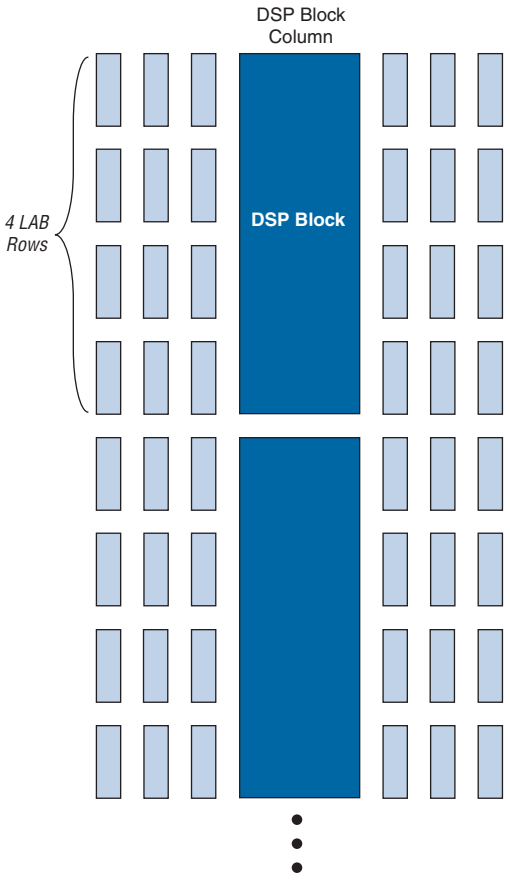
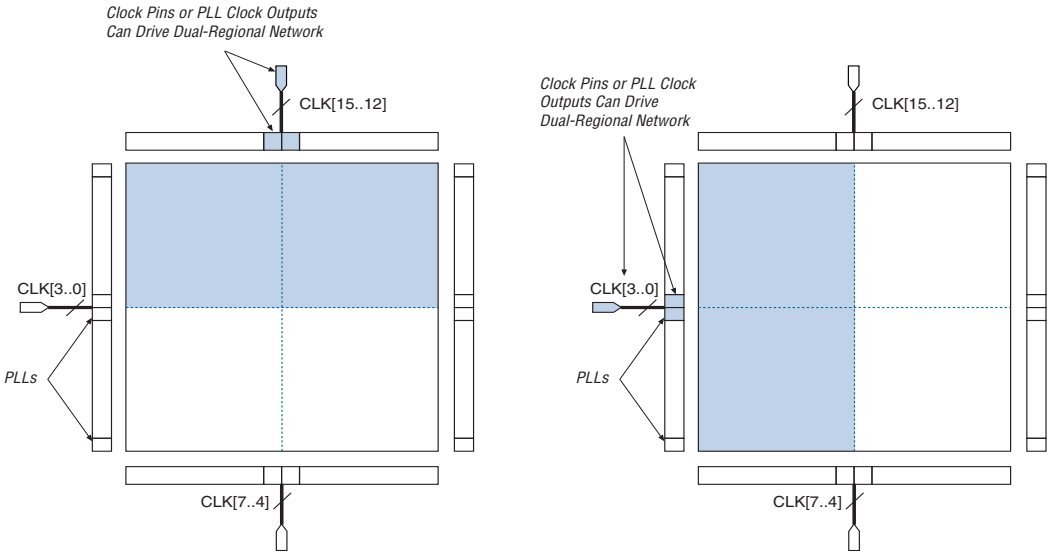


*Figure 2–63. Dual-Regional Clocks*




### Combined Resources

Within each quadrant, there are 24 distinct dedicated clocking resources consisting of 16 global clock lines and 8 regional clock lines. Multiplexers are used with these clocks to form buses to drive LAB row clocks, column IOE clocks, or row IOE clocks. Another multiplexer is used at the LAB level to select three of the six row clocks to feed the ALM registers in the LAB (see Figure 2–64).

*Figure 2–64. Hierarchical Clock Networks per Quadrant*

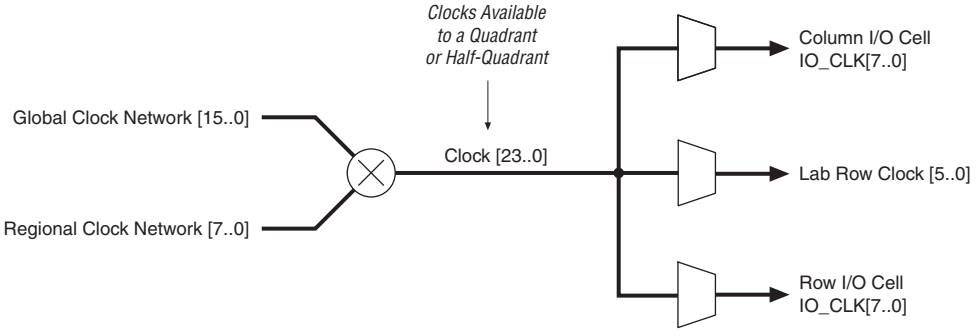
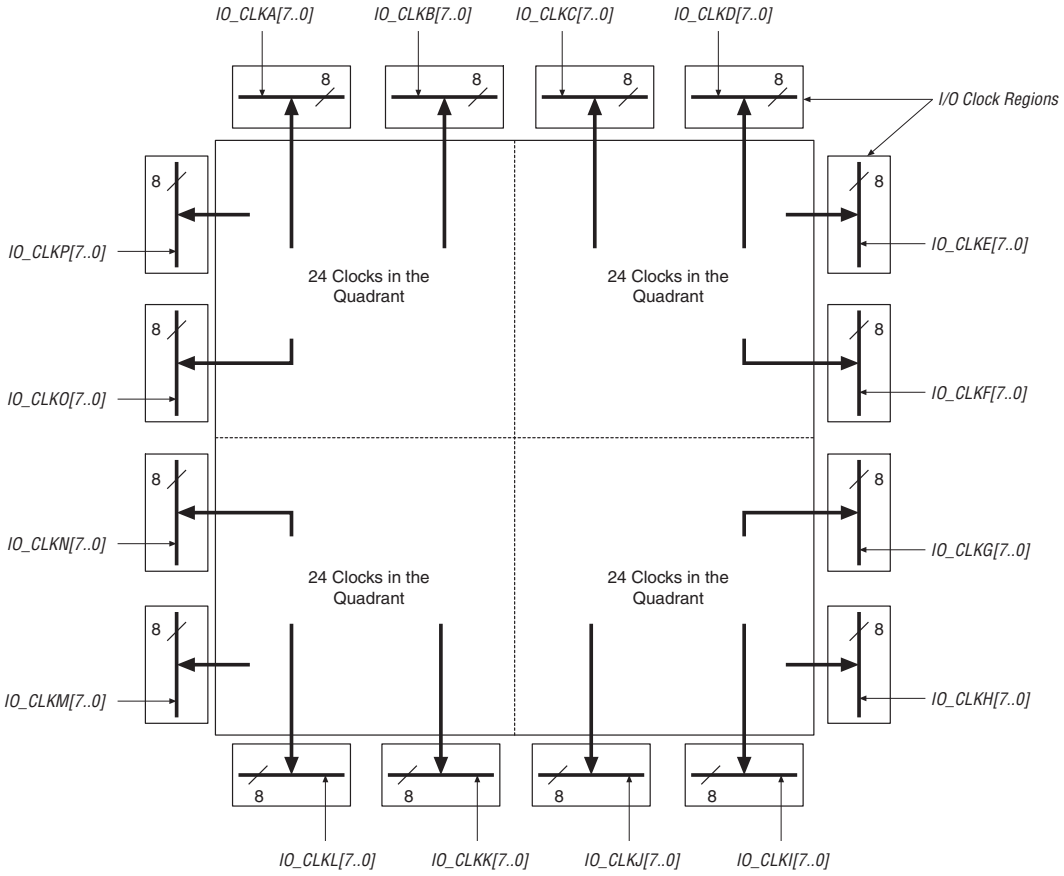


*Figure 2–66. EP2SGX60, EP2SGX90 and EP2SGX130 Device I/O Clock Groups*



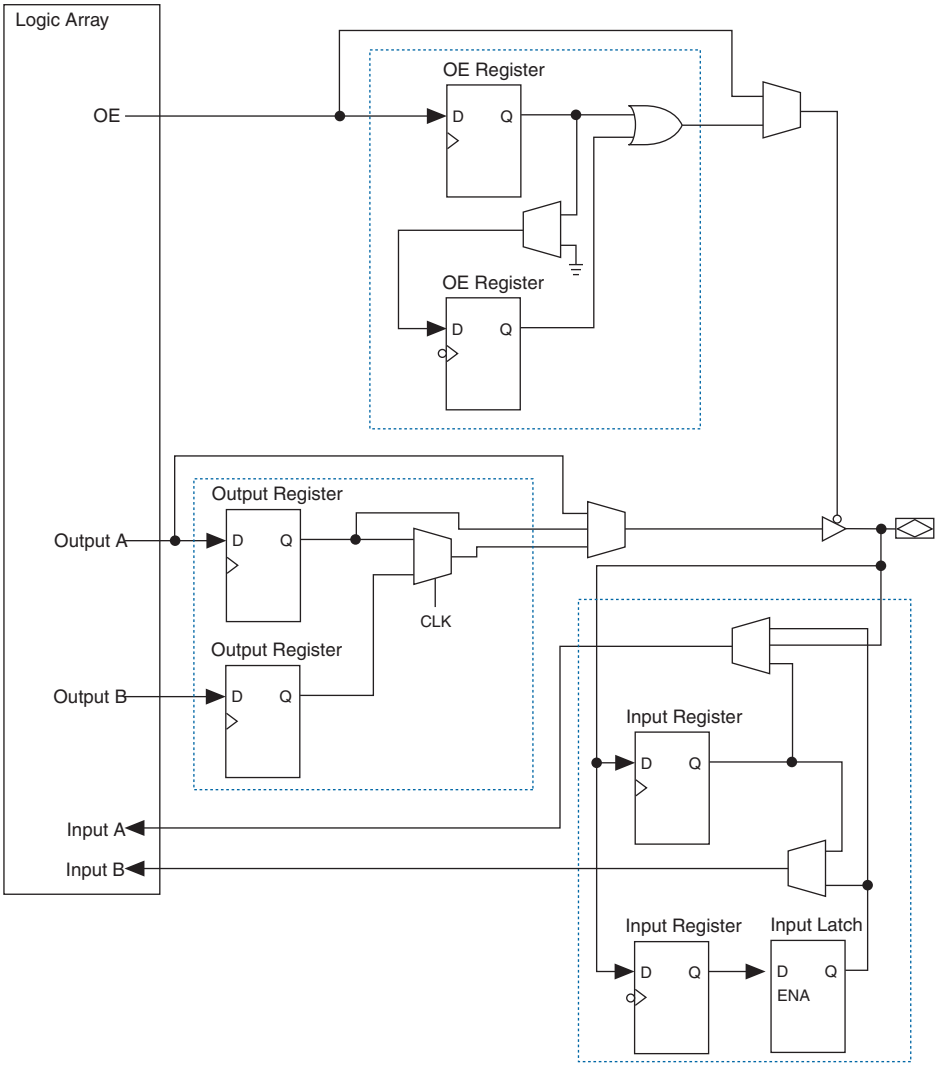

You can use the Quartus II software to control whether a clock input pin drives either a global, regional, or dual-regional clock network. The Quartus II software automatically selects the clocking resources if not specified.

### *Clock Control Block*

Each global clock, regional clock, and PLL external clock output has its own clock control block. The control block has two functions:

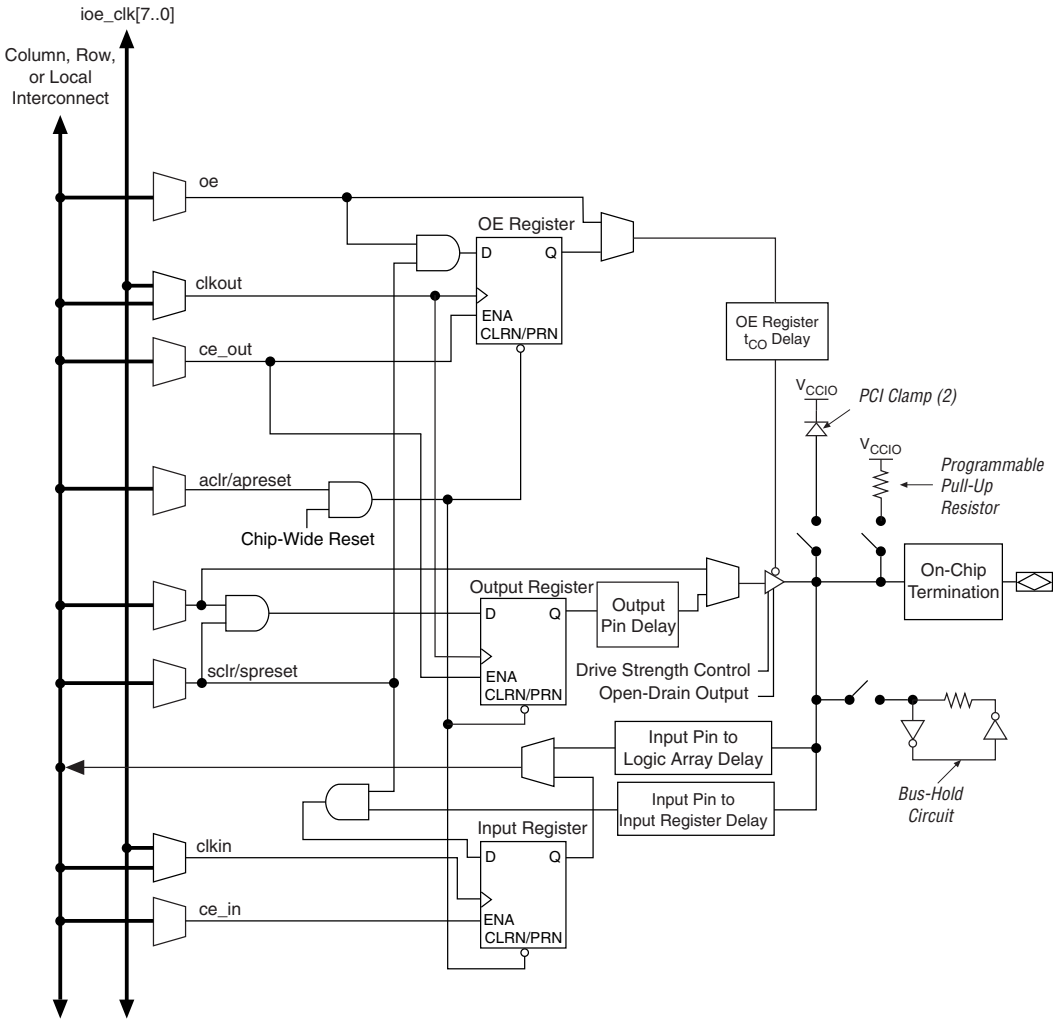
- Clock source selection (dynamic selection for global clocks)
- Clock power-down (dynamic clock enable or disable)

*Figure 2–76. Stratix II GX IOE Structure*




The IOEs are located in I/O blocks around the periphery of the Stratix II GX device. There are up to four IOEs per row I/O block and four IOEs per column I/O block. The row I/O blocks drive row, column, or direct link interconnects. The column I/O blocks drive column interconnects.

*Figure 2–81. Stratix II GX IOE in Bidirectional I/O Configuration* *Note (1)*




*Notes to Figure 2–81:*
(1) All input signals to the IOE can be inverted at the IOE.
(2) The optional PCI clamp is only available on column I/O pins.

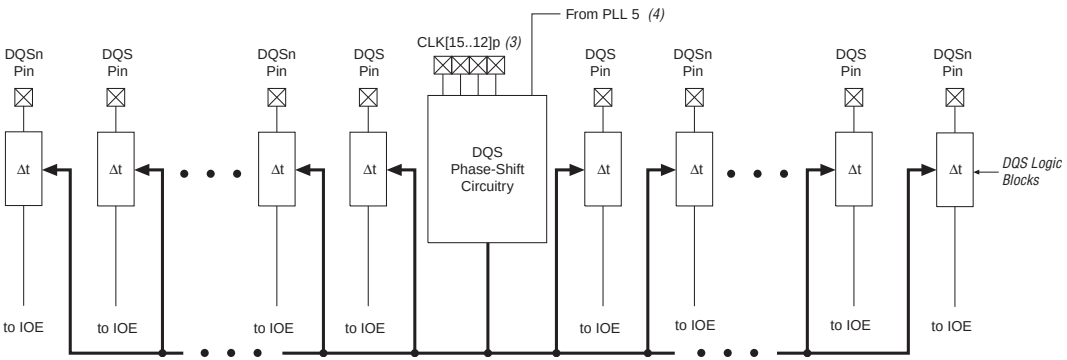
The Stratix II GX device IOE includes programmable delays that can be activated to ensure input IOE register-to-logic array register transfers, input pin-to-logic array register transfers, or output IOE register-to-pin transfers.

A compensated delay element on each DQS pin automatically aligns input DQS synchronization signals with the data window of their corresponding DQ data signals. The DQS signals drive a local DQS bus in the top and bottom I/O banks. This DQS bus is an additional resource to the I/O clocks and is used to clock DQ input registers with the DQS signal.

The Stratix II GX device has two phase-shifting reference circuits, one on the top and one on the bottom of the device. The circuit on the top controls the compensated delay elements for all DQS pins on the top. The circuit on the bottom controls the compensated delay elements for all DQS pins on the bottom.

Each phase-shifting reference circuit is driven by a system reference clock, which must have the same frequency as the DQS signal. Clock pins `CLK[15..12]p` feed the phase circuitry on the top of the device and clock pins `CLK[7..4]p` feed the phase circuitry on the bottom of the device. In addition, PLL clock outputs can also feed the phase-shifting reference circuits. Figure 2–86 shows the phase-shift reference circuit control of each DQS delay shift on the top of the device. This same circuit is duplicated on the bottom of the device.

***Figure 2–86. DQS Phase-Shift Circuitry*** *Notes (1), (2)*




*Notes to Figure 2–86:*

(1) There are up to 18 pairs of DQS and DQSn pins available on the top or the bottom of the Stratix II GX device. There are up to 10 pairs on the right side and 8 pairs on the left side of the DQS phase-shift circuitry.

(2) The "t" module represents the DQS logic block.

(3) Clock pins `CLK[15..12]p` feed the phase-shift circuitry on the top of the device and clock pins `CLK[7..4]p` feed the phase circuitry on the bottom of the device. You can also use a PLL clock output as a reference clock to the phaseshift circuitry.

(4) You can only use PLL 5 to feed the DQS phase-shift circuitry on the top of the device and PLL 6 to feed the DQS phase-shift circuitry on the bottom of the device.

Table 2–32 shows the possible settings for the I/O standards with drive strength control.

*Table 2–32. Programmable Drive Strength* *Note (1)*

| I/O Standard | $I_{OH}$ / $I_{OL}$ Current Strength Setting (mA) for Column I/O Pins | $I_{OH}$ / $I_{OL}$ Current Strength Setting (mA) for Row I/O Pins |
|---|---|---|
| 3.3-V LVTTL | 24, 20, 16, 12, 8, 4 | 12, 8, 4 |
| 3.3-V LVCMOS | 24, 20, 16, 12, 8, 4 | 8, 4 |
| 2.5-V LVTTL/LVCMOS | 16, 12, 8, 4 | 12, 8, 4 |
| 1.8-V LVTTL/LVCMOS | 12, 10, 8, 6, 4, 2 | 8, 6, 4, 2 |
| 1.5-V LVCMOS | 8, 6, 4, 2 | 4, 2 |
| SSTL-2 Class I | 12, 8 | 12, 8 |
| SSTL-2 Class II | 24, 20, 16 | 16 |
| SSTL-18 Class I | 12, 10, 8, 6, 4 | 10, 8, 6, 4 |
| SSTL-18 Class II | 20, 18, 16, 8 | — |
| HSTL-18 Class I | 12, 10, 8, 6, 4 | 12, 10, 8, 6, 4 |
| HSTL-18 Class II | 20, 18, 16 | — |
| HSTL-15 Class I | 12, 10, 8, 6, 4 | 8, 6, 4 |
| HSTL-15 Class II | 20, 18, 16 | — |

*Note to Table 2–32:*

(1) The Quartus II software default current setting is the maximum setting for each I/O standard.

## Open-Drain Output

Stratix II GX devices provide an optional open-drain (equivalent to an open collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (for example, interrupt and write enable signals) that can be asserted by any of several devices.

## Bus Hold

Each Stratix II GX device I/O pin provides an optional bus-hold feature. The bus-hold circuitry can hold the signal on an I/O pin at its last-driven state. Since the bus-hold feature holds the last-driven state of the pin until the next input signal is present, an external pull-up or pull-down resistor is not needed to hold a signal level when the bus is tri-stated.

*Table 2–41. EP2SGX130 Device Differential Channels* *Note (1)*

| Package | Transmitter/Receiver | Total Channels | Center Fast PLLs | | Corner Fast PLLs | |
|---|---|---|---|---|---|---|
| | | | PLL1 | PLL2 | PLL7 | PLL8 |
| 1508-pin FineLine BGA | Transmitter | 71 | 37 | 41 | 37 | 41 |
| | Receiver | 73 | 37 | 41 | 37 | 41 |

*Note to Tables 2–38 through 2–41:*
(1) The total number of receiver channels includes the four non-dedicated clock channels that can be optionally used as data channels.

Therefore, the total number of channels is not the addition of the number of channels accessible by PLLs 1 and 2 with the number of channels accessible by PLLs 7 and 8.

## Dedicated Circuitry with DPA Support

Stratix II GX devices support source-synchronous interfacing with LVDS signaling at up to 1 Gbps. Stratix II GX devices can transmit or receive serial channels along with a low-speed or high-speed clock.

The receiving device PLL multiplies the clock by an integer factor W = 1 through 32. The SERDES factor J determines the parallel data width to deserialize from receivers or to serialize for transmitters. The SERDES factor J can be set to 4, 5, 6, 7, 8, 9, or 10 and does not have to equal the PLL clock-multiplication W value. A design using the dynamic phase aligner also supports all of these J factor values. For a J factor of 1, the Stratix II GX device bypasses the SERDES block. For a J factor of 2, the Stratix II GX device bypasses the SERDES block, and the DDR input and output registers are used in the IOE. Figure 2–88 shows the block diagram of the Stratix II GX transmitter channel.

## Configuration Schemes

You can load the configuration data for a Stratix II GX device with one of five configuration schemes (refer to Table 3–4), chosen on the basis of the target application. You can use a configuration device, intelligent controller, or the JTAG port to configure a Stratix II GX device. A configuration device can automatically configure a Stratix II GX device at system power-up.

Multiple Stratix II GX devices can be configured in any of the five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device. Stratix II GX FPGAs offer the following:

- Configuration data decompression to reduce configuration file storage
- Design security using configuration data encryption to protect designs
- Remote system upgrades for remotely updating Stratix II GX designs

Table 3–4 summarizes which configuration features can be used in each configuration scheme.

Refer to the *Configuring Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook* for more information about configuration schemes in Stratix II GX devices.

*Table 3–4. Stratix II GX Configuration Features (Part 1 of 2)*

| Configuration Scheme | Configuration Method | Design Security | Decompression | Remote System Upgrade |
|---|---|---|---|---|
| FPP | MAX II device or microprocessor and flash device | ✓ *(1)* | ✓ *(1)* | ✓ |
| | Enhanced configuration device | | ✓ *(2)* | ✓ |
| AS | Serial configuration device | ✓ | ✓ | ✓ *(3)* |
| PS | MAX II device or microprocessor and flash device | ✓ | ✓ | ✓ |
| | Enhanced configuration device | ✓ | ✓ | ✓ |
| | Download cable *(4)* | ✓ | ✓ | |
| PPA | MAX II device or microprocessor and flash device | | | ✓ |

*Table 3–4. Stratix II GX Configuration Features (Part 2 of 2)*

| Configuration Scheme | Configuration Method | Design Security | Decompression | Remote System Upgrade |
|---|---|---|---|---|
| JTAG | Download cable *(4)* | | | |
| | MAX II device or microprocessor and flash device | | | |

*Notes for Table 3–4:*
(1) In these modes, the host system must send a DCLK that is 4× the data rate.
(2) The enhanced configuration device decompression feature is available, while the Stratix II GX decompression feature is not available.
(3) Only remote update mode is supported when using the AS configuration scheme. Local update mode is not supported.
(4) The supported download cables include the Altera USB-Blaster universal serial bus (USB) port download cable, MasterBlaster serial/USB communications cable, ByteBlaster II parallel port download cable, and the ByteBlasterMV parallel port download cable.

## Device Security Using Configuration Bitstream Encryption

Stratix II and Stratix II GX FPGAs are the industry's first FPGAs with the ability to decrypt a configuration bitstream using the AES algorithm. When using the design security feature, a 128-bit security key is stored in the Stratix II GX FPGA. To successfully configure a Stratix II GX FPGA that has the design security feature enabled, the device must be configured with a configuration file that was encrypted using the same 128-bit security key. The security key can be stored in non-volatile memory inside the Stratix II GX device. This nonvolatile memory does not require any external devices, such as a battery back up, for storage.

An encrypted configuration file is the same size as a non-encrypted configuration file. When using a serial configuration scheme such as passive serial (PS) or active serial (AS), configuration time is the same whether or not the design security feature is enabled. If the fast passive parallel (FPP) scheme is used with the design security or decompression feature, a 4× DCLK is required. This results in a slower configuration time when compared to the configuration time of an FPGA that has neither the design security nor the decompression feature enabled. For more information about this feature, contact an Altera sales representative.

## Device Configuration Data Decompression

Stratix II GX FPGAs support decompression of configuration data, which saves configuration memory space and time. This feature allows you to store compressed configuration data in configuration devices or other

*Table 4–5. Stratix II GX Transceiver Block Operating Conditions*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CCA}$ | Transceiver block supply voltage | Commercial and industrial | 3.135 | 3.3 | 3.465 | V |
| $V_{CCP}$ | Transceiver block supply voltage | Commercial and industrial | 1.15 | 1.2 | 1.25 | V |
| $V_{CCR}$ | Transceiver block supply voltage | Commercial and industrial | 1.15 | 1.2 | 1.25 | V |
| $V_{CCT}$ | Transceiver block supply voltage | Commercial and industrial | 1.15 | 1.2 | 1.25 | V |
| $V_{CCT\_B}$ | Transceiver block supply voltage | Commercial and industrial | 1.15 | 1.2 | 1.25 | V |
| $V_{CCL}$ | Transceiver block supply voltage | Commercial and industrial | 1.15 | 1.2 | 1.25 | V |
| $V_{CCH\_B}$ *(2)* | Transceiver block supply voltage | Commercial and industrial | 1.15 | 1.2 | 1.25 | V |
| | | | 1.425 | 1.5 | 1.575 | V |
| $R_{REF}$ *(1)* | Reference resistor | Commercial and industrial | 2000 –1% | 2000 | 2000 +1% | Ω |

*Notes to Table 4–5:*
(1) The DC signal on this pin must be as clean as possible. Ensure that no noise is coupled to this pin.
(2) Refer to the *Stratix II GX Device Handbook*, volume 2, for more information.

*Table 4–6. Stratix II GX Transceiver Block AC Specification (Part 1 of 6)*

| Symbol / Description | Conditions | -3 Speed Commercial Speed Grade | | | -4 Speed Commercial and Industrial Speed Grade | | | -5 Speed Commercial Speed Grade | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| **Reference clock** | | | | | | | | | | | |
| Input frequency from REFCLK input | | 50 | - | 622.08 | 50 | - | 622.08 | 50 | - | 622.08 | MHz |
| Input frequency from PLD input | | 50 | - | 325 | 50 | - | 325 | 50 | - | 325 | MHz |
| Input clock jitter | | Refer to Table 4–20 on page 4–36 for the input jitter specifications for the reference clock. | | | | | | | | | |
| Absolute $V_{MAX}$ for a REFCLK pin *(12)* | | - | - | 3.3 | - | - | 3.3 | - | - | 3.3 | V |

*Table 4–32. LVPECL Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ *(1)* | I/O supply voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{ID}$ | Input differential voltage swing (single-ended) | | 300 | 600 | 1,000 | mV |
| $V_{ICM}$ | Input common mode voltage | | 1.0 | | 2.5 | V |
| $V_{OD}$ | Output differential voltage (single-ended) | $R_L$ = 100 Ω | 525 | | 970 | mV |
| $V_{OCM}$ | Output common mode voltage | $R_L$ = 100 Ω | 1,650 | | 2,250 | mV |
| $R_L$ | Receiver differential input resistor | | 90 | 100 | 110 | Ω |

*Note to Table 4–32:*

(1) The top and bottom clock input differential buffers in I/O banks 3, 4, 7, and 8 are powered by $V_{CCINT}$, not $V_{CCIO}$. The PLL clock output/feedback differential buffers are powered by VCC_PLL_OUT. For differential clock output/feedback operation, connect VCC_PLL_OUT to 3.3 V.

*Table 4–33. 3.3-V PCI Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 3.0 | 3.3 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | 0.5 $V_{CCIO}$ | | $V_{CCIO}$ + 0.5 | V |
| $V_{IL}$ | Low-level input voltage | | –0.3 | | 0.3 $V_{CCIO}$ | V |
| $V_{OH}$ | High-level output voltage | $I_{OUT}$ = –500 µA | 0.9 $V_{CCIO}$ | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OUT}$ = 1,500 µA | | | 0.1 $V_{CCIO}$ | V |

*Table 4–34. PCI-X Mode 1 Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 3.0 | | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | 0.5 $V_{CCIO}$ | | $V_{CCIO}$ + 0.5 | V |
| $V_{IL}$ | Low-level input voltage | | –0.3 | | 0.35 $V_{CCIO}$ | V |
| $V_{IPU}$ | Input pull-up voltage | | 0.7 $V_{CCIO}$ | | | V |
| $V_{OH}$ | High-level output voltage | $I_{OUT}$ = –500 µA | 0.9 $V_{CCIO}$ | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OUT}$ = 1,500 µA | | | 0.1 $V_{CCIO}$ | V |

Final timing numbers are based on actual device operation and testing. These numbers reflect the actual performance of the device under worst-case voltage and junction temperature conditions.

*Table 4–52. Stratix II GX Device Timing Model Status*

| Device | Preliminary | Final |
|---|---|---|
| EP2SGX30 | | ✓ |
| EP2SGX60 | | ✓ |
| EP2SGX90 | | ✓ |
| EP2SGX130 | | ✓ |

## I/O Timing Measurement Methodology

Different I/O standards require different baseline loading techniques for reporting timing delays. Altera characterizes timing delays with the required termination for each I/O standard and with 0 pF (except for PCI and PCI-X which use 10 pF) loading and the timing is specified up to the output pin of the FPGA device. The Quartus II software calculates the I/O timing for each I/O standard with a default baseline loading as specified by the I/O standards.

The following measurements are made during device characterization. Altera measures clock-to-output delays ($t_{CO}$) at worst-case process, minimum voltage, and maximum temperature (PVT) for default loading conditions shown in Table 4–53. Use the following equations to calculate clock pin to output pin timing for Stratix II GX devices.

$t_{CO}$ from clock pin to I/O pin = delay from clock pad to I/O output register + IOE output register clock-to-output delay + delay from output register to output pin + I/O output delay

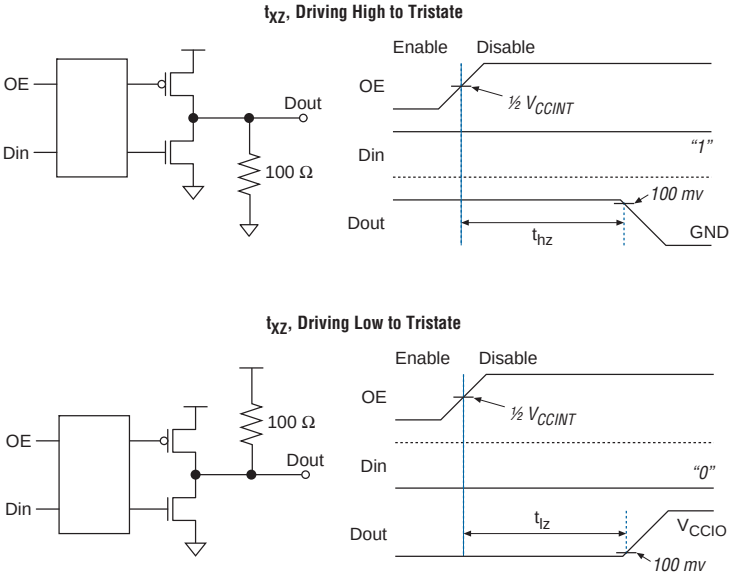
$t_{xz}/t_{zx}$ from clock pin to I/O pin = delay from clock pad to I/O output register + IOE output register clock-to-output delay + delay from output register to output pin + I/O output delay + output enable pin delay

Simulation using IBIS models is required to determine the delays on the PCB traces in addition to the output pin delay timing reported by the Quartus II software and the timing model in the device handbook.

1. Simulate the output driver of choice into the generalized test setup, using values from Table 4–53.
2. Record the time to $V_{MEAS}$.

Figures 4–9 and 4–10 show the measurement setup for output disable and output enable timing.

***Figure 4–9. Measurement Setup for $t_{xz}$*** *Note (1)*




***Note to Figure 4–9:***

(1) $V_{CCINT}$ is 1.12 V for this measurement.

*Table 4–59. M512 Block Internal Timing Microparameters (Part 2 of 2)*

| Symbol | Parameter | -3 Speed Grade (2) | | -3 Speed Grade (3) | | -4 Speed Grade | | -5 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{M512CLR}$ | Minimum clear pulse width | 144 | | 151 | | 160 | | 192 | | ps |

(1) The M512 block $f_{MAX}$ obtained using the Quartus II software does not necessarily equal to 1/TM512RC.
(2) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
(3) This column refers to –3 speed grades for EP2SGX130 devices.

*Table 4–60. M4K Block Internal Timing Microparameters (Part 1 of 2)* *Note (1)*

| Symbol | Parameter | -3 Speed Grade (2) | | -3 Speed Grade (3) | | -4 Speed Grade | | -5 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{M4KRC}$ | Synchronous read cycle time | 1462 | 2240 | 1462 | 2351 | 1462 | 2500 | 1462 | 3000 | ps |
| $t_{M4KWERESU}$ | Write or read enable setup time before clock | 22 | | 23 | | 24 | | 29 | | ps |
| $t_{M4KWEREH}$ | Write or read enable hold time after clock | 203 | | 213 | | 226 | | 272 | | ps |
| $t_{M4KBESU}$ | Byte enable setup time before clock | 22 | | 23 | | 24 | | 29 | | ps |
| $t_{M4KBEH}$ | Byte enable hold time after clock | 203 | | 213 | | 226 | | 272 | | ps |
| $t_{M4KDATAASU}$ | A port data setup time before clock | 22 | | 23 | | 24 | | 29 | | ps |
| $t_{M4KDATAAH}$ | A port data hold time after clock | 203 | | 213 | | 226 | | 272 | | ps |
| $t_{M4KADDRASU}$ | A port address setup time before clock | 22 | | 23 | | 24 | | 29 | | ps |
| $t_{M4KADDRAH}$ | A port address hold time after clock | 203 | | 213 | | 226 | | 272 | | ps |
| $t_{M4KDATABSU}$ | B port data setup time before clock | 22 | | 23 | | 24 | | 29 | | ps |

| Table 4–88. Stratix II GX Maximum Input Clock Rate for Column I/O Pins (Part 2 of 2) | | | | |
|---|---|---|---|---|
| I/O Standard | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Unit |
| Differential SSTL-18 Class I I | 500 | 500 | 500 | MHz |
| 1.8-V differential HSTL Class I | 500 | 500 | 500 | MHz |
| 1.8-V differential HSTL Class II | 500 | 500 | 500 | MHz |
| 1.5-V differential HSTL Class I | 500 | 500 | 500 | MHz |
| 1.5-V differential HSTL Class I I | 500 | 500 | 500 | MHz |
| 1.2-V HSTL | 280 | 250 | 250 | MHz |
| 1.2-V differential HSTL | 280 | 250 | 250 | MHz |

Table 4–89 shows the maximum input clock toggle rates for Stratix II GX device row pins.

| Table 4–89. Stratix II GX Maximum Input Clock Rate for Row I/O Pins (Part 1 of 2) | | | | |
|---|---|---|---|---|
| I/O Standard | -3 Speed Grade | -4 Speed Grade | -5 Speed Grade | Unit |
| LVTTL | 500 | 500 | 450 | MHz |
| 2.5 V | 500 | 500 | 450 | MHz |
| 1.8 V | 500 | 500 | 450 | MHz |
| 1.5 V | 500 | 500 | 450 | MHz |
| LVCMOS | 500 | 500 | 450 | MHz |
| SSTL-2 Class I | 500 | 500 | 500 | MHz |
| SSTL-2 Class II | 500 | 500 | 500 | MHz |
| SSTL-18 Class I | 500 | 500 | 500 | MHz |
| SSTL-18 Class II | 500 | 500 | 500 | MHz |
| 1.5-V HSTL Class I | 500 | 500 | 500 | MHz |
| 1.5-V HSTL Class II | 500 | 500 | 500 | MHz |
| 1.8-V HSTL Class I | 500 | 500 | 500 | MHz |
| 1.8-V HSTL Class II | 500 | 500 | 500 | MHz |
| PCI | 500 | 500 | 425 | MHz |
| PCI-X | 500 | 500 | 425 | MHz |
| Differential SSTL-2 Class I | 500 | 500 | 500 | MHz |

Table 4–109 shows the high-speed I/O timing specifications for -5 speed grade Stratix II GX devices.

**Table 4–109. High-Speed I/O Specifications for -5 Speed Grade** *Notes (1), (2)*

| Symbol | Conditions | | | -5 Speed Grade | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $f_{IN} = f_{HSDR} / W$ | W = 2 to 32 (LVDS, HyperTransport technology) *(3)* | | | 16 | | 420 | MHz |
| | W = 1 (SERDES bypass, LVDS only) | | | 16 | | 500 | MHz |
| | W = 1 (SERDES used, LVDS only) | | | 150 | | 640 | MHz |
| $f_{HSDR}$ (data rate) | J = 4 to 10 (LVDS, HyperTransport technology) | | | 150 | | 840 | Mbps |
| | J = 2 (LVDS, HyperTransport technology) | | | *(4)* | | 700 | Mbps |
| | J = 1 (LVDS only) | | | *(4)* | | 500 | Mbps |
| $f_{HSDRDPA}$ (DPA data rate) | J = 4 to 10 (LVDS, HyperTransport technology) | | | 150 | | 840 | Mbps |
| TCCS | All differential I/O standards | | | - | | 200 | ps |
| SW | All differential I/O standards | | | 440 | | - | ps |
| Output jitter | | | | | | 190 | ps |
| Output $t_{RISE}$ | All differential I/O standards | | | | | 290 | ps |
| Output $t_{FALL}$ | All differential I/O standards | | | | | 290 | ps |
| $t_{DUTY}$ | | | | 45 | 50 | 55 | % |
| DPA run length | | | | | | 6,400 | UI |
| DPA jitter tolerance | Data channel peak-to-peak jitter | | | 0.44 | | | UI |
| DPA lock time | | | | | | | Number of repetitions |
| | SPI-4 | 0000000000 1111111111 | 10% | 256 | | | |
| | Parallel Rapid I/O | 00001111 | 25% | 256 | | | |
| | | 10010000 | 50% | 256 | | | |
| | Miscellaneous | 10101010 | 100% | 256 | | | |
| | | 01010101 | | 256 | | | |

(1) When J = 4 to 10, the SERDES block is used.
(2) When J = 1 or 2, the SERDES block is bypassed.
(3) The input clock frequency and the W factor must satisfy the following fast PLL VCO specification: 150 ≤ input clock frequency × W ≤ 840.
(4) The minimum specification is dependent on the clock source (fast PLL, enhanced PLL, clock pin, and so on) and the clock routing resource (global, regional, or local) utilized. The I/O differential buffer and input register do not have a minimum toggle rate.