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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3022
Number of Logic Elements/Cells	60440
Total RAM Bits	2544192
Number of I/O	534
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2sgx60ef1152c4

- Support for multiple intellectual property megafunctions from Altera® MegaCore® functions and Altera Megafunction Partners Program (AMPP^{SM}) megafunctions
- Support for design security using configuration bitstream encryption
- Support for remote configuration updates

- Transceiver block features:
  - High-speed serial transceiver channels with clock data recovery (CDR) provide 600-megabits per second (Mbps) to 6.375-Gbps full-duplex transceiver operation per channel
  - Devices available with 4, 8, 12, 16, or 20 high-speed serial transceiver channels providing up to 255 Gbps of serial bandwidth (full duplex)
  - Dynamically programmable voltage output differential (V_{OD}) and pre-emphasis settings for improved signal integrity
  - Support for CDR-based serial protocols, including PCI Express, Gigabit Ethernet, SDI, Altera's SerialLite II, XAUI, CEI-6G, CPRI, Serial RapidIO, SONET/SDH
  - Dynamic reconfiguration of transceiver channels to switch between multiple protocols and data rates
  - Individual transmitter and receiver channel power-down capability for reduced power consumption during non-operation
  - Adaptive equalization (AEQ) capability at the receiver to compensate for changing link characteristics
  - Selectable on-chip termination resistors (100, 120, or 150 Ω) for improved signal integrity on a variety of transmission media
  - Programmable transceiver-to-FPGA interface with support for 8-, 10-, 16-, 20-, 32-, and 40-bit wide data transfer
  - 1.2- and 1.5-V pseudo current mode logic (PCML) for 600 Mbps to 6.375 Gbps (AC coupling)
  - Receiver indicator for loss of signal (available only in PIPE mode)
  - Built-in self test (BIST)
  - Hot socketing for hot plug-in or hot swap and power sequencing support without the use of external devices
  - Rate matcher, byte-reordering, bit-reordering, pattern detector, and word aligner support programmable patterns
  - Dedicated circuitry that is compliant with PIPE, XAUI, and GIGE
  - Built-in byte ordering so that a frame or packet always starts in a known byte lane
  - Transmitters with two PLL inputs for each transceiver block with independent clock dividers to provide varying clock rates on each of its transmitters

Control and Status Signals

The rx_enapatternalign signal is the FPGA control signal that enables word alignment in non-automatic modes. The rx_enapatternalign signal is not used in automatic modes (PCI Express, XAUI, GIGE, CPRI, and Serial RapidIO).

In manual alignment mode, after the rx_enapatternalign signal is activated, the rx_syncstatus signal goes high for one parallel clock cycle to indicate that the alignment pattern has been detected and the word boundary has been locked. If the rx_enapatternalign is deactivated, the rx_syncstatus signal acts as a re-synchronization signal to signify that the alignment pattern has been detected but not locked on a different word boundary.

When using the synchronization state machine, the rx_syncstatus signal indicates the link status. If the rx_syncstatus signal is high, link synchronization is achieved. If the rx_syncstatus signal is low, synchronization has not yet been achieved, or there were enough code group errors to lose synchronization.

In some modes, the rx_enapatternalign signal can be configured to operate as a rising edge signal.

For more information on manual alignment modes, refer to the *Stratix II GX Device Handbook*, volume 2.

When the rx_enapatternalign signal is sensitive to the rising edge, each rising edge triggers a new boundary alignment search, clearing the rx_syncstatus signal.

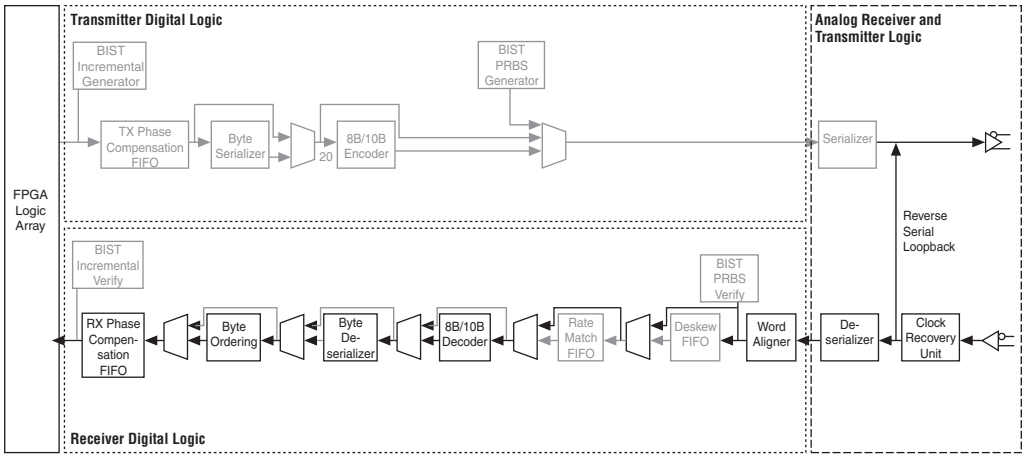
The rx_patterndetect signal pulses high during a new alignment, and also whenever the alignment pattern occurs on the current word boundary.

SONET/SDH

In all the SONET/SDH modes, you can configure the word aligner to either align to A1A2 or A1A1A2A2 patterns. Once the pattern is found, the word boundary is aligned and the word aligner asserts the rx_patterndetect signal for one clock cycle.

Figure 2–26 shows the data path in reverse serial loopback mode.

Figure 2–26. Stratix II GX Block in Reverse Serial Loopback Mode



Reverse Serial Pre-CDR Loopback

The reverse serial pre-CDR loopback mode uses the analog portion of the transceiver. An external source (pattern generator or transceiver) generates the source data. The high-speed serial source data arrives at the high-speed differential receiver input buffer, loops back before the CRU unit, and is transmitted though the high-speed differential transmitter output buffer. It is for test or verification use only to verify the signal being received after the gain and equalization improvements of the input buffer. The signal at the output is not exactly what is received since the signal goes through the output buffer and the VOD is changed to the VOD setting level. The pre-emphasis settings have no effect.

Adaptive Logic Modules

The basic building block of logic in the Stratix II GX architecture is the ALM. The ALM provides advanced features with efficient logic utilization. Each ALM contains a variety of look-up table (LUT)-based resources that can be divided between two adaptive LUTs (ALUTs). With up to eight inputs to the two ALUTs, one ALM can implement various combinations of two functions. This adaptability allows the ALM to be completely backward-compatible with four-input LUT architectures. One ALM can also implement any function of up to six inputs and certain seven-input functions.

In addition to the adaptive LUT-based resources, each ALM contains two programmable registers, two dedicated full adders, a carry chain, a shared arithmetic chain, and a register chain. Through these dedicated resources, the ALM can efficiently implement various arithmetic functions and shift registers. Each ALM drives all types of interconnects: local, row, column, carry chain, shared arithmetic chain, register chain, and direct link interconnects. Figure 2–35 shows a high-level block diagram of the Stratix II GX ALM while Figure 2–36 shows a detailed view of all the connections in the ALM.

Figure 2–35. High-Level Block Diagram of the Stratix II GX ALM

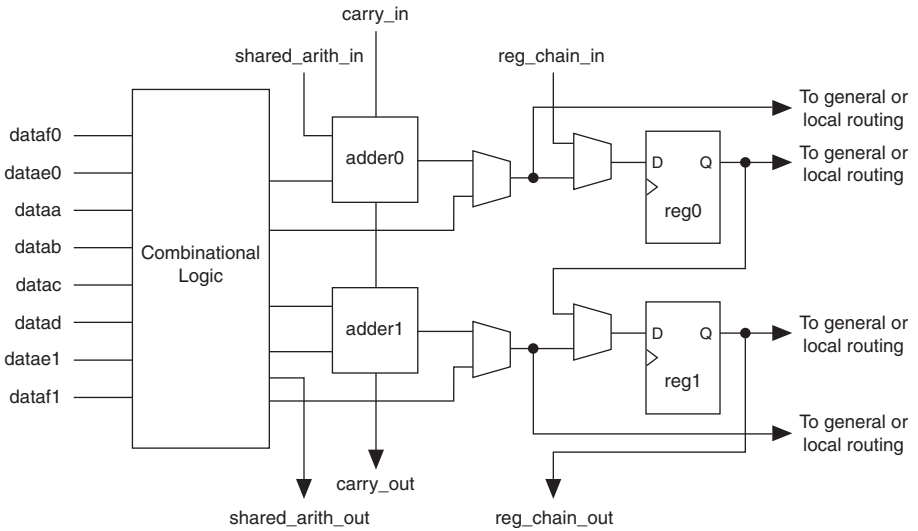
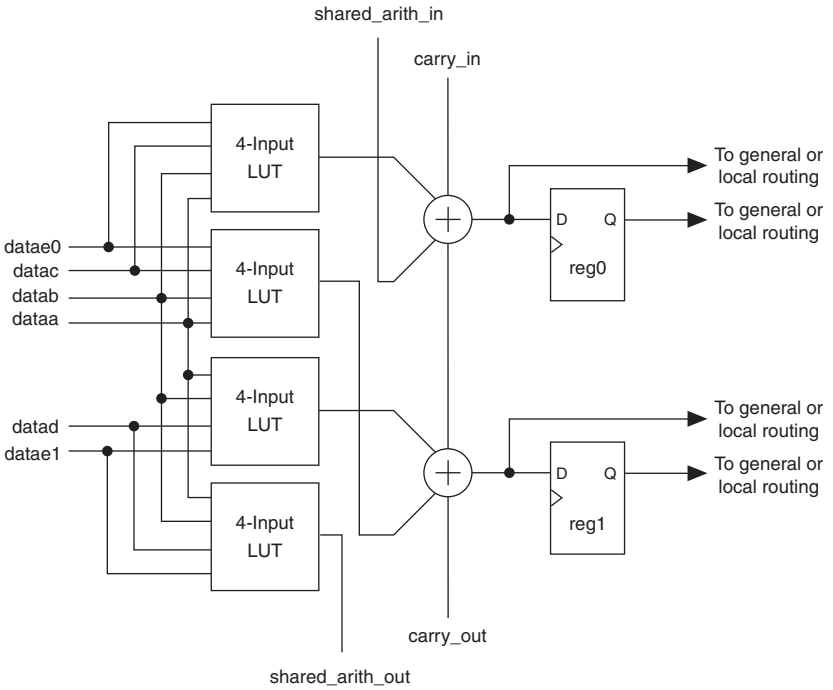


Figure 2–43. ALM in Shared Arithmetic Mode



Note to Figure 2–43:
(1) Inputs `dataf0` and `dataf1` are available for register packing in shared arithmetic mode.

Adder trees are used in many different applications. For example, the summation of the partial products in a logic-based multiplier can be implemented in a tree structure. Another example is a correlator function that can use a large adder tree to sum filtered data samples in a given time frame to recover or to de-spread data which was transmitted utilizing spread spectrum technology. An example of a three-bit add operation utilizing the shared arithmetic mode is shown in Figure 2–44. The partial sum (`S[2..0]`) and the partial carry (`C[2..0]`) is obtained using the LUTs, while the result (`R[2..0]`) is computed using the dedicated adders.

R24 row interconnects span 24 LABs and provide the fastest resource for long row connections between LABs, TriMatrix memory, DSP blocks, and Row IOEs. The R24 row interconnects can cross M-RAM blocks. R24 row interconnects drive to other row or column interconnects at every fourth LAB and do not drive directly to LAB local interconnects. R24 row interconnects drive LAB local interconnects via R4 and C4 interconnects. R24 interconnects can drive R24, R4, C16, and C4 interconnects. The column interconnect operates similarly to the row interconnect and vertically routes signals to and from LABs, TriMatrix memory, DSP blocks, and IOEs. Each column of LABs is served by a dedicated column interconnect.

These column resources include:

- Shared arithmetic chain interconnects in a LAB
- Carry chain interconnects in a LAB and from LAB to LAB
- Register chain interconnects in a LAB
- C4 interconnects traversing a distance of four blocks in an up and down direction
- C16 column interconnects for high-speed vertical routing through the device

Stratix II GX devices include an enhanced interconnect structure in LABs for routing shared arithmetic chains and carry chains for efficient arithmetic functions. The register chain connection allows the register output of one ALM to connect directly to the register input of the next ALM in the LAB for fast shift registers. These ALM-to-ALM connections bypass the local interconnect. The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. Figure 2–47 shows the shared arithmetic chain, carry chain, and register chain interconnects.

PLLs and Clock Networks

Stratix II GX devices provide a hierarchical clock structure and multiple phase-locked loops (PLLs) with advanced features. The large number of clocking resources in combination with the clock synthesis precision provided by enhanced and fast PLLs provides a complete clock management solution.

Global and Hierarchical Clocking

Stratix II GX devices provide 16 dedicated global clock networks and 32 regional clock networks (eight per device quadrant). These clocks are organized into a hierarchical clock structure that allows for up to 24 clocks per device region with low skew and delay. This hierarchical clocking scheme provides up to 48 unique clock domains in Stratix II GX devices.

There are 12 dedicated clock pins to drive either the global or regional clock networks. Four clock pins drive each side of the device, as shown in Figures 2–61 and 2–62. Internal logic and enhanced and fast PLL outputs can also drive the global and regional clock networks. Each global and regional clock has a clock control block, which controls the selection of the clock source and dynamically enables or disables the clock to reduce power consumption. Table 2–24 shows global and regional clock features.

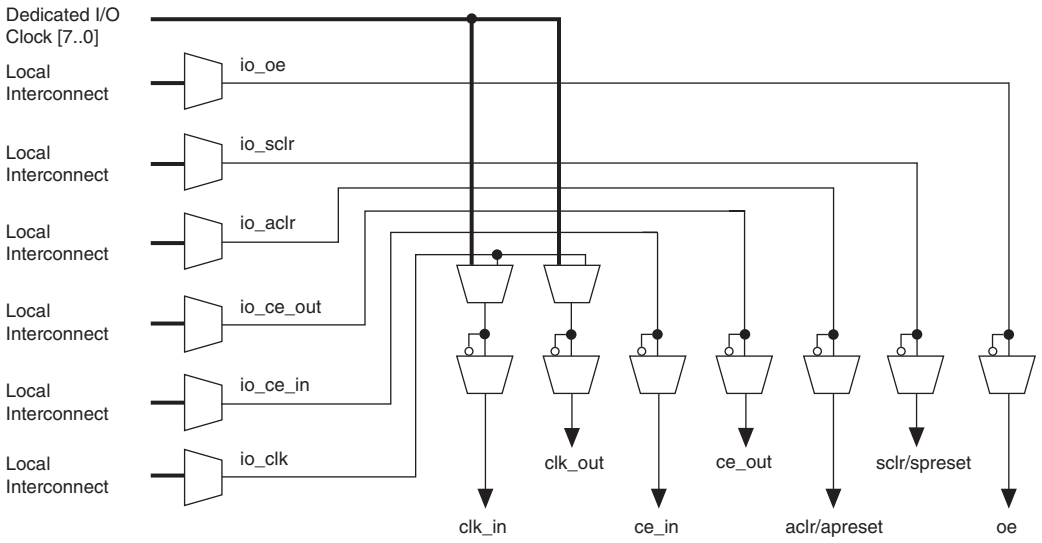
Table 2–24. Global and Regional Clock Features

Feature	Global Clocks	Regional Clocks
Number per device	16	32
Number available per quadrant	16	8
Sources	Clock pins, PLL outputs, core routings, inter-transceiver clocks	Clock pins, PLL outputs, core routings, inter-transceiver clocks
Dynamic clock source selection	✓	—
Dynamic enable/disable	✓	✓

Global Clock Network

These clocks drive throughout the entire device, feeding all device quadrants. The global clock networks can be used as clock sources for all resources in the device IOEs, ALMs, DSP blocks, and all memory blocks. These resources can also be used for control signals, such as clock enables and synchronous or asynchronous clears fed from the external pin. The global clock networks can also be driven by internal logic for internally

Figure 2–80. Control Signal Selection per IOE *Note (1)*



Note to Figure 2–80:

(1) Control signals `ce_in`, `ce_out`, `aclr/apreset`, `sclr/spreset`, and `oe` can be global signals even though their control selection multiplexers are not directly fed by the `ioe_clk[7..0]` signals. The `ioe_clk` signals can drive the I/O local interconnect, which then drives the control selection multiplexers.

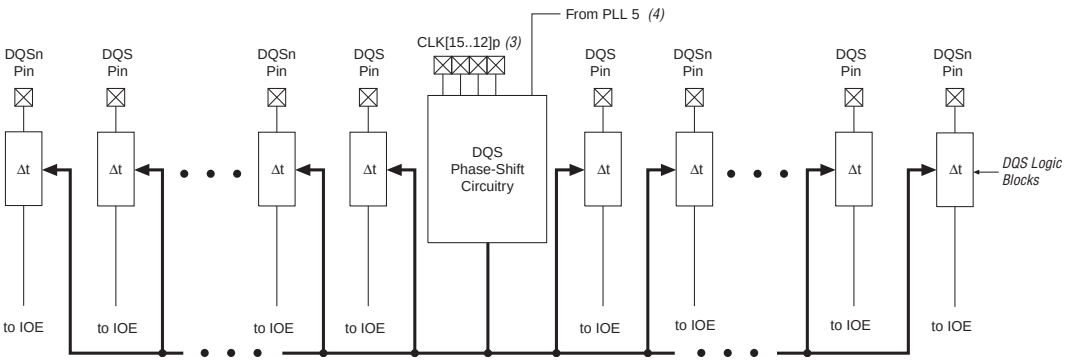
In normal bidirectional operation, you can use the input register for input data requiring fast setup times. The input register can have its own clock input and clock enable separate from the OE and output registers. The output register can be used for data requiring fast clock-to-output performance. You can use the OE register for fast clock-to-output enable timing. The OE and output register share the same clock source and the same clock enable source from local interconnect in the associated LAB, dedicated I/O clocks, and the column and row interconnects. Figure 2–81 shows the IOE in bidirectional configuration.

A compensated delay element on each DQS pin automatically aligns input DQS synchronization signals with the data window of their corresponding DQ data signals. The DQS signals drive a local DQS bus in the top and bottom I/O banks. This DQS bus is an additional resource to the I/O clocks and is used to clock DQ input registers with the DQS signal.

The Stratix II GX device has two phase-shifting reference circuits, one on the top and one on the bottom of the device. The circuit on the top controls the compensated delay elements for all DQS pins on the top. The circuit on the bottom controls the compensated delay elements for all DQS pins on the bottom.

Each phase-shifting reference circuit is driven by a system reference clock, which must have the same frequency as the DQS signal. Clock pins `CLK[15..12]p` feed the phase circuitry on the top of the device and clock pins `CLK[7..4]p` feed the phase circuitry on the bottom of the device. In addition, PLL clock outputs can also feed the phase-shifting reference circuits. Figure 2–86 shows the phase-shift reference circuit control of each DQS delay shift on the top of the device. This same circuit is duplicated on the bottom of the device.

Figure 2–86. DQS Phase-Shift Circuitry *Notes (1), (2)*



Notes to Figure 2–86:

(1) There are up to 18 pairs of DQS and DQSn pins available on the top or the bottom of the Stratix II GX device. There are up to 10 pairs on the right side and 8 pairs on the left side of the DQS phase-shift circuitry.

(2) The "t" module represents the DQS logic block.

(3) Clock pins `CLK[15..12]p` feed the phase-shift circuitry on the top of the device and clock pins `CLK[7..4]p` feed the phase circuitry on the bottom of the device. You can also use a PLL clock output as a reference clock to the phaseshift circuitry.

(4) You can only use PLL 5 to feed the DQS phase-shift circuitry on the top of the device and PLL 6 to feed the DQS phase-shift circuitry on the bottom of the device.

Table 2–34. On-Chip Termination Support by I/O Banks (Part 2 of 2)

On-Chip Termination Support	I/O Standard Support	Top and Bottom Banks (3, 4, 7, 8)	Left Bank (1, 2)
Series termination with calibration	3.3-V LVTTL	✓	—
	3.3-V LVCMOS	✓	—
	2.5-V LVTTL	✓	—
	2.5-V LVCMOS	✓	—
	1.8-V LVTTL	✓	—
	1.8-V LVCMOS	✓	—
	1.5-V LVTTL	✓	—
	1.5-V LVCMOS	✓	—
	SSTL-2 class I and II	✓	—
	SSTL-18 class I and II	✓	—
	1.8-V HSTL class I	✓	—
	1.8-V HSTL class II	✓	—
	1.5-V HSTL class I	✓	—
	1.2-V HSTL	✓	—
Differential termination *(1)*	LVDS	—	✓
	HyperTransport technology	—	✓

Note to Table 2–34:

(1) Clock pins `CLK1` and `CLK3`, and pins `FPLL[7..8]CLK` do not support differential on-chip termination. Clock pins `CLK0` and `CLK2`, do support differential on-chip termination. Clock pins in the top and bottom banks (`CLK[4..7, 12..15]`) do not support differential on-chip termination.

Differential On-Chip Termination

Stratix II GX devices support internal differential termination with a nominal resistance value of 100 for LVDS input receiver buffers. LVPECL input signals (supported on clock pins only) require an external termination resistor. Differential on-chip termination is supported across the full range of supported differential data rates, as shown in the *High-Speed I/O Specifications* section of the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II GX Device Handbook*.

For more information on differential on-chip termination, refer to the *High-Speed Differential I/O Interfaces with DPA in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook*.

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 4 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Sinusoidal jitter FC-1	Fc/25000	> 1.5			> 1.5			> 1.5			UI
	Fc/1667	> 0.1			> 0.1			> 0.1			UI
Deterministic jitter FC-2	Pattern = CJTPAT No Equalization DC Gain = 0 dB	> 0.33			> 0.33			> 0.33			UI
Random jitter FC-2	Pattern = CJTPAT No Equalization DC Gain = 0 dB	> 0.29			> 0.29			> 0.29			UI
Sinusoidal jitter FC-2	Fc/25000	> 1.5			> 1.5			> 1.5			UI
	Fc/1667	> 0.1			> 0.1			> 0.1			UI
Deterministic jitter FC-4	Pattern = CJTPAT No Equalization DC Gain = 0 dB	> 0.33			> 0.33			> 0.33			UI
Random jitter FC-4	Pattern = CJTPAT No Equalization DC Gain = 0 dB	> 0.29			> 0.29			> 0.29			UI
Sinusoidal jitter FC-4	Fc/25000	> 1.5			> 1.5			> 1.5			UI
	Fc/1667	> 0.1			> 0.1			> 0.1			UI
XAUI Transmit Jitter Generation *(9)*											
Total jitter at 3.125 Gbps	REFCLK = 156.25 MHz Pattern = CJPAT V_{OD} = 1200 mV No Pre-emphasis	-	-	0.3	-	-	0.3	-	-	0.3	UI
Deterministic jitter at 3.125 Gbps	REFCLK = 156.25 MHz Pattern = CJPAT V_{OD} = 1200 mV No Pre-emphasis	-	-	0.17	-	-	0.17	-	-	0.17	UI
XAUI Receiver Jitter Tolerance *(9)*											
Total jitter	Pattern = CJPAT No Equalization DC Gain = 3 dB	> 0.65			> 0.65			> 0.65			UI
Deterministic jitter	Pattern = CJPAT No Equalization DC Gain = 3 dB	> 0.37			> 0.37			> 0.37			UI

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 5 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Peak-to-peak jitter	Jitter frequency = 22.1 KHz		> 8.5			> 8.5			> 8.5		UI
Peak-to-peak jitter	Jitter frequency = 1.875 MHz		> 0.1			> 0.1			> 0.1		UI
Peak-to-peak jitter	Jitter frequency = 20 MHz		> 0.1			> 0.1			> 0.1		UI
PCI Express Transmit Jitter Generation *(10)*											
Total jitter at 2.5 Gbps	Compliance pattern V_{OD} = 800 mV Pre-emphasis (1st post-tap) = Setting 5	-	-	0.25	-	-	0.25	-	-	0.25	UI
PCI Express Receiver Jitter Tolerance *(10)*											
Total jitter at 2.5 Gbps	Compliance pattern No Equalization DC gain = 3 dB		> 0.6			> 0.6			> 0.6		UI
Serial RapidIO Transmit Jitter Generation *(11)*											
Deterministic Jitter (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps REFCLK = 125 MHz Pattern = CJPAT V_{OD} = 800 mV No Pre-emphasis	-	-	0.17	-	-	0.17	-	-	0.17	UI
Total Jitter (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps REFCLK = 125 MHz Pattern = CJPAT V_{OD} = 800 mV No Pre-emphasis	-	-	0.35	-	-	0.35	-	-	0.35	UI

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 6 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Serial RapidIO Receiver Jitter Tolerance *(11)*											
Deterministic Jitter Tolerance (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps REFCLK = 125 MHz Pattern = CJPAT Equalizer Setting = 0 for 1.25 Gbps Equalizer Setting = 6 for 2.5 Gbps Equalizer Setting = 6 for 3.125 Gbps	> 0.37			> 0.37			> 0.37			UI
Combined Deterministic and Random Jitter Tolerance (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps REFCLK = 125 MHz Pattern = CJPAT Equalizer Setting = 0 for 1.25 Gbps Equalizer Setting = 6 for 2.5 Gbps Equalizer Setting = 6 for 3.125 Gbps	> 0.55			> 0.55			> 0.55			UI

Table 4–23. Stratix II GX Device DC Operating Conditions (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Device	Minimum	Typical	Maximum	Unit
R_{CONF} *(4)*	Value of I/O pin pull-up resistor before and during configuration	Vi = 0, V_{CCIO} = 3.3 V		10	25	50	KOhm
		Vi = 0, V_{CCIO} = 2.5 V		15	35	70	KOhm
		Vi = 0, V_{CCIO} = 1.8 V		30	50	100	KOhm
		Vi = 0, V_{CCIO} = 1.5 V		40	75	150	KOhm
		Vi = 0, V_{CCIO} = 1.2 V		50	90	170	KOhm
	Recommended value of I/O pin external pull-down resistor before and during configuration				1	2	KOhm

Notes to Table 4–23:

(1) Typical values are for T_A = 25 °C, V_{CCINT} = 1.2 V, and V_{CCIO} = 1.5 V, 1.8 V, 2.5 V, and 3.3 V.

(2) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3, 2.5, 1.8, and 1.5 V).

(3) Maximum values depend on the actual TJ and design utilization. See *PowerPlay Early Power Estimator (EPE) and Power Analyzer* or the *Quartus II PowerPlay Power Analyzer and Optimization Technology* (available at **www.altera.com**) for maximum values. See the section "Power Consumption" on page 4–59 for more information.

(4) Pin pull-up resistance values will lower if an external source drives the pin higher than V_{CCIO}.

I/O Standard Specifications

Tables 4–24 through 4–47 show the Stratix II GX device family I/O standard specifications.

Table 4–24. LVTTL Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO} *(1)*	Output supply voltage		3.135	3.465	V
V_{IH}	High-level input voltage		1.7	4.0	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	High-level output voltage	I_{OH} = –4 mA *(2)*	2.4		V

Bus Hold Specifications

Table 4–48 shows the Stratix II GX device family bus hold specifications.

Table 4–48. Bus Hold Parameters

Parameter	Conditions	V_{CCIO} Level										Unit
		1.2 V		1.5 V		1.8 V		2.5 V		3.3 V		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	$V_{IN} > V_{IL}$ (maximum)	22.5		25		30		50		70		µA
High sustaining current	$V_{IN} < V_{IH}$ (minimum)	–22.5		–25		–30		–50		–70		µA
Low overdrive current	$0 V < V_{IN} < V_{CCIO}$		120		160		200		300		500	µA
High overdrive current	$0 V < V_{IN} < V_{CCIO}$		–120		–160		–200		–300		–500	µA
Bus-hold trip point		0.45	0.95	0.5	1.0	0.68	1.07	0.7	1.7	0.8	2.0	V

On-Chip Termination Specifications

Tables 4–49 and 4–50 define the specification for internal termination resistance tolerance when using series or differential on-chip termination.

Table 4–49. On-Chip Termination Specification for Top and Bottom I/O Banks (Part 1 of 2) *Notes (1), (2)*

Symbol	Description	Conditions	Resistance Tolerance		
			Commercial Max	Industrial Max	Unit
25-Ω R_S 3.3/2.5	Internal series termination with calibration (25-Ω setting)	V_{CCIO} = 3.3/2.5 V	±5	±10	%
	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 3.3/2.5 V	±30	±30	%
50-Ω R_S 3.3/2.5	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 3.3/2.5 V	±5	±10	%
	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 3.3/2.5 V	±30	± 30	%

Table 4–49. On-Chip Termination Specification for Top and Bottom I/O Banks (Part 2 of 2) *Notes (1), (2)*

Symbol	Description	Conditions	Resistance Tolerance		
			Commercial Max	Industrial Max	Unit
50-Ω R_T 2.5	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 1.8 V	±30	± 30	%
25-Ω R_S 1.8	Internal series termination with calibration (25-Ω setting)	V_{CCIO} = 1.8 V	±5	±10	%
	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.8 V	±30	±30	%
50-Ω R_S 1.8	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 1.8 V	±5	±10	%
	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.8 V	±30	±30	%
50-Ω R_T 1.8	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 1.8 V	±10	±15	%
50-Ω R_S 1.5	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 1.5 V	±8	±10	%
	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.5 V	±36	±36	%
50-Ω R_T 1.5	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 1.5 V	±10	±15	%
50-Ω R_S 1.2	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 1.2 V	±8	±10	%
	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.2 V	±50	±50	%
50-Ω R_T 1.2	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 1.2 V	±10	±15	%

Note for Table 4–49:

(1) The resistance tolerance for calibrated SOCT is for the moment of calibration. If the temperature or voltage changes over time, the tolerance may also change.

(2) On-chip parallel termination with calibration is only supported for input pins.

Table 4–92 shows the maximum output clock toggle rates for Stratix II GX device row pins.

Table 4–92. Stratix II GX Maximum Output Clock Rate for Row Pins (Part 1 of 2)

I/O Standard	Drive Strength	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
LVTTL	4 mA	270	225	210	MHz
	8 mA	435	355	325	MHz
	12 mA *(1)*	580	475	420	MHz
LVCMOS	4 mA	290	250	230	MHz
	8 mA	565	480	440	MHz
	12 mA *(1)*	350	350	297	MHz
2.5 V	4 mA	230	194	180	MHz
	8 mA	430	380	380	MHz
	12 mA *(1)*	630	575	550	MHz
1.8 V	2 mA	120	109	104	MHz
	4 mA	285	250	230	MHz
	6 mA	450	390	360	MHz
	8 mA *(1)*	660	570	520	MHz
1.5 V	2 mA	244	200	180	MHz
	4 mA *(1)*	470	370	325	MHz
SSTL-2 Class I	8 mA	400	300	300	MHz
	12 mA *(1)*	400	400	350	MHz
SSTL-2 Class II	16 mA	350	350	300	MHz
	20 mA *(1)*	350	350	297	MHz
SSTL-18 Class I	4 mA	200	150	150	MHz
	6 mA	350	250	200	MHz
	8 mA	450	300	300	MHz
	10 mA	500	400	400	MHz
	12 mA *(1)*	350	350	297	MHz
1.8-V HSTL Class I	4 mA	300	300	300	MHz
	6 mA	500	450	450	MHz
	8 mA	650	600	600	MHz
	10 mA	700	650	600	MHz
	12 mA *(1)*	700	700	650	MHz
1.5-V HSTL Class I	4 mA	350	300	300	MHz
	6 mA	500	500	450	MHz
	8 mA *(1)*	700	650	600	MHz

Table 4–102. Maximum DCD for DDIO Output on Column I/O Pins Without PLL in the Clock Path for -3 Devices (Part 2 of 2) *Note (1)*

Maximum DCD (ps) for DDIO Column Output I/O Standard	Input IO Standard (No PLL in the Clock Path)					Unit
	TTL/CMOS		SSTL-2	SSTL/HSTL	HSTL12	
	3.3/2.5V	1.8/1.5V	2.5V	1.8/1.5V	1.2V	
SSTL-18 Class II	140	260	70	70	70	ps
1.8-V HSTL Class I	150	270	60	60	60	ps
1.8-V HSTL Class II	150	270	60	60	60	ps
1.5-V HSTL Class I	150	270	55	55	55	ps
1.5-V HSTL Class II	125	240	85	85	85	ps
1.2-V HSTL	240	360	155	155	155	ps
LVPECL	180	180	180	180	180	ps

(1) Table 4–102 assumes the input clock has zero DCD.

Table 4–103. Maximum DCD for DDIO Output on Column I/O Pins Without PLL in the Clock Path for -4 and -5 Devices *Note (1)*

Maximum DCD (ps) for DDIO Column Output I/O Standard	Input IO Standard (No PLL in the Clock Path)				Unit
	TTL/CMOS		SSTL-2	SSTL/HSTL	
	3.3/2.5V	1.8/1.5V	2.5V	1.8/1.5V	
3.3-V LVTTL	440	495	170	160	ps
3.3-V LVCMOS	390	450	120	110	ps
2.5 V	375	430	105	95	ps
1.8 V	325	385	90	100	ps
1.5-V LVCMOS	430	490	160	155	ps
SSTL-2 Class I	355	410	85	75	ps
SSTL-2 Class II	350	405	80	70	ps
SSTL-18 Class I	335	390	65	65	ps
SSTL-18 Class II	320	375	70	80	ps
1.8-V HSTL Class I	330	385	60	70	ps
1.8-V HSTL Class II	330	385	60	70	ps
1.5-V HSTL Class I	330	390	60	70	ps
1.5-V HSTL Class II	330	360	90	100	ps
LVPECL	180	180	180	180	ps

(1) Table 4–103 assumes the input clock has zero DCD.

Table 4–105. Maximum DCD for DDIO Output on Column I/O Pins With PLL in the Clock Path (Part 2 of 2)			
Maximum DCD (ps) for Column DDIO Output I/O Standard	Stratix II GX Devices (PLL Output Feeding DDIO)		Unit
	-3 Device	-4 and -5 Device	
1.2-V HSTL	155	155	ps
LVPECL	180	180	ps

High-Speed I/O Specifications

Table 4–106 provides high-speed timing specifications definitions.

Table 4–106. High-Speed Timing Specifications and Definitions	
High-Speed Timing Specifications	Definitions
t_C	High-speed receiver/transmitter input and output clock period.
f_{HSCLK}	High-speed receiver/transmitter input and output clock frequency.
J	Deserialization factor (width of parallel data bus).
W	PLL multiplication factor.
t_{RISE}	Low-to-high transmission time.
t_{FALL}	High-to-low transmission time.
Timing unit interval (TUI)	The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency × Multiplication Factor) = t_C/w).
f_{IN}	Fast PLL input clock frequency
f_{HSDR}	Maximum/minimum LVDS data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
$f_{HSDRDPA}$	Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.
Channel-to-channel skew (TCCS)	The timing difference between the fastest and the slowest output edges including t_{CO} variation and clock skew across channels driven by the same fast PLL. The clock is included in the TCCS measurement.
Sampling window (SW)	The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window.
Input jitter	Peak-to-peak input jitter on high-speed PLLs.
Output jitter	Peak-to-peak output jitter on high-speed PLLs.
t_{DUTY}	Duty cycle on high-speed transmitter output clock.
t_{LOCK}	Lock time for high-speed transmitter and receiver PLLs.

Document Revision History

Table 6–105 shows the revision history for this chapter.

Table 4–118. Document Revision History (Part 1 of 5)

Date and Document Version	Changes Made	Summary of Changes
June 2009 v4.6	Replaced Table 4–31 Updated: • Table 4–5 • Table 4–6 • Table 4–7 • Table 4–8 • Table 4–9 • Table 4–10 • Table 4–11 • Table 4–12 • Table 4–13 • Table 4–14 • Table 4–15 • Table 4–16 • Table 4–17 • Table 4–18 • Table 4–20 • Table 4–50 • Table 4–95 • Table 4–105 • Table 4–110 • Table 4–111	
October 2007 v4.5	Updated: • Table 4–3 • Table 4–6 • Table 4–16 • Table 4–19 • Table 4–20 • Table 4–21 • Table 4–22 • Table 4–55 • Table 4–106 • Table 4–107 • Table 4–108 • Table 4–109 • Table 4–112	
	Updated title only in Tables 4–88 and 4–89.	
	Minor text edits.	