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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3022
Number of Logic Elements/Cells	60440
Total RAM Bits	2544192
Number of I/O	534
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2sgx60ef1152c4n

GIGE Mode

In GIGE mode, the rate matcher adheres to the specifications in clause 36 of the IEEE 802.3 documentation for idle additions or removals. The rate matcher performs clock compensation only on /I2/ ordered sets, composed of a /K28.5/+ followed by a /D16.2/-. The rate matcher does not perform clock compensation on any other ordered set combinations. An /I2/ is added or deleted automatically based on the number of words in the FIFO buffer. A K28.4 is given at the control and data ports when the FIFO buffer is in an overflow or underflow condition.

XAUI Mode

In XAUI mode, the rate matcher adheres to clause 48 of the IEEE 802.3ae specification for clock rate compensation. The rate matcher performs clock compensation on columns of /R/ (/K28.0/), denoted by //R//. An //R// is added or deleted automatically based on the number of words in the FIFO buffer.

PCI Express Mode

PCI Express mode operates at a data rate of 2.5 Gbps, and supports lane widths of ×1, ×2, ×4, and ×8. The rate matcher can support up to ± 300-PPM differences between the upstream transmitter and the receiver. The rate matcher looks for the skip ordered sets (SOS), which usually consist of a /K28.5/ comma followed by three /K28.0/ skip characters. The rate matcher deletes or inserts skip characters when necessary to prevent the rate matching FIFO buffer from overflowing or underflowing.

The Stratix II GX rate matcher in PCI Express mode has FIFO overflow and underflow protection. In the event of a FIFO overflow, the rate matcher deletes any data after the overflow condition to prevent FIFO pointer corruption until the rate matcher is not full. In an underflow condition, the rate matcher inserts 9'h1FE (/K30.7/) until the FIFO is not empty. These measures ensure that the FIFO can gracefully exit the overflow and underflow condition without requiring a FIFO reset.

8B/10B Decoder

The 8B/10B decoder (Figure 2–21) is part of the Stratix II GX transceiver digital blocks (PCS) and lies in the receiver path between the rate matcher and the byte deserializer blocks. The 8B/10B decoder operates in single-width and double-width modes, and can be bypassed if the 8B/10B decoding is not necessary. In single-width mode, the 8B/10B decoder restores the 8-bit data + 1-bit control identifier from the 10-bit code. In double-width mode, there are two 8B/10B decoders in parallel, which restores the 16-bit (2 × 8-bit) data + 2-bit (2 × 1-bit) control identifier from the 20-bit (2 × 10-bit) code. This 8B/10B decoder conforms to the IEEE 802.3 1998 edition standards.

The dynamic reconfiguration block can dynamically reconfigure the following PMA settings:

- Pre-emphasis settings
- Equalizer and DC gain settings
- Voltage Output Differential (V_{OD}) settings

The channel reconfiguration allows you to dynamically modify the data rate, local dividers, and the functional mode of the transceiver channel.

Refer to the *Stratix II GX Device Handbook*, volume 2, for more information.

The dynamic reconfiguration block requires an input clock between 2.5 MHz and 50 MHz. The clock for the dynamic reconfiguration block is derived from a high-speed clock and divided down using a counter.

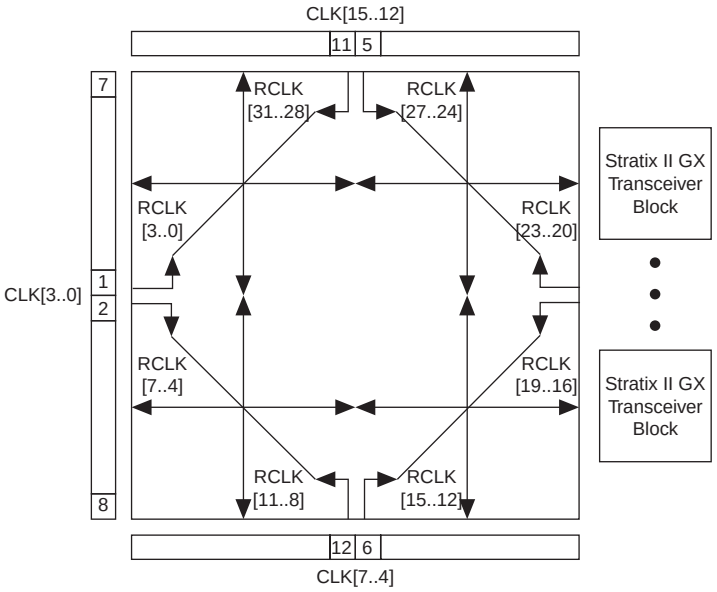
Individual Power Down and Reset for the Transmitter and Receiver

Stratix II GX transceivers offer a power saving advantage with their ability to shut off functions that are not needed. The device can individually reset the receiver and transmitter blocks and the PLLs. The Stratix II GX device can either globally or individually power down and reset the transceiver. Table 2–16 shows the connectivity between the reset signals and the Stratix II GX transceiver blocks. These reset signals can be controlled from the FPGA or pins.

Table 2–23. DSP Block Signal Sources and Destinations

LAB Row at Interface	Control Signals Generated	Data Inputs	Data Outputs
0	clock0 aclr0 ena0 mult01_saturate addnsub1_round/ accum_round addnsub1 signa sourcea sourceb	A1[17..0] B1[17..0]	OA[17..0] OB[17..0]
1	clock1 aclr1 ena1 accum_saturate mult01_round accum_sload sourcea sourceb mode0	A2[17..0] B2[17..0]	OC[17..0] OD[17..0]
2	clock2 aclr2 ena2 mult23_saturate addnsub3_round/ accum_round addnsub3 sign_b sourcea sourceb	A3[17..0] B3[17..0]	OE[17..0] OF[17..0]
3	clock3 aclr3 ena3 accum_saturate mult23_round accum_sload sourcea sourceb mode1	A4[17..0] B4[17..0]	OG[17..0] OH[17..0]

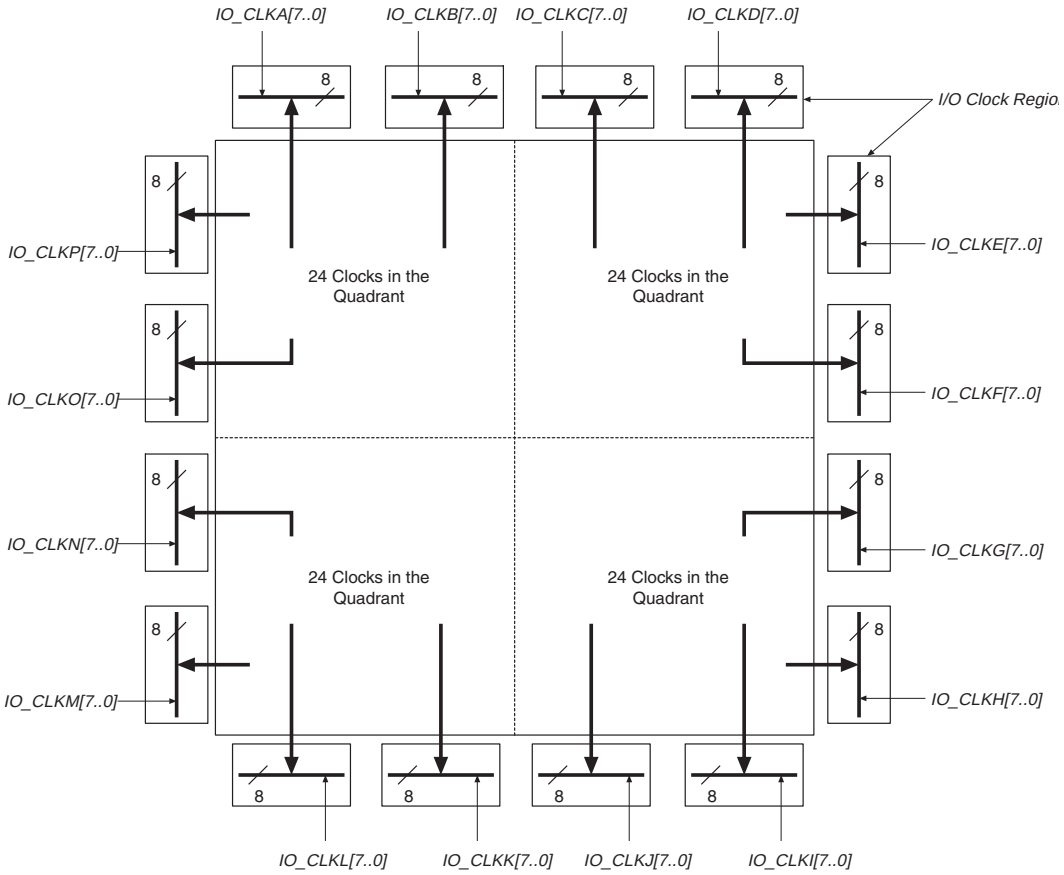
Figure 2–62. Regional Clocks



Dual-Regional Clock Network

A single source (CLK pin or PLL output) can generate a dual-regional clock by driving two regional clock network lines in adjacent quadrants (one from each quadrant), which allows logic that spans multiple quadrants to utilize the same low skew clock. The routing of this clock signal on an entire side has approximately the same speed but slightly higher clock skew when compared with a clock signal that drives a single quadrant. Internal logic-array routing can also drive a dual-regional clock. Clock pins and enhanced PLL outputs on the top and bottom can drive horizontal dual-regional clocks. Clock pins and fast PLL outputs on the left and right can drive vertical dual-regional clocks, as shown in Figure 2–63. Corner PLLs cannot drive dual-regional clocks.

Figure 2–66. EP2SGX60, EP2SGX90 and EP2SGX130 Device I/O Clock Groups



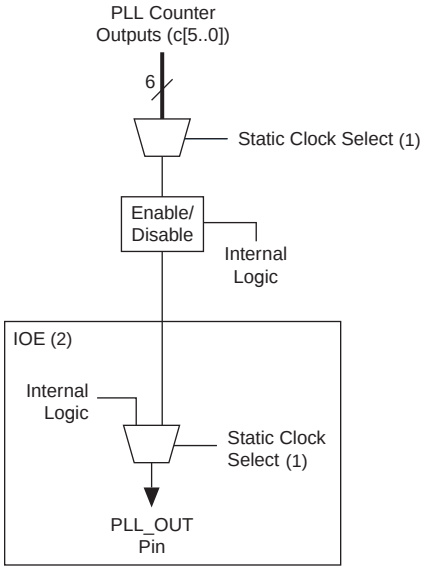
You can use the Quartus II software to control whether a clock input pin drives either a global, regional, or dual-regional clock network. The Quartus II software automatically selects the clocking resources if not specified.

Clock Control Block

Each global clock, regional clock, and PLL external clock output has its own clock control block. The control block has two functions:

- Clock source selection (dynamic selection for global clocks)
- Clock power-down (dynamic clock enable or disable)

Figure 2–69. External PLL Output Clock Control Blocks



Notes to Figure 2–69:

(1) These clock select signals can only be set through a configuration file (**.sof** or **.pof**) and cannot be dynamically controlled during user mode operation.

(2) The clock control block feeds to a multiplexer within the PLL_OUT pin's IOE. The PLL_OUT pin is a dual-purpose pin. Therefore, this multiplexer selects either an internal signal or the output of the clock control block.

For the global clock control block, the clock source selection can be controlled either statically or dynamically. You have the option of statically selecting the clock source by using the Quartus II software to set specific configuration bits in the configuration file (**.sof** or **.pof**) or you can control the selection dynamically by using internal logic to drive the multiplexer select inputs. When selecting statically, the clock source can be set to any of the inputs to the select multiplexer. When selecting the clock source dynamically, you can either select between two PLL outputs (such as the C0 or C1 outputs from one PLL), between two PLLs (such as the C0/C1 clock output of one PLL or the C0/C1 clock output of the other PLL), between two clock pins (such as CLK0 or CLK1), or between a combination of clock pins or PLL outputs.

For the regional and PLL_OUT clock control block, the clock source selection can only be controlled statically using configuration bits. Any of the inputs to the clock select multiplexer can be set as the clock source.

Table 4 3. Stratix II GX Device Recommended Operating Conditions (Part 2 of 2) Note (1)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
T_J	Operating junction temperature	For commercial use	0	85	C
		For industrial use	–40	100	C

Notes to Table 4 3:
(1) Supply voltage specifications apply to voltage readings taken at the device pins, not at the power supply.
(2) During transitions, the inputs may overshoot to the voltage shown in Table 4 2 based upon the input duty cycle. The DC case is equivalent to 100% duty cycle. During transitions, the inputs may undershoot to 2.0 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically from ground to V_{CC}.
(4) V_{CCPD} must ramp-up from 0 V to 3.3 V within 100 s to 100 ms. If V_{CCPD} is not ramped up within this specified time, the Stratix II GX device will not configure successfully. If the system does not allow for a V_{CCPD} ramp-up time of 100 ms or less, hold nCONFIG low until all power supplies are reliable.
(5) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT}, V_{CCPD}, and V_{CCIO} are powered.
(6) V_{CCIO} maximum and minimum conditions for PCI and PCI-X are shown in parentheses.

Transceiver Block Characteristics

Tables 4 4 through 4 6 contain transceiver block specifications.

Table 4 4. Stratix II GX Transceiver Block Absolute Maximum Ratings Note (1)

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCA}	Transceiver block supply voltage	Commercial and industrial	–0.5	4.6	V
V_{CCP}	Transceiver block supply voltage	Commercial and industrial	–0.5	1.8	V
V_{CCR}	Transceiver block supply Voltage	Commercial and industrial	–0.5	1.8	V
V_{CCT}	Transceiver block supply voltage	Commercial and industrial	–0.5	1.8	V
V_{CCT_B}	Transceiver block supply voltage	Commercial and industrial	–0.5	1.8	V
V_{CCL}	Transceiver block supply voltage	Commercial and industrial	–0.5	1.8	V
V_{CCH_B}	Transceiver block supply voltage	Commercial and industrial	–0.5	2.4	V

Note to Table 4 4:
(1) The device can tolerate prolonged operation at this absolute maximum, as long as the maximum specification is not violated.

Figure 4 10. Measurement Setup for t_{zx}

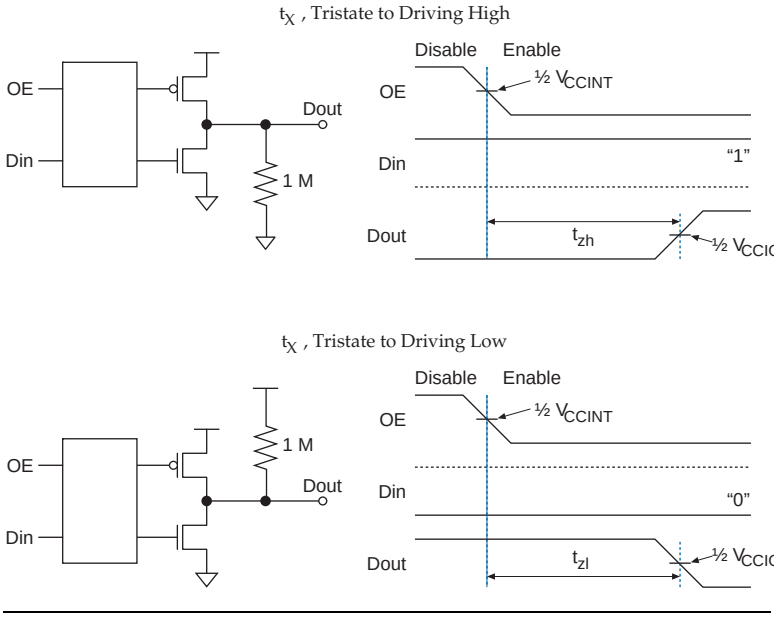


Table 4 54 specifies the input timing measurement setup.

Table 4 54. Timing Measurement Methodology for Input Pins (Part 1 of 2) Notes (1), (2), (3), (4)

I/O Standard	Measurement Conditions			Measurement Point
	V_{CCIO} (V)	V_{REF} (V)	Edge Rate (ns)	VMEAS (V)
LVTTL (5)	3.135		3.135	1.5675
LVCMOS (5)	3.135		3.135	1.5675
2.5 V (5)	2.375		2.375	1.1875
1.8 V (5)	1.710		1.710	0.855
1.5 V (5)	1.425		1.425	0.7125
PCI (6)	2.970		2.970	1.485
PCI-X (6)	2.970		2.970	1.485
SSTL-2 Class I	2.325	1.163	2.325	1.1625
SSTL-2 Class II	2.325	1.163	2.325	1.1625
SSTL-18 Class I	1.660	0.830	1.660	0.83
SSTL-18 Class II	1.660	0.830	1.660	0.83
1.8-V HSTL Class I	1.660	0.830	1.660	0.83