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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

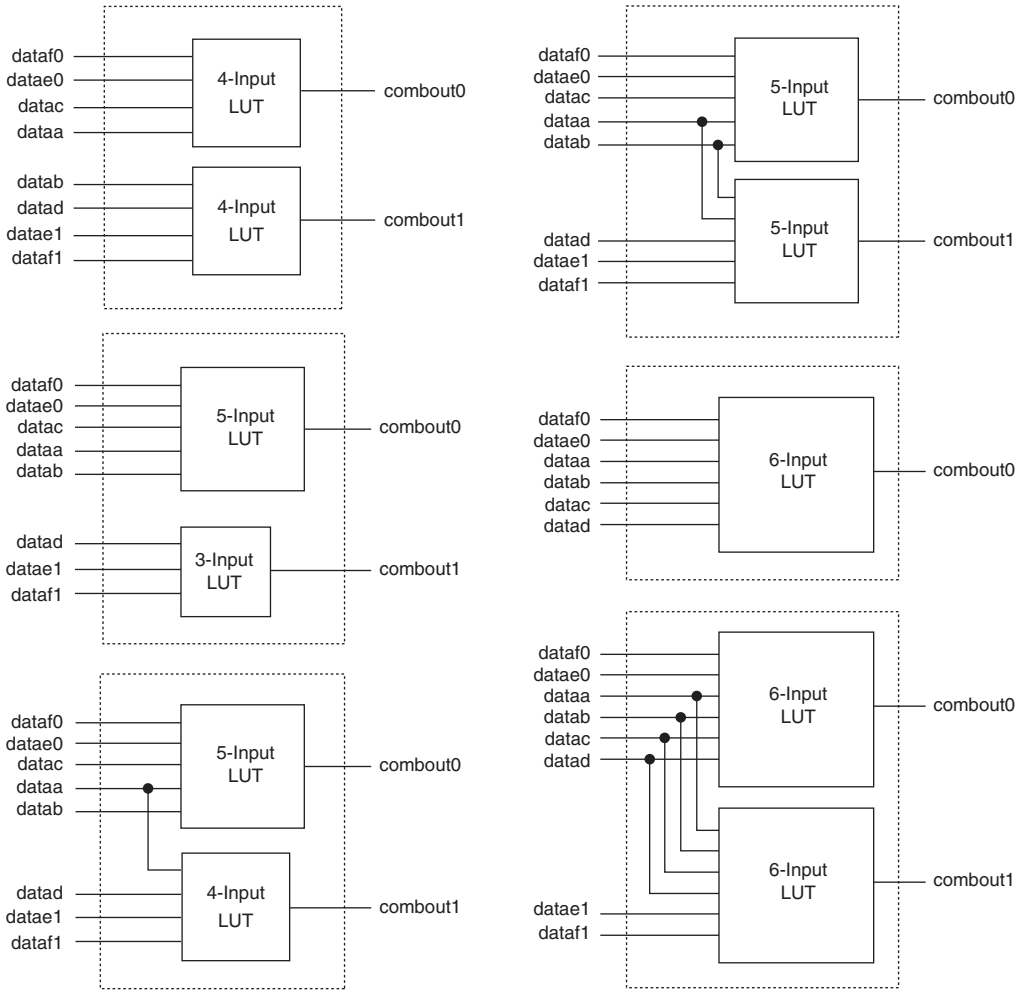
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3022
Number of Logic Elements/Cells	60440
Total RAM Bits	2544192
Number of I/O	534
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2sgx60ef1152c5n

- Support for multiple intellectual property megafunctions from Altera® MegaCore® functions and Altera Megafunction Partners Program (AMPP^{SM}) megafunctions
- Support for design security using configuration bitstream encryption
- Support for remote configuration updates

- Transceiver block features:
  - High-speed serial transceiver channels with clock data recovery (CDR) provide 600-megabits per second (Mbps) to 6.375-Gbps full-duplex transceiver operation per channel
  - Devices available with 4, 8, 12, 16, or 20 high-speed serial transceiver channels providing up to 255 Gbps of serial bandwidth (full duplex)
  - Dynamically programmable voltage output differential (V_{OD}) and pre-emphasis settings for improved signal integrity
  - Support for CDR-based serial protocols, including PCI Express, Gigabit Ethernet, SDI, Altera's SerialLite II, XAUI, CEI-6G, CPRI, Serial RapidIO, SONET/SDH
  - Dynamic reconfiguration of transceiver channels to switch between multiple protocols and data rates
  - Individual transmitter and receiver channel power-down capability for reduced power consumption during non-operation
  - Adaptive equalization (AEQ) capability at the receiver to compensate for changing link characteristics
  - Selectable on-chip termination resistors (100, 120, or 150 Ω) for improved signal integrity on a variety of transmission media
  - Programmable transceiver-to-FPGA interface with support for 8-, 10-, 16-, 20-, 32-, and 40-bit wide data transfer
  - 1.2- and 1.5-V pseudo current mode logic (PCML) for 600 Mbps to 6.375 Gbps (AC coupling)
  - Receiver indicator for loss of signal (available only in PIPE mode)
  - Built-in self test (BIST)
  - Hot socketing for hot plug-in or hot swap and power sequencing support without the use of external devices
  - Rate matcher, byte-reordering, bit-reordering, pattern detector, and word aligner support programmable patterns
  - Dedicated circuitry that is compliant with PIPE, XAUI, and GIGE
  - Built-in byte ordering so that a frame or packet always starts in a known byte lane
  - Transmitters with two PLL inputs for each transceiver block with independent clock dividers to provide varying clock rates on each of its transmitters

Figure 2–37. ALM in Normal Mode *Note (1)*

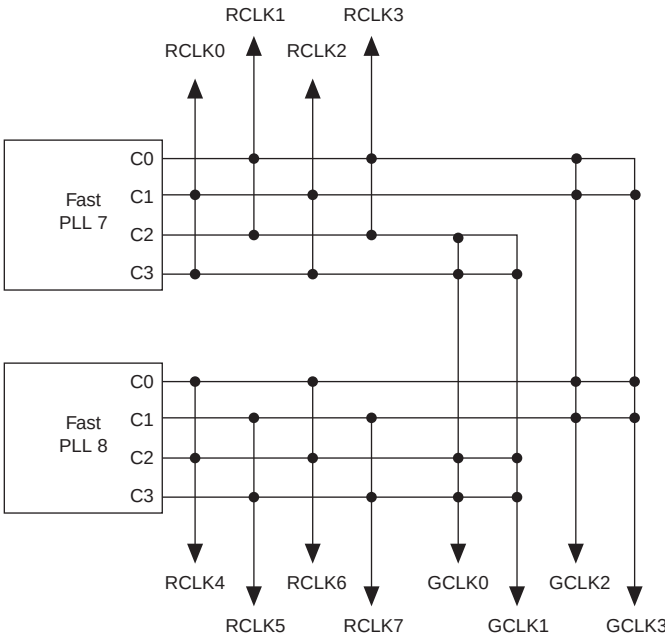


Note to Figure 2–37:

(1) Combinations of functions with less inputs than those shown are also supported. For example, combinations of functions with the following number of inputs are supported: 4 and 3, 3 and 3, 3 and 2, 5 and 2, etc.

The normal mode provides complete backward compatibility with four-input LUT architectures. Two independent functions of four inputs or less can be implemented in one Stratix II GX ALM. In addition, a five-input function and an independent three-input function can be implemented without sharing inputs.

Figure 2–72. Global and Regional Clock Connections from Corner Clock Pins and Fast PLL Outputs Notes (1), (2)



Notes to Figure 2–72:

(1) The global or regional clocks in a fast PLL's quadrant can drive the fast PLL input. A dedicated clock input pin or other PLL must drive the global or regional source. The source cannot be driven by internally generated logic before driving the fast PLL.

(2) EP2SGX30C/D and EP2SGX60C/D devices only have two fast PLLs (1 and 2); they do not contain corner fast PLLs.

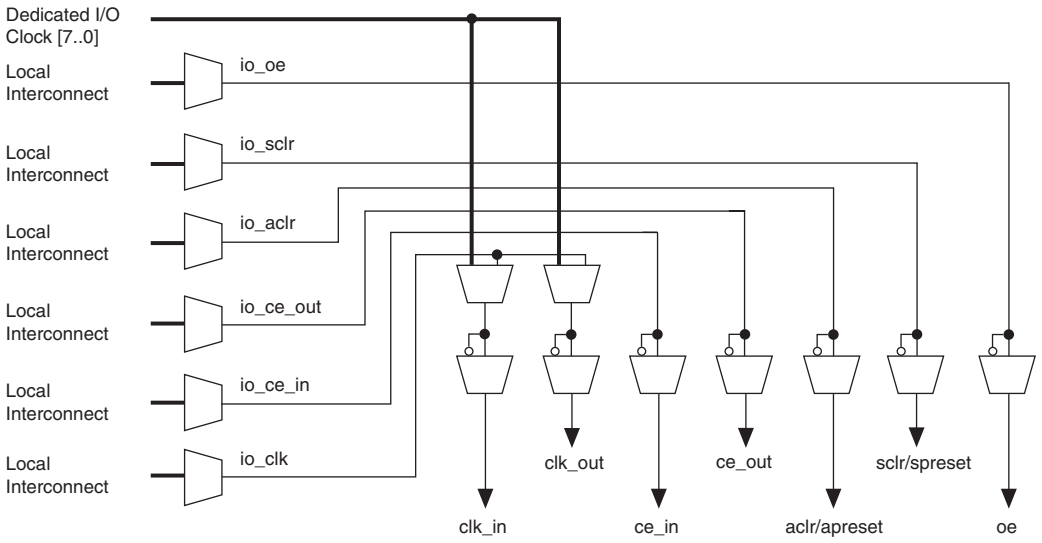
Table 2–27. Global and Regional Clock Connections from Left Side Clock Pins and Fast PLL Outputs (Part 1 of 3)

Left Side Global and Regional Clock Network Connectivity	CLK0	CLK1	CLK2	CLK3	RCLK0	RCLK1	RCLK2	RCLK3	RCLK4	RCLK5	RCLK6	RCLK7
Clock pins												
CLK0p	✓	✓			✓				✓			
CLK1p	✓	✓				✓				✓		
CLK2p			✓	✓			✓				✓	
CLK3p			✓	✓				✓				✓

- Open-drain outputs
- DQ and DQS I/O pins
- Double data rate (DDR) registers

The IOE in Stratix II GX devices contains a bidirectional I/O buffer, six registers, and a latch for a complete embedded bidirectional single data rate or DDR transfer. Figure 2–76 shows the Stratix II GX IOE structure. The IOE contains two input registers (plus a latch), two output registers, and two output enable registers. You can use both input registers and the latch to capture DDR input and both output registers to drive DDR outputs. Additionally, you can use the output enable (OE) register for fast clock-to-output enable timing. The negative edge-clocked OE register is used for DDR SDRAM interfacing. The Quartus II software automatically duplicates a single OE register that controls multiple output or bidirectional pins.

Figure 2–80. Control Signal Selection per IOE *Note (1)*

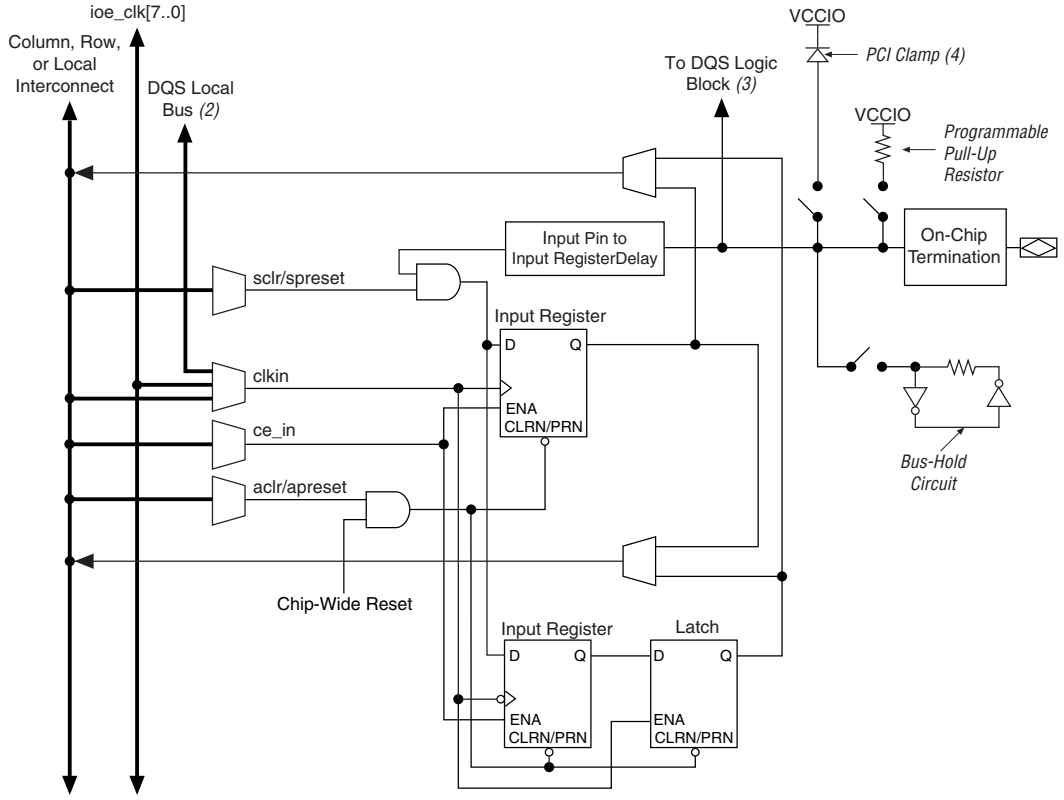


Note to Figure 2–80:

(1) Control signals `ce_in`, `ce_out`, `aclr/apreset`, `sclr/spreset`, and `oe` can be global signals even though their control selection multiplexers are not directly fed by the `ioe_clk[7..0]` signals. The `ioe_clk` signals can drive the I/O local interconnect, which then drives the control selection multiplexers.

In normal bidirectional operation, you can use the input register for input data requiring fast setup times. The input register can have its own clock input and clock enable separate from the OE and output registers. The output register can be used for data requiring fast clock-to-output performance. You can use the OE register for fast clock-to-output enable timing. The OE and output register share the same clock source and the same clock enable source from local interconnect in the associated LAB, dedicated I/O clocks, and the column and row interconnects. Figure 2–81 shows the IOE in bidirectional configuration.

Figure 2–82. Stratix II GX IOE in DDR Input I/O Configuration *Note (1)*



Notes to Figure 2–82:

(1) All input signals to the IOE can be inverted at the IOE.
(2) This signal connection is only allowed on dedicated DQ function pins.
(3) This signal is for dedicated DQS function pins only.
(4) The optional PCI clamp is only available on column I/O pins.

Table 2–33. Stratix II GX Supported I/O Standards

I/O Standard	Type	Input Reference Voltage (V_{REF}) (V)	Output Supply Voltage (V_{CCIO}) (V)	Board Termination Voltage (V_{TT}) (V)
SSTL-2 class I and II	Voltage-referenced	1.25	2.5	1.25

Notes to Table 2–33:
(1) This I/O standard is only available on input and output column clock pins.
(2) This I/O standard is only available on input clock pins and DQS pins in I/O banks 3, 4, 7, and 8, and output clock pins in I/O banks 9,10, 11, and 12.
(3) V_{CCIO} is 3.3 V when using this I/O standard in input and output column clock pins (in I/O banks 3, 4, 7, 8, 9, 10, 11, and 12).
(4) 1.2-V HSTL is only supported in I/O banks 4, 7, and 8.

For more information on I/O standards supported by Stratix II GX I/O banks, refer to the *Selectable I/O Standards in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook*.

Stratix II GX devices contain six I/O banks and four enhanced PLL external clock output banks, as shown in Figure 2–87. The two I/O banks on the left of the device contain circuitry to support source-synchronous, high-speed differential I/O for LVDS inputs and outputs. These banks support all Stratix II GX I/O standards except PCI or PCI-X I/O pins, and SSTL-18 class II and HSTL outputs. The top and bottom I/O banks support all single-ended I/O standards. Additionally, enhanced PLL external clock output banks allow clock output capabilities such as differential support for SSTL and HSTL.

Table 2–36 contains board design recommendations to ensure that nCEO can successfully drive nCE for all power supply combinations.

Table 2–36. Board Design Recommendations for nCEO and nCE Input Buffer Power

nCE Input Buffer Power in I/O Bank 3	Stratix II GX nCEO V_{CCIO} Voltage Level in I/O Bank 7				
	V_{CCIO} = 3.3 V	V_{CCIO} = 2.5 V	V_{CCIO} = 1.8 V	V_{CCIO} = 1.5 V	V_{CCIO} = 1.2 V
VCCSEL high (V_{CCIO} Bank 3 = 1.5 V)	✓ (1), (2)	✓ (3), (4)	✓ (5)	✓	✓
VCCSEL high (V_{CCIO} Bank 3 = 1.8 V)	✓ (1), (2)	✓ (3), (4)	✓	✓	Level shifter required
VCCSEL low (nCE powered by V_{CCPD} = 3.3 V)	✓	✓ (4)	✓ (6)	Level shifter required	Level shifter required

Notes to Table 2–36:
(1) Input buffer is 3.3-V tolerant.
(2) The nCEO output buffer meets V_{OH} (MIN) = 2.4 V.
(3) Input buffer is 2.5-V tolerant.
(4) The nCEO output buffer meets V_{OH} (MIN) = 2.0 V.
(5) Input buffer is 1.8-V tolerant.
(6) An external 250-Ω pull-up resistor is not required, but recommended if signal levels on the board are not optimal.

For JTAG chains, the TDO pin of the first device drives the TDI pin of the second device in the chain. The V_{CCSEL} input on the JTAG input I/O cells (TCK, TMS, TDI, and TRST) is internally hardwired to GND selecting the 3.3-V/2.5-V input buffer powered by V_{CCPD}. The ideal case is to have the V_{CCIO} of the TDO bank from the first device match the V_{CCSEL} settings for TDI on the second device, but that may not be possible depending on the application. Table 2–37 contains board design recommendations to ensure proper JTAG chain operation.

Table 2–37. Supported TDO/TDI Voltage Combinations (Part 1 of 2)

Device	TDI Input Buffer Power	Stratix II GX TDO V_{CCIO} Voltage Level in I/O Bank 4				
		V_{CCIO} = 3.3 V	V_{CCIO} = 2.5 V	V_{CCIO} = 1.8 V	V_{CCIO} = 1.5 V	V_{CCIO} = 1.2 V
Stratix II GX	Always V_{CCPD} (3.3 V)	✓ (1)	✓ (2)	✓ (3)	Level shifter required	Level shifter required

Table 2–37. Supported TDO/TDI Voltage Combinations (Part 2 of 2)

Device	TDI Input Buffer Power	Stratix II GX TDO V_{CCIO} Voltage Level in I/O Bank 4				
		V_{CCIO} = 3.3 V	V_{CCIO} = 2.5 V	V_{CCIO} = 1.8 V	V_{CCIO} = 1.5 V	V_{CCIO} = 1.2 V
Non-Stratix II GX	VCC = 3.3 V	✓ (1)	✓ (2)	✓ (3)	Level shifter required	Level shifter required
	VCC = 2.5 V	✓ (1), (4)	✓ (2)	✓ (3)	Level shifter required	Level shifter required
	VCC = 1.8 V	✓ (1), (4)	✓ (2), (5)	✓	Level shifter required	Level shifter required
	VCC = 1.5 V	✓ (1), (4)	✓ (2), (5)	✓ (6)	✓	✓

Notes to Table 2–37:

(1) The TDO output buffer meets V_{OH} (MIN) = 2.4 V.
(2) The TDO output buffer meets V_{OH} (MIN) = 2.0 V.
(3) An external 250-Ω pull-up resistor is not required, but recommended if signal levels on the board are not optimal.
(4) Input buffer must be 3.3-V tolerant.
(5) Input buffer must be 2.5-V tolerant.
(6) Input buffer must be 1.8-V tolerant.

High-Speed Differential I/O with DPA Support

Stratix II GX devices contain dedicated circuitry for supporting differential standards at speeds up to 1 Gbps. The LVDS differential I/O standards are supported in the Stratix II GX device. In addition, the LVPECL I/O standard is supported on input and output clock pins on the top and bottom I/O banks.

The high-speed differential I/O circuitry supports the following high-speed I/O interconnect standards and applications:

- SPI-4 Phase 2 (POS-PHY Level 4)
- SFI-4
- Parallel RapidIO standard

There are two dedicated high-speed PLLs in the EP2SGX30 device and four dedicated high-speed PLLs in the EP2SGX60, EP2SGX90, and EP2SGX130 devices to multiply reference clocks and drive high-speed differential SERDES channels.

Tables 2–38 through 2–41 show the number of channels that each Fast PLL can clock in each of the Stratix II GX devices. In Tables 2–38 through 2–41, the first row for each transmitter or receiver provides the number of channels driven directly by the PLL. The second row below it shows the maximum channels a Fast PLL can drive if cross bank channels are used from the adjacent center Fast PLL. For example, in the 780-pin FineLine BGA EP2SGX30 device, PLL 1 can drive a maximum of

Table 4–6. Stratix II GX Transceiver Block AC Specification (Part 6 of 6)

Symbol / Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Bandwidth at 6.375 Gbps	BW = Low	-	2	-	-	-	-	-	-	-	MHz
	BW = Med	-	3	-	-	-	-	-	-	-	MHz
	BW = High	-	7	-	-	-	-	-	-	-	MHz
Bandwidth at 3.125 Gbps	BW = Low	-	3	-	-	3	-	-	3	-	MHz
	BW = Med	-	5	-	-	5	-	-	5	-	MHz
	BW = High	-	9	-	-	9	-	-	9	-	MHz
Bandwidth at 2.5 Gbps	BW = Low	-	1	-	-	1	-	-	1	-	MHz
	BW = Med	-	2	-	-	2	--	-	2	-	MHz
	BW = High	-	4	-	-	4	-	-	4	-	MHz
TX PLL lock time from `gxb_powerdown` deassertion *(9)*, *(10)*		-	-	100	-	-	100	-	-	100	us
PLD-Transceiver Interface											
Interface speed		25	-	250	25	-	250	25	-	200	MHz
Digital Reset Pulse Width		Minimum is 2 parallel clock cycles									

Notes to Table 4–6:

(1) The device cannot tolerate prolonged operation at this absolute maximum. Refer to Figure 4–5 for more information.
(2) The rate matcher supports only up to +/-300 ppm.
(3) This parameter is measured by embedding the run length data in a PRBS sequence.
(4) This feature is only available in PCI-Express (PIPE) mode.
(5) Time taken to `rx_pll_locked` goes high from `rx_analogreset` deassertion. Refer to Figure 4–1.
(6) This is how long GXB needs to stay in LTR mode after `rx_pll_locked` is asserted and before `rx_locktodata` is asserted in manual mode. Refer to Figure 4–1.
(7) Time taken to recover valid data from GXB after `rx_locktodata` signal is asserted in manual mode. Measurement results are based on PRBS31, for native data rates only. Refer to Figure 4–1.
(8) Time taken to recover valid data from GXB after `rx_freqlocked` signal goes high in automatic mode. Measurement results are based on PRBS31, for native data rates only. Refer to Figure 4–1.
(9) Please refer to the Protocol Characterization documents for lock times specific to the protocols.
(10) Time taken to lock TX PLL from `gxb_powerdown` deassertion.
(11) The 1.2 V RX V_{ICM} setting is intended for DC-coupled LVDS links.
(12) For AC-coupled links, the on-chip biasing circuit is switched off before and during configuration. Make sure that input specifications are not violated during this period.

Figure 4–4. Transmitter Output Waveform

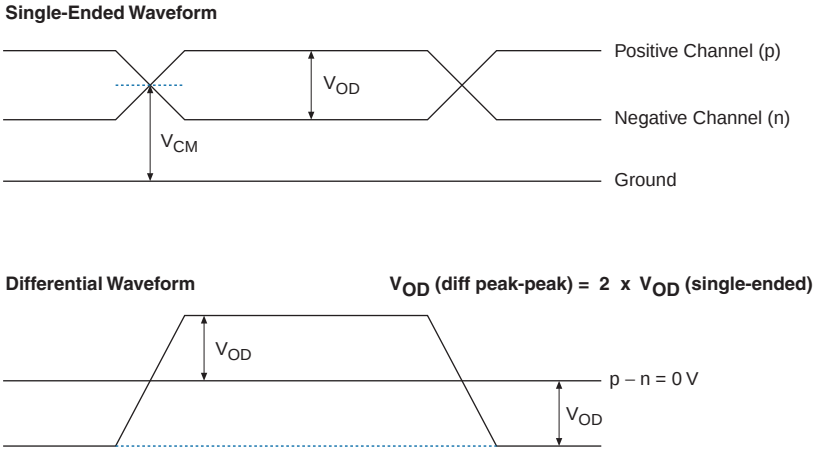
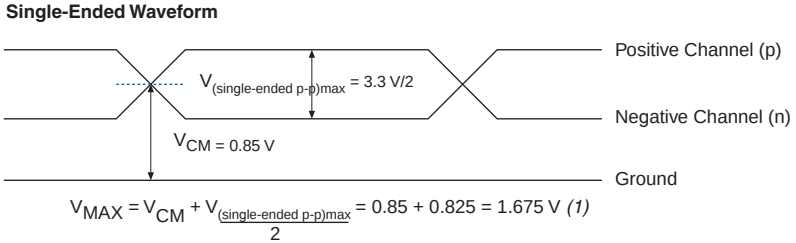


Figure 4–5. Maximum Receiver Input Pin Voltage



Note to Figure 4–5:
(1) The absolute V_{MAX} that the receiver input pins can tolerate is 2 V.

Tables 4–7 through 4–12 show the typical V_{OD} for data rates from 600 Mbps to 6.375 Gbps. The specification is for measurement at the package ball.

Table 4–7. Typical V_{OD} Setting, TX Term = 100 Ω Note (1)

V_{CCH} TX = 1.5 V	V_{OD} Setting (mV)						
	200	400	600	800	1000	1200	1400
V_{OD} Typical (mV)	220	430	625	830	1020	1200	1350

Note to Table 4–7:
(1) Applicable to data rates from 600 Mbps to 6.375 Gbps. Specification is for measurement at the package ball.

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 15 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Sinusoidal Jitter Tolerance (peak-to-peak) *(6)* (cont.)	Jitter Frequency = 20 MHz Data Rate = 614.4 Mbps, 1.2288 Gbps, 2.4576 Gbps REFCLK = 61.44 MHz for 614.4 Mbps REFCLK = 122.88 MHz for 1.2288 Gbps and 2.4576 Gbps Pattern = CJPAT Equalizer Setting = 6 DC Gain = 0 dB	> 0.1			> 0.1			N/A			UI

Table 4–39. SSTL-2 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{IH} (DC)	High-level DC input voltage		V_{REF} + 0.18		V_{CCIO} + 0.3	V
V_{IL} (DC)	Low-level DC input voltage		–0.3		V_{REF} – 0.18	V
V_{IH} (AC)	High-level AC input voltage		V_{REF} + 0.35			V
V_{IL} (AC)	Low-level AC input voltage				V_{REF} – 0.35	V
V_{OH}	High-level output voltage	I_{OH} = –16.4 mA *(1)*	V_{TT} + 0.76			V
V_{OL}	Low-level output voltage	I_{OL} = 16.4 mA *(1)*			V_{TT} – 0.76	V

Note to Table 4–39:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Table 4–40. SSTL-2 Class I and II Differential Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		2.375	2.5	2.625	V
V_{SWING} (DC)	DC differential input voltage		0.36			V
V_X (AC)	AC differential input cross point voltage		(V_{CCIO}/2) – 0.2		(V_{CCIO}/2) + 0.2	V
V_{SWING} (AC)	AC differential input voltage		0.7			V
V_{ISO}	Input clock signal offset voltage			0.5 V_{CCIO}		V
ΔV_{ISO}	Input clock signal offset voltage variation			200		mV
V_{OX} (AC)	AC differential output cross point voltage		(V_{CCIO}/2) – 0.2		(V_{CCIO}/2) + 0.2	V

Table 4–41. 1.2-V HSTL Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.14	1.2	1.26	V
V_{REF}	Reference voltage		0.48 V_{CCIO}	0.5 V_{CCIO}	0.52 V_{CCIO}	V
V_{IH} (DC)	High-level DC input voltage		V_{REF} + 0.08		V_{CCIO} + 0.15	V
V_{IL} (DC)	Low-level DC input voltage		–0.15		V_{REF} – 0.08	V
V_{IH} (AC)	High-level AC input voltage		V_{REF} + 0.15		V_{CCIO} + 0.24	V
V_{IL} (AC)	Low-level AC input voltage		–0.24		V_{REF} – 0.15	V

Table 4–44. 1.5-V HSTL Class I and II Differential Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage		1.425	1.5	1.575	V
V_{DIF} (DC)	DC input differential voltage		0.2			V
V_{CM} (DC)	DC common mode input voltage		0.68		0.9	V
V_{DIF} (AC)	AC differential input voltage		0.4			V
V_{OX} (AC)	AC differential cross point voltage		0.68		0.9	V

Table 4–45. 1.8-V HSTL Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.71	1.80	1.89	V
V_{REF}	Input reference voltage		0.85	0.90	0.95	V
V_{TT}	Termination voltage		0.85	0.90	0.95	V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 8 mA *(1)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OH} = –8 mA *(1)*			0.4	V

Note to Table 4–45:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Bus Hold Specifications

Table 4–48 shows the Stratix II GX device family bus hold specifications.

Table 4–48. Bus Hold Parameters

Parameter	Conditions	V_{CCIO} Level										Unit
		1.2 V		1.5 V		1.8 V		2.5 V		3.3 V		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	$V_{IN} > V_{IL}$ (maximum)	22.5		25		30		50		70		µA
High sustaining current	$V_{IN} < V_{IH}$ (minimum)	–22.5		–25		–30		–50		–70		µA
Low overdrive current	$0 V < V_{IN} < V_{CCIO}$		120		160		200		300		500	µA
High overdrive current	$0 V < V_{IN} < V_{CCIO}$		–120		–160		–200		–300		–500	µA
Bus-hold trip point		0.45	0.95	0.5	1.0	0.68	1.07	0.7	1.7	0.8	2.0	V

On-Chip Termination Specifications

Tables 4–49 and 4–50 define the specification for internal termination resistance tolerance when using series or differential on-chip termination.

Table 4–49. On-Chip Termination Specification for Top and Bottom I/O Banks (Part 1 of 2) *Notes (1), (2)*

Symbol	Description	Conditions	Resistance Tolerance		
			Commercial Max	Industrial Max	Unit
25-Ω R_S 3.3/2.5	Internal series termination with calibration (25-Ω setting)	V_{CCIO} = 3.3/2.5 V	±5	±10	%
	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 3.3/2.5 V	±30	±30	%
50-Ω R_S 3.3/2.5	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 3.3/2.5 V	±5	±10	%
	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 3.3/2.5 V	±30	± 30	%

Table 4–59. M512 Block Internal Timing Microparameters (Part 2 of 2)

Symbol	Parameter	-3 Speed Grade (2)		-3 Speed Grade (3)		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{M512CLR}$	Minimum clear pulse width	144		151		160		192		ps

(1) The M512 block f_{MAX} obtained using the Quartus II software does not necessarily equal to 1/TM512RC.
(2) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
(3) This column refers to –3 speed grades for EP2SGX130 devices.

Table 4–60. M4K Block Internal Timing Microparameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	-3 Speed Grade (2)		-3 Speed Grade (3)		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{M4KRC}	Synchronous read cycle time	1462	2240	1462	2351	1462	2500	1462	3000	ps
$t_{M4KWERESU}$	Write or read enable setup time before clock	22		23		24		29		ps
$t_{M4KWEREH}$	Write or read enable hold time after clock	203		213		226		272		ps
$t_{M4KBESU}$	Byte enable setup time before clock	22		23		24		29		ps
t_{M4KBEH}	Byte enable hold time after clock	203		213		226		272		ps
$t_{M4KDATAASU}$	A port data setup time before clock	22		23		24		29		ps
$t_{M4KDATAAH}$	A port data hold time after clock	203		213		226		272		ps
$t_{M4KADDRASU}$	A port address setup time before clock	22		23		24		29		ps
$t_{M4KADDRAH}$	A port address hold time after clock	203		213		226		272		ps
$t_{M4KDATABSU}$	B port data setup time before clock	22		23		24		29		ps

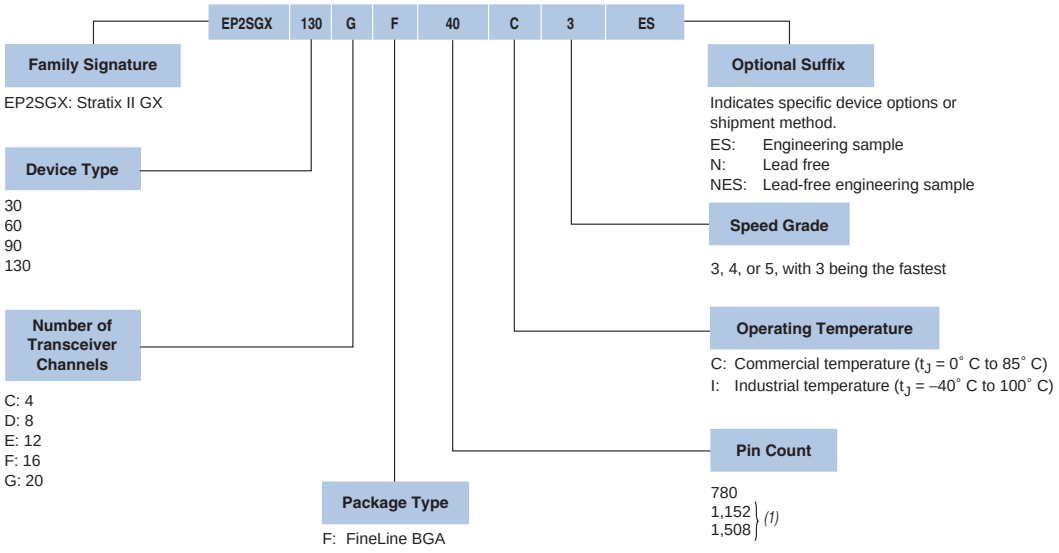
Table 4–93. Stratix II GX Maximum Output Clock Rate for Dedicated Clock Pins (Part 2 of 4)					
I/O Standard	Drive Strength	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
2.5 V	4 mA	230	194	180	MHz
	8 mA	430	380	380	MHz
	12 mA	630	575	550	MHz
	16 mA *(1)*	930	845	820	MHz
1.8 V	2 mA	120	109	104	MHz
	4 mA	285	250	230	MHz
	6 mA	450	390	360	MHz
	8 mA	660	570	520	MHz
	10 mA	905	805	755	MHz
	12 mA *(1)*	1131	1040	990	MHz
1.5 V	2 mA	244	200	180	MHz
	4 mA	470	370	325	MHz
	6 mA	550	430	375	MHz
	8 mA *(1)*	625	495	420	MHz
SSTL-2 Class I	8 mA	400	300	300	MHz
	12 mA *(1)*	400	400	350	MHz
SSTL-2 Class II	16 mA	350	350	300	MHz
	20 mA	400	350	350	MHz
	24 mA *(1)*	400	400	350	MHz
SSTL-18 Class I	4 mA	200	150	150	MHz
	6 mA	350	250	200	MHz
	8 mA	450	300	300	MHz
	10 mA	500	400	400	MHz
	12 mA *(1)*	650	550	400	MHz
SSTL-18 Class II	8 mA	200	200	150	MHz
	16 mA	400	350	350	MHz
	18 mA	450	400	400	MHz
	20 mA *(1)*	550	500	450	MHz
1.8-V HSTL Class I	4 mA	300	300	300	MHz
	6 mA	500	450	450	MHz
	8 mA	650	600	600	MHz
	10 mA	700	650	600	MHz
	12 mA *(1)*	700	700	650	MHz

Table 4–110. Enhanced PLL Specifications (Part 2 of 2)					
Name	**Description**	**Min**	**Typ**	**Max**	**Unit**
f_{VCO}	PLL VCO operating range for –3 and –4 speed grade devices	300		1,040	MHz
	PLL VCO operating range for –5 speed grade devices	300		840	MHz
f_{SS}	Spread-spectrum modulation frequency	100		500	kHz
% spread	Percent down spread for a given clock frequency	0.4	0.5	0.6	%
t_{PLL_PSERR}	Accuracy of PLL phase shift			±30	ps
t_{ARESET}	Minimum pulse width on `areset` signal.	10			ns
$t_{ARESET\_RECONFIG}$	Minimum pulse width on the `areset` signal when using PLL reconfiguration. Reset the PLL after `scandone` goes high.	500			ns
$t_{RECONFIGWAIT}$	The time required for the wait after the reconfiguration is done and the areset is applied.			2	us

(1) This is limited by the I/O f_{MAX}. See Tables 4–91 through 4–95 for the maximum.
(2) If the counter cascading feature of the PLL is utilized, there is no minimum output clock frequency.

Table 4–111. Fast PLL Specifications (Part 1 of 2)					
Name	**Description**	**Min**	**Typ**	**Max**	**Unit**
f_{IN}	Input clock frequency (for -3 and -4 speed grade devices)	16		717	MHz
	Input clock frequency (for -5 speed grade devices)	16		640	MHz
f_{INPFD}	Input frequency to the PFD	16		500	MHz
f_{INDUTY}	Input clock duty cycle	40		60	%
$t_{INJITTER}$	Input clock jitter tolerance in terms of period jitter. Bandwidth ≤2 MHz		0.5		ns (p-p)
	Input clock jitter tolerance in terms of period jitter. Bandwidth > 0.2 MHz		1.0		ns (p-p)

Figure 5–1. Stratix II GX Device Packaging Ordering Information



(1) Product code notations for ES silicon for all EP2SGX130 family members (standard and lead free) and EP2SGX90 (lead free) use the following codings to denote pin count: 35 for 1152-pin devices and 40 for 1508-pin devices

Referenced Documents

This chapter references the following documents:

- *Package Information for Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook*
- *Pin-Out Files for Altera Devices*
- *Quartus II Development Software Handbook*

Document Revision History

Table 5–1 shows the revision history for this chapter.

Table 5–1. Document Revision History (Part 1 of 2)

Date and Document Version	Changes Made	Summary of Changes
August 2007 v1.3	Added the "Referenced Documents" section.	
	Minor text edits.	