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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3022
Number of Logic Elements/Cells	60440
Total RAM Bits	2544192
Number of I/O	534
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2sgx60ef1152i4

Transceiver Clocking

Each Stratix II GX device transceiver block contains two transmitter PLLs and four receiver PLLs. These PLLs can be driven by either of the two reference clocks per transceiver block. These REFCLK signals can drive all global clocks, transmitter PLL inputs, and all receiver PLL inputs. Subsequently, the transmitter PLL output can only drive global clock lines and the receiver PLL reference clock port. Only one of the two reference clocks in a quad can drive the Inter Quad (I/Q) lines to clock the PLLs in the other quads.

Figure 2–29 shows the inter-transceiver line connections as well as the global clock connections for the EP2SGX130 device.

Table 2–16. Reset Signal Map to Stratix II GX Blocks

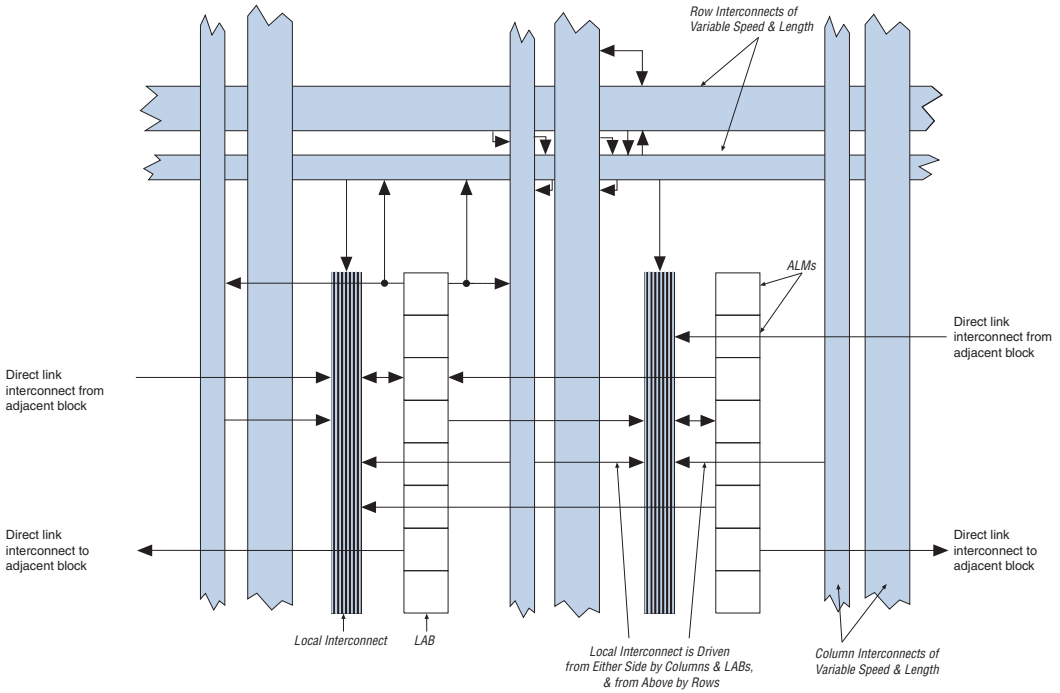
Reset Signal	Transmitter Phase Compensation FIFO Module/ Byte Serializer	Transmitter 8B/10B Encoder	Transmitter Serializer	Transmitter Analog Circuits	Transmitter PLL	Transmitter XAUI State Machine	BIST Generators	Receiver Deserializer	Receiver Word Aligner	Receiver Deskew FIFO Module	Receiver Rate Matcher	Receiver 8B/10B Decoder	Receiver Phase Comp FIFO Module/ Byte Deserializer	Receiver PLL / CRU	Receiver XAUI State Machine	BIST Verifiers	Receiver Analog Circuits
rx_digitalreset									✓	✓	✓	✓	✓		✓	✓	
rx_analogreset								✓						✓			✓
tx_digitalreset	✓	✓				✓	✓										
gxb_powerdown	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
gxb_enable	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Voltage Reference Capabilities

Stratix II GX transceivers provide voltage reference and bias circuitry. To set up internal bias for controlling the transmitter output driver voltage swings, as well as to provide voltage and current biasing for other analog circuitry, the device uses an internal bandgap voltage reference of 0.7 V. An external 2-KΩ resistor connected to ground generates a constant bias current (independent of power supply drift, process changes, or temperature variation). An on-chip resistor generates a tracking current that tracks on-chip resistor variation. These currents are mirrored and distributed to the analog circuitry in each channel.

For more information, refer to the *DC and Switching Characteristics* chapter in volume 1 of the *Stratix II GX Handbook*.

Figure 2–32. Stratix II GX LAB Structure



LAB Interconnects

The LAB local interconnect can drive all eight ALMs in the same LAB. It is driven by column and row interconnects and ALM outputs in the same LAB. Neighboring LABs, M512 RAM blocks, M4K RAM blocks, M-RAM blocks, or digital signal processing (DSP) blocks from the left and right can also drive a LAB's local interconnect through the direct link connection. The direct link connection feature minimizes the use of row and column interconnects, providing higher performance and flexibility. Each ALM can drive 24 ALMs through fast local and direct link interconnects.

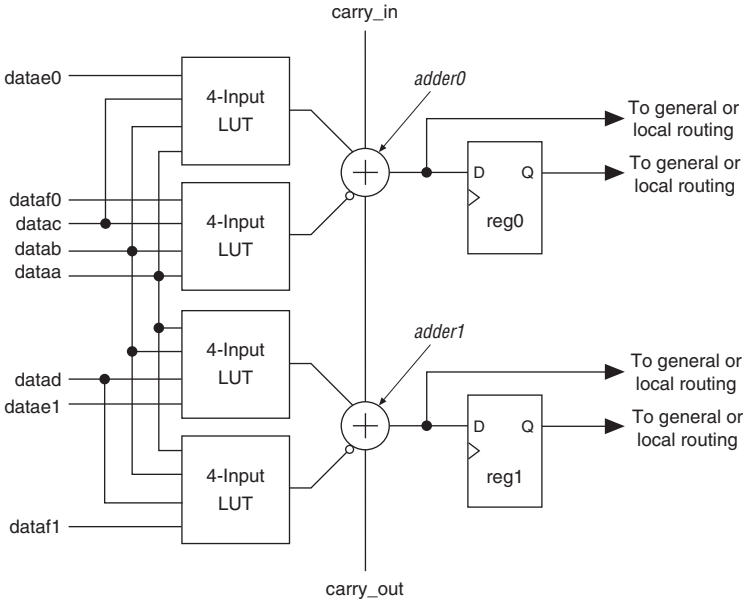
asynchronous clear, asynchronous preset/load, synchronous clear, synchronous load, and clock enable control for the register. These LAB wide signals are available in all ALM modes. Refer to "LAB Control Signals" on page 2–46 for more information on the LAB-wide control signals.

The Quartus II software and supported third-party synthesis tools, in conjunction with parameterized functions such as library of parameterized modules (LPM) functions, automatically choose the appropriate mode for common functions such as counters, adders, subtractors, and arithmetic functions. If required, you can also create special-purpose functions that specify which ALM operating mode to use for optimal performance.

Normal Mode

The normal mode is suitable for general logic applications and combinational functions. In this mode, up to eight data inputs from the LAB local interconnect are inputs to the combinational logic. The normal mode allows two functions to be implemented in one Stratix II GX ALM, or an ALM to implement a single function of up to six inputs. The ALM can support certain combinations of completely independent functions and various combinations of functions which have common inputs. Figure 2–37 shows the supported LUT combinations in normal mode.

Figure 2–41. ALM in Arithmetic Mode



While operating in arithmetic mode, the ALM can support simultaneous use of the adder's carry output along with combinational logic outputs. In this operation, the adder output is ignored. This usage of the adder with the combinational logic output provides resource savings of up to 50% for functions that can use this ability. An example of such functionality is a conditional operation, such as the one shown in Figure 2–42. The equation for this example is:

R = (X < Y) ? Y : X

To implement this function, the adder is used to subtract 'Y' from 'X'. If 'X' is less than 'Y', the `carry_out` signal will be '1'. The `carry_out` signal is fed to an adder where it drives out to the LAB local interconnect. It then feeds to the LAB-wide `syncload` signal. When asserted, `syncload` selects the `syncdata` input. In this case, the data 'Y' drives the `syncdata` inputs to the registers. If 'X' is greater than or equal to 'Y', the `syncload` signal is de-asserted and 'X' drives the data port of the registers.

Table 2–18. Stratix II GX Device Routing Scheme (Part 2 of 2)

Source	Destination															
	Shared Arithmetic Chain	Carry Chain	Register Chain	Local Interconnect	Direct Link Interconnect	R4 Interconnect	R24 Interconnect	C4 Interconnect	C16 Interconnect	ALM	M512 RAM Block	M4K RAM Block	M-RAM Block	DSP Blocks	Column IOE	Row IOE
Column IOE					✓			✓	✓							
Row IOE					✓	✓	✓	✓								

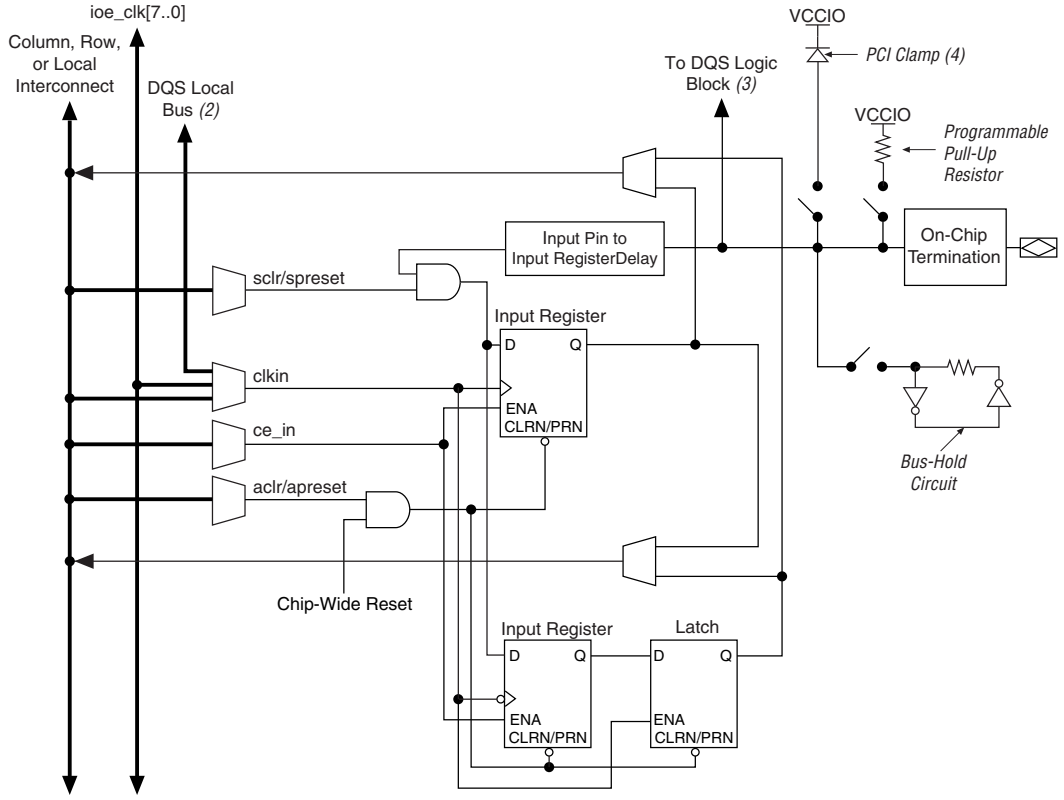
TriMatrix Memory

TriMatrix memory consists of three types of RAM blocks: M512, M4K, and M-RAM. Although these memory blocks are different, they can all implement various types of memory with or without parity, including true dual-port, simple dual-port, and single-port RAM, ROM, and FIFO buffers. Table 2–19 shows the size and features of the different RAM blocks.

Table 2–19. TriMatrix Memory Features (Part 1 of 2)

Memory Feature	M512 RAM Block (32 × 18 Bits)	M4K RAM Block (128 × 36 Bits)	M-RAM Block (4K × 144 Bits)
Maximum performance	500 MHz	550 MHz	420 MHz
True dual-port memory		✓	✓
Simple dual-port memory	✓	✓	✓
Single-port memory	✓	✓	✓
Shift register	✓	✓	
ROM	✓	✓	*(1)*
FIFO buffer	✓	✓	✓
Pack mode		✓	✓
Byte enable	✓	✓	✓
Address clock enable		✓	✓
Parity bits	✓	✓	✓
Mixed clock mode	✓	✓	✓
Memory initialization (**.mif**)	✓	✓	

Figure 2–82. Stratix II GX IOE in DDR Input I/O Configuration *Note (1)*



Notes to Figure 2–82:

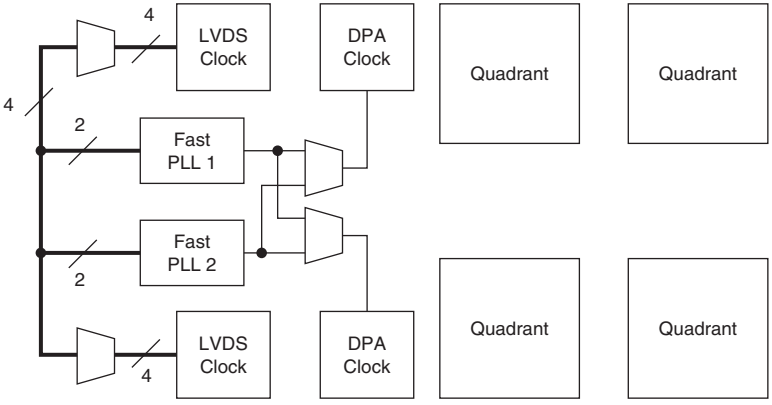
(1) All input signals to the IOE can be inverted at the IOE.
(2) This signal connection is only allowed on dedicated DQ function pins.
(3) This signal is for dedicated DQS function pins only.
(4) The optional PCI clamp is only available on column I/O pins.

For high-speed source synchronous interfaces such as POS-PHY 4 and the Parallel RapidIO standard, the source synchronous clock rate is not a byte- or SERDES-rate multiple of the data rate. Byte alignment is necessary for these protocols because the source synchronous clock does not provide a byte or word boundary since the clock is one half the data rate, not one eighth. The Stratix II GX device's high-speed differential I/O circuitry provides dedicated data realignment circuitry for user-controlled byte boundary shifting. This simplifies designs while saving ALM resources. You can use an ALM-based state machine to signal the shift of receiver byte boundaries until a specified pattern is detected to indicate byte alignment.

Fast PLL and Channel Layout

The receiver and transmitter channels are interleaved such that each I/O bank on the left side of the device has one receiver channel and one transmitter channel per LAB row. Figure 2–90 shows the fast PLL and channel layout in the EP2SGX30C/D and EP2SGX60C/D devices. Figure 2–91 shows the fast PLL and channel layout in EP2SGX60E, EP2SGX90E/F, and EP2SGX130G devices.

Figure 2–90. Fast PLL and Channel Layout in the EP2SGX30C/D and EP2SGX60C/D Devices *Note (1)*



Note to Figure 2–90:
(1) See Table 2–38 for the number of channels each device supports.

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 5 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Peak-to-peak jitter	Jitter frequency = 22.1 KHz		> 8.5			> 8.5			> 8.5		UI
Peak-to-peak jitter	Jitter frequency = 1.875 MHz		> 0.1			> 0.1			> 0.1		UI
Peak-to-peak jitter	Jitter frequency = 20 MHz		> 0.1			> 0.1			> 0.1		UI
PCI Express Transmit Jitter Generation *(10)*											
Total jitter at 2.5 Gbps	Compliance pattern V_{OD} = 800 mV Pre-emphasis (1st post-tap) = Setting 5	-	-	0.25	-	-	0.25	-	-	0.25	UI
PCI Express Receiver Jitter Tolerance *(10)*											
Total jitter at 2.5 Gbps	Compliance pattern No Equalization DC gain = 3 dB		> 0.6			> 0.6			> 0.6		UI
Serial RapidIO Transmit Jitter Generation *(11)*											
Deterministic Jitter (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps REFCLK = 125 MHz Pattern = CJPAT V_{OD} = 800 mV No Pre-emphasis	-	-	0.17	-	-	0.17	-	-	0.17	UI
Total Jitter (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps REFCLK = 125 MHz Pattern = CJPAT V_{OD} = 800 mV No Pre-emphasis	-	-	0.35	-	-	0.35	-	-	0.35	UI

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 6 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Serial RapidIO Receiver Jitter Tolerance *(11)*											
Deterministic Jitter Tolerance (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps REFCLK = 125 MHz Pattern = CJPAT Equalizer Setting = 0 for 1.25 Gbps Equalizer Setting = 6 for 2.5 Gbps Equalizer Setting = 6 for 3.125 Gbps	> 0.37			> 0.37			> 0.37			UI
Combined Deterministic and Random Jitter Tolerance (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps REFCLK = 125 MHz Pattern = CJPAT Equalizer Setting = 0 for 1.25 Gbps Equalizer Setting = 6 for 2.5 Gbps Equalizer Setting = 6 for 3.125 Gbps	> 0.55			> 0.55			> 0.55			UI

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 13 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
CPRI Receiver Jitter Tolerance *(15)*											
Deterministic Jitter Tolerance (peak-to-peak)	Data Rate = 614.4 Mbps, 1.2288 Gbps, 2.4576 Gbps REFCLK = 61.44 MHz for 614.4 Mbps REFCLK = 122.88 MHz for 1.2288 Gbps and 2.4576 Gbps Pattern = CJPAT Equalizer Setting = 6 DC Gain = 0 dB		> 0.4			> 0.4			N/A		UI
Combined Deterministic and Random Jitter Tolerance (peak-to-peak)	Data Rate = 614.4 Mbps, 1.2288 Gbps, 2.4576 Gbps REFCLK = 61.44 MHz for 614.4 Mbps REFCLK = 122.88 MHz for 1.2288 Gbps and 2.4576 Gbps Pattern = CJPAT Equalizer Setting = 6 DC Gain = 0 dB		> 0.66			> 0.66			N/A		UI

Figures 4–6 and 4–7 show receiver input and transmitter output waveforms, respectively, for all differential I/O standards (LVDS and LVPECL).

Figure 4–6. Receiver Input Waveforms for Differential I/O Standards

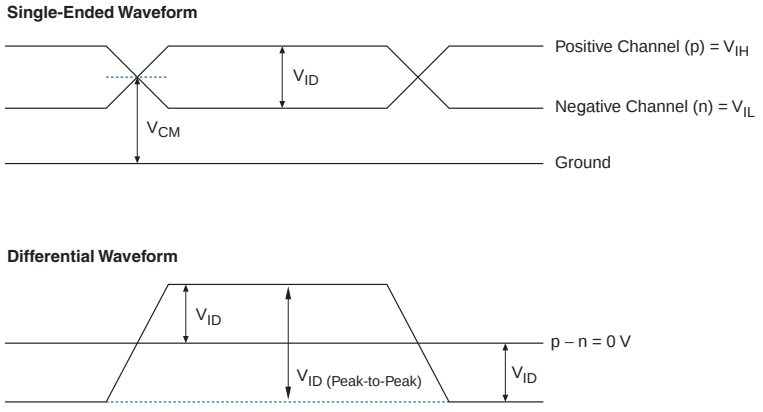
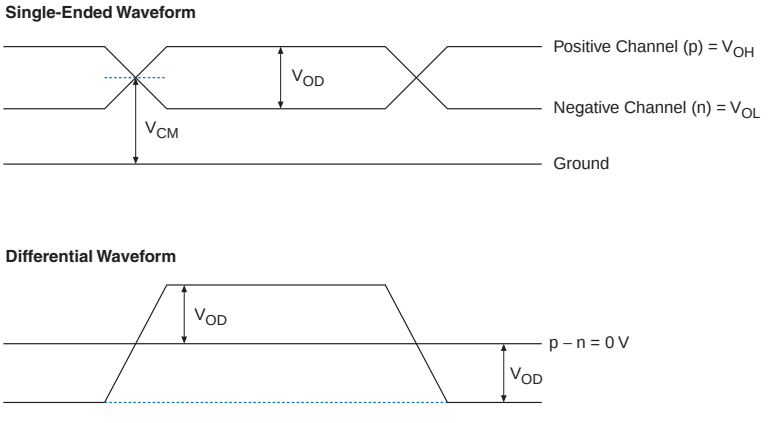
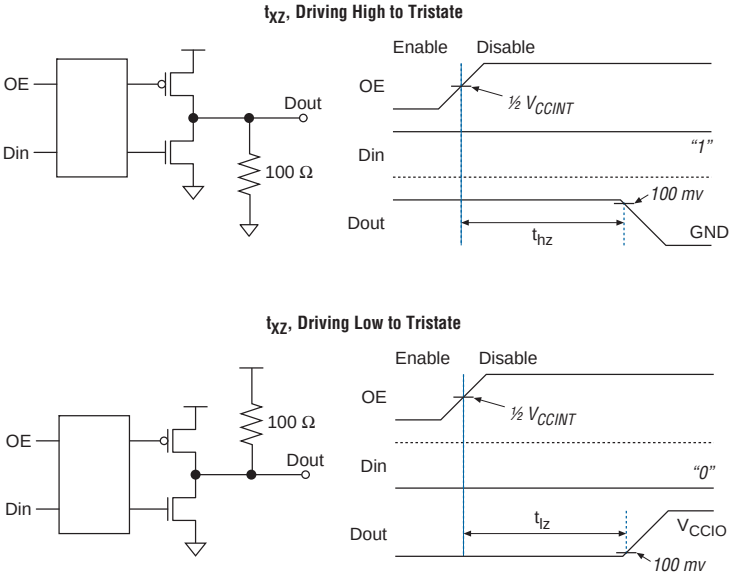


Figure 4–7. Transmitter Output Waveforms for Differential I/O Standards



Figures 4–9 and 4–10 show the measurement setup for output disable and output enable timing.

Figure 4–9. Measurement Setup for t_{xz} *Note (1)*



Note to Figure 4–9:

(1) V_{CCINT} is 1.12 V for this measurement.

Table 4–74. EP2SGX90 Row Pins Regional Clock Timing Parameters						
Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.444	1.461	2.792	3.108	3.716	ns
t_{COUT}	1.449	1.466	2.792	3.108	3.716	ns
t_{PLLCIN}	-0.348	-0.333	0.204	0.217	0.243	ns
$t_{PLLCOUT}$	-0.343	-0.328	0.212	0.217	0.254	ns

EP2SGX130 Clock Timing Parameters

Tables 4–75 through 4–78 show the maximum clock timing parameters for EP2SGX130 devices.

Table 4–75. EP2SGX130 Column Pins Global Clock Timing Parameters						
Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.980	1.998	3.491	3.706	4.434	ns
t_{COUT}	1.815	1.833	3.237	3.436	4.110	ns
t_{PLLCIN}	-0.027	-0.009	0.307	0.322	0.376	ns
$t_{PLLCOUT}$	-0.192	-0.174	0.053	0.052	0.052	ns

Table 4–76. EP2SGX130 Row Pins Global Clock Timing Parameters						
Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.741	1.759	3.112	3.303	3.950	ns
t_{COUT}	1.746	1.764	3.108	3.299	3.945	ns
t_{PLLCIN}	-0.261	-0.243	-0.089	-0.099	-0.129	ns
$t_{PLLCOUT}$	-0.256	-0.238	-0.093	-0.103	-0.134	ns

Table 4–85. Stratix II GX I/O Input Delay for Row Pins (Part 3 of 3)

I/O Standard	Parameter	Fast Corner Industrial/ Commercial	-3 Speed Grade *(2)*	-3 Speed Grade *(3)*	-4 Speed Grade	-5 Speed Grade	Unit
Differential SSTL-18 Class I	t_{PI}	605	960	1006	1070	1285	ps
	t_{PCOUT}	266	433	454	483	580	ps
Differential SSTL-18 Class II	t_{PI}	605	960	1006	1070	1285	ps
	t_{PCOUT}	266	433	454	483	580	ps
1.8-V differential HSTL Class I	t_{PI}	605	960	1006	1070	1285	ps
	t_{PCOUT}	266	433	454	483	580	ps
1.8-V differential HSTL Class II	t_{PI}	605	960	1006	1070	1285	ps
	t_{PCOUT}	266	433	454	483	580	ps
1.5-V differential HSTL Class I	t_{PI}	631	1056	1107	1177	1413	ps
	t_{PCOUT}	292	529	555	590	708	ps
1.5-V differential HSTL Class II	t_{PI}	631	1056	1107	1177	1413	ps
	t_{PCOUT}	292	529	555	590	708	ps

(1) The parameters are only available on the left side of the device.
(2) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
(3) This column refers to –3 speed grades for EP2SGX130 devices.

Table 4–87. Stratix II GX I/O Output Delay for Row Pins (Part 2 of 4)								
I/O Standard	Drive Strength	Parameter	Fast Corner Industrial/ Commercial	-3 Speed Grade (3)	-3 Speed Grade (4)	-4 Speed Grade	-5 Speed Grade	Unit
LVCMOS	4 mA	t_{OP}	1200	2113	2217	2357	2549	ps
		t_{DIP}	1157	2058	2160	2297	2476	ps
	8 mA (1)	t_{OP}	1094	1853	1944	2067	2243	ps
		t_{DIP}	1051	1798	1887	2007	2170	ps
	12 mA (1)	t_{OP}	1061	1723	1808	1922	2089	ps
		t_{DIP}	1018	1668	1751	1862	2016	ps
2.5 V	4 mA	t_{OP}	1183	2091	2194	2332	2523	ps
		t_{DIP}	1140	2036	2137	2272	2450	ps
	8 mA	t_{OP}	1080	1872	1964	2088	2265	ps
		t_{DIP}	1037	1817	1907	2028	2192	ps
	12 mA (1)	t_{OP}	1061	1775	1862	1980	2151	ps
		t_{DIP}	1018	1720	1805	1920	2078	ps
1.8 V	2 mA	t_{OP}	1253	2954	3100	3296	3542	ps
		t_{DIP}	1210	2899	3043	3236	3469	ps
	4 mA	t_{OP}	1242	2294	2407	2559	2763	ps
		t_{DIP}	1199	2239	2350	2499	2690	ps
	6 mA	t_{OP}	1131	2039	2140	2274	2462	ps
		t_{DIP}	1088	1984	2083	2214	2389	ps
	8 mA (1)	t_{OP}	1100	1942	2038	2166	2348	ps
		t_{DIP}	1057	1887	1981	2106	2275	ps
1.5 V	2 mA	t_{OP}	1213	2530	2655	2823	3041	ps
		t_{DIP}	1170	2475	2598	2763	2968	ps
	4 mA (1)	t_{OP}	1106	2020	2120	2253	2440	ps
		t_{DIP}	1063	1965	2063	2193	2367	ps
SSTL-2 Class I	8 mA	t_{OP}	1050	1759	1846	1962	2104	ps
		t_{DIP}	1007	1704	1789	1902	2031	ps
	12 mA (1)	t_{OP}	1026	1694	1777	1889	2028	ps
		t_{DIP}	983	1639	1720	1829	1955	ps
SSTL-2 Class II	16 mA (1)	t_{OP}	992	1581	1659	1763	1897	ps
		t_{DIP}	949	1526	1602	1703	1824	ps

Table 4–87. Stratix II GX I/O Output Delay for Row Pins (Part 3 of 4)

I/O Standard	Drive Strength	Parameter	Fast Corner Industrial/ Commercial	-3 Speed Grade *(3)*	-3 Speed Grade *(4)*	-4 Speed Grade	-5 Speed Grade	Unit
SSTL-18 Class I	4 mA	t_{OP}	1038	1709	1793	1906	2046	ps
		t_{DIP}	995	1654	1736	1846	1973	ps
	6 mA	t_{OP}	1042	1648	1729	1838	1975	ps
		t_{DIP}	999	1593	1672	1778	1902	ps
	8 mA	t_{OP}	1018	1633	1713	1821	1958	ps
		t_{DIP}	975	1578	1656	1761	1885	ps
	10 mA *(1)*	t_{OP}	1021	1615	1694	1801	1937	ps
		t_{DIP}	978	1560	1637	1741	1864	ps
1.8-V HSTL Class I	4 mA	t_{OP}	1019	1610	1689	1795	1956	ps
		t_{DIP}	976	1555	1632	1735	1883	ps
	6 mA	t_{OP}	1022	1580	1658	1762	1920	ps
		t_{DIP}	979	1525	1601	1702	1847	ps
	8 mA	t_{OP}	1004	1576	1653	1757	1916	ps
		t_{DIP}	961	1521	1596	1697	1843	ps
	10 mA	t_{OP}	1008	1567	1644	1747	1905	ps
		t_{DIP}	965	1512	1587	1687	1832	ps
	12 mA *(1)*	t_{OP}	999	1566	1643	1746	1904	ps
		t_{DIP}	956	1511	1586	1686	1831	ps
1.5-V HSTL Class I	4 mA	t_{OP}	1018	1591	1669	1774	1933	ps
		t_{DIP}	975	1536	1612	1714	1860	ps
	6 mA	t_{OP}	1021	1579	1657	1761	1919	ps
		t_{DIP}	978	1524	1600	1701	1846	ps
	8 mA *(1)*	t_{OP}	1006	1572	1649	1753	1911	ps
		t_{DIP}	963	1517	1592	1693	1838	ps
Differential SSTL-2 Class I	8 mA	t_{OP}	1050	1759	1846	1962	2104	ps
		t_{DIP}	1007	1704	1789	1902	2031	ps
	12 mA	t_{OP}	1026	1694	1777	1889	2028	ps
		t_{DIP}	983	1639	1720	1829	1955	ps
Differential SSTL-2 Class II	16 mA	t_{OP}	992	1581	1659	1763	1897	ps
		t_{DIP}	949	1526	1602	1703	1824	ps

Table 4–87. Stratix II GX I/O Output Delay for Row Pins (Part 4 of 4)								
I/O Standard	**Drive Strength**	**Parameter**	**Fast Corner Industrial/ Commercial**	**-3 Speed Grade** *(3)*	**-3 Speed Grade** *(4)*	**-4 Speed Grade**	**-5 Speed Grade**	**Unit**
Differential SSTL-18 Class I	4 mA	t_{OP}	1038	1709	1793	1906	2046	ps
		t_{DIP}	995	1654	1736	1846	1973	ps
	6 mA	t_{OP}	1042	1648	1729	1838	1975	ps
		t_{DIP}	999	1593	1672	1778	1902	ps
	8 mA	t_{OP}	1018	1633	1713	1821	1958	ps
		t_{DIP}	975	1578	1656	1761	1885	ps
	10 mA	t_{OP}	1021	1615	1694	1801	1937	ps
		t_{DIP}	978	1560	1637	1741	1864	ps
LVDS *(2)*	-	t_{OP}	1067	1723	1808	1922	2089	ps
		t_{DIP}	1024	1668	1751	1862	2016	ps
HyperTransport	-	t_{OP}	1053	1723	1808	1922	2089	ps
		t_{DIP}	1010	1668	1751	1862	2016	ps

(1) This is the default setting in the Quartus II software.
(2) The parameters are only available on the left side of the device.
(3) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
(4) This column refers to –3 speed grades for EP2SGX130 devices.

Maximum Input and Output Clock Toggle Rate

Maximum clock toggle rate is defined as the maximum frequency achievable for a clock type signal at an I/O pin. The I/O pin can be a regular I/O pin or a dedicated clock I/O pin.

The maximum clock toggle rate is different from the maximum data bit rate. If the maximum clock toggle rate on a regular I/O pin is 300 MHz, the maximum data bit rate for dual data rate (DDR) could be potentially as high as 600 Mbps on the same I/O pin.

Tables 4–88 through 4–90 specify the maximum input clock toggle rates. Tables 4–91 through 4–96 specify the maximum output clock toggle rates at 0 pF load. Table 4–97 specifies the derating factors for the output clock toggle rate for a non 0 pF load.

Table 4–93. Stratix II GX Maximum Output Clock Rate for Dedicated Clock Pins (Part 2 of 4)					
I/O Standard	Drive Strength	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
2.5 V	4 mA	230	194	180	MHz
	8 mA	430	380	380	MHz
	12 mA	630	575	550	MHz
	16 mA *(1)*	930	845	820	MHz
1.8 V	2 mA	120	109	104	MHz
	4 mA	285	250	230	MHz
	6 mA	450	390	360	MHz
	8 mA	660	570	520	MHz
	10 mA	905	805	755	MHz
	12 mA *(1)*	1131	1040	990	MHz
1.5 V	2 mA	244	200	180	MHz
	4 mA	470	370	325	MHz
	6 mA	550	430	375	MHz
	8 mA *(1)*	625	495	420	MHz
SSTL-2 Class I	8 mA	400	300	300	MHz
	12 mA *(1)*	400	400	350	MHz
SSTL-2 Class II	16 mA	350	350	300	MHz
	20 mA	400	350	350	MHz
	24 mA *(1)*	400	400	350	MHz
SSTL-18 Class I	4 mA	200	150	150	MHz
	6 mA	350	250	200	MHz
	8 mA	450	300	300	MHz
	10 mA	500	400	400	MHz
	12 mA *(1)*	650	550	400	MHz
SSTL-18 Class II	8 mA	200	200	150	MHz
	16 mA	400	350	350	MHz
	18 mA	450	400	400	MHz
	20 mA *(1)*	550	500	450	MHz
1.8-V HSTL Class I	4 mA	300	300	300	MHz
	6 mA	500	450	450	MHz
	8 mA	650	600	600	MHz
	10 mA	700	650	600	MHz
	12 mA *(1)*	700	700	650	MHz

Referenced Documents

This chapter references the following documents:

- *Operating Requirements for Altera Devices Data Sheet*
- *PowerPlay Power Analyzer* chapter in volume 3 of the *Quartus II Handbook*.
- *PowerPlay Early Power Estimator (EPE) and Power Analyzer*
- *Quartus II PowerPlay Analysis and Optimization Technology*
- *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*
- *Stratix II GX Transceiver Architecture Overview* chapter in volume 2 of the *Stratix II GX Device Handbook*
- Volume 2, *Stratix II GX Device Handbook*