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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	4548
Number of Logic Elements/Cells	90960
Total RAM Bits	4520448
Number of I/O	558
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2sgx90ef1152c3n

The Stratix® II GX family of devices is Altera's third generation of FPGAs to combine high-speed serial transceivers with a scalable, high-performance logic array. Stratix II GX devices include 4 to 20 high-speed transceiver channels, each incorporating clock and data recovery unit (CRU) technology and embedded SERDES capability at data rates of up to 6.375 gigabits per second (Gbps). The transceivers are grouped into four-channel transceiver blocks and are designed for low power consumption and small die size. The Stratix II GX FPGA technology is built upon the Stratix II architecture and offers a 1.2-V logic array with unmatched performance, flexibility, and time-to-market capabilities. This scalable, high-performance architecture makes Stratix II GX devices ideal for high-speed backplane interface, chip-to-chip, and communications protocol-bridging applications.

Features

This section lists the Stratix II GX device features.

- Main device features:
 - TriMatrix memory consisting of three RAM block sizes to implement true dual-port memory and first-in first-out (FIFO) buffers with performance up to 550 MHz
 - Up to 16 global clock networks with up to 32 regional clock networks per device region
 - High-speed DSP blocks provide dedicated implementation of multipliers (at up to 450 MHz), multiply-accumulate functions, and finite impulse response (FIR) filters
 - Up to four enhanced PLLs per device provide spread spectrum, programmable bandwidth, clock switch-over, real-time PLL reconfiguration, and advanced multiplication and phase shifting
 - Support for numerous single-ended and differential I/O standards
 - High-speed source-synchronous differential I/O support on up to 71 channels
 - Support for source-synchronous bus standards, including SPI-4 Phase 2 (POS-PHY Level 4), SFI-4.1, XSBI, UTOPIA IV, NPSI, and CSIX-L1
 - Support for high-speed external memory, including quad data rate (QDR and QDRII) SRAM, double data rate (DDR and DDR2) SDRAM, and single data rate (SDR) SDRAM

Table 1–1. Stratix II GX Device Features (Part 2 of 2)

Feature	EP2SGX30C/D		EP2SGX60C/D/E			EP2SGX90E/F		EP2SGX130/G
	C	D	C	D	E	E	F	G
Package	780-pin FineLine BGA		780-pin FineLine BGA		1,152-pin FineLine BGA	1,152-pin FineLine BGA	1,508-pin FineLine BGA	1,508-pin FineLine BGA

Note to Table 1–1:

- (1) Includes two sets of dual-purpose differential pins that can be used as two additional channels for the differential receiver or differential clock inputs.

Stratix II GX devices are available in space-saving FineLine BGA packages (refer to Table 1–2). All Stratix II GX devices support vertical migration within the same package. Vertical migration means that you can migrate to devices whose dedicated pins, configuration pins, and power pins are the same for a given package across device densities. For I/O pin migration across densities, you must cross-reference the available I/O pins using the device pin-outs for all planned densities of a given package type to identify which I/O pins are migratable. Table 1–3 lists the Stratix II GX device package sizes.

Table 1–2. Stratix II GX Package Options (Pin Counts and Transceiver Channels)

Device	Transceiver Channels	Source-Synchronous Channels		Maximum User I/O Pin Count		
		Receive (1)	Transmit	780-Pin FineLine BGA (29 mm)	1,152-Pin FineLine BGA (35 mm)	1,508-Pin FineLine BGA (40 mm)
EP2SGX30C	4	31	29	361	—	—
EP2SGX60C	4	31	29	364	—	—
EP2SGX30D	8	31	29	361	—	—
EP2SGX60D	8	31	29	364	—	—
EP2SGX60E	12	42	42	—	534	—
EP2SGX90E	12	47	45	—	558	—
EP2SGX90F	16	59	59	—	—	650
EP2SGX130G	20	73	71	—	—	734

Note to Table 1–2:

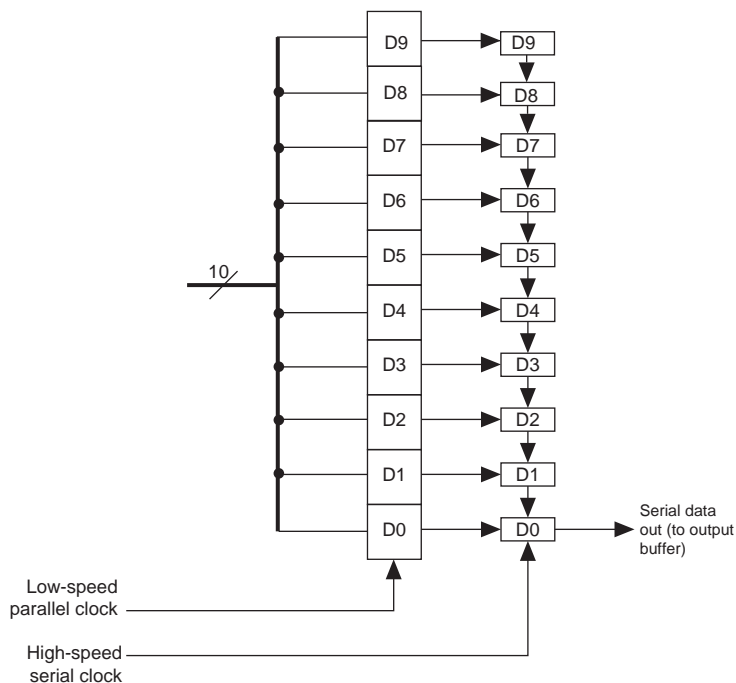
- (1) Includes two differential clock inputs that can also be used as two additional channels for the differential receiver.

Serializer (Parallel-to-Serial Converter)

The serializer converts the parallel 8, 10, 16, or 20-bit data into a serial data bit stream, transmitting the least significant bit (LSB) first. The serialized data stream is then fed to the high-speed differential transmit buffer.

Figure 2-7 is a diagram of the serializer.

Figure 2-7. Serializer *Note (1)*



Note to Figure 2-7:

(1) This is a 10-bit serializer. The serializer can also convert 8, 16, and 20 bits of data.

Transmit Buffer

The Stratix II GX transceiver buffers support the 1.2- and 1.5-V PCML I/O standard at rates up to 6.375 Gbps. The common mode voltage (V_{CM}) of the output driver is programmable. The following V_{CM} values are available when the buffer is in 1.2- and 1.5-V PCML.

- $V_{CM} = 0.6\text{ V}$
- $V_{CM} = 0.7\text{ V}$

The CRU has a built-in switchover circuit to select whether the PLL VCO is aligned by the reference clock or the data. The optional port `rx_freqlocked` monitors when the CRU is in locked-to-data mode.

In the automatic mode, the CRU PLL must be within the prescribed PPM frequency threshold setting of the CRU reference clock for the CRU to switch from locked-to-reference to locked-to-data mode.

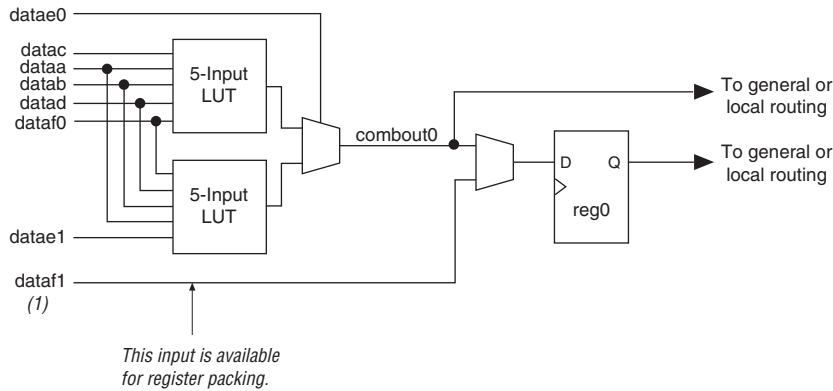
The automatic switchover circuit can be overridden by using the optional ports `rx_locktorefclk` and `rx_locktodata`. Table 2-6 shows the possible combinations of these two signals.

Table 2-6. Receiver Lock Combinations		
rx_locktodata	rx_locktorefclk	VCO (Lock to Mode)
0	0	Auto
0	1	Reference clock
1	x	Data

If the `rx_locktorefclk` and `rx_locktodata` ports are not used, the default is auto mode.

Deserializer (Serial-to-Parallel Converter)

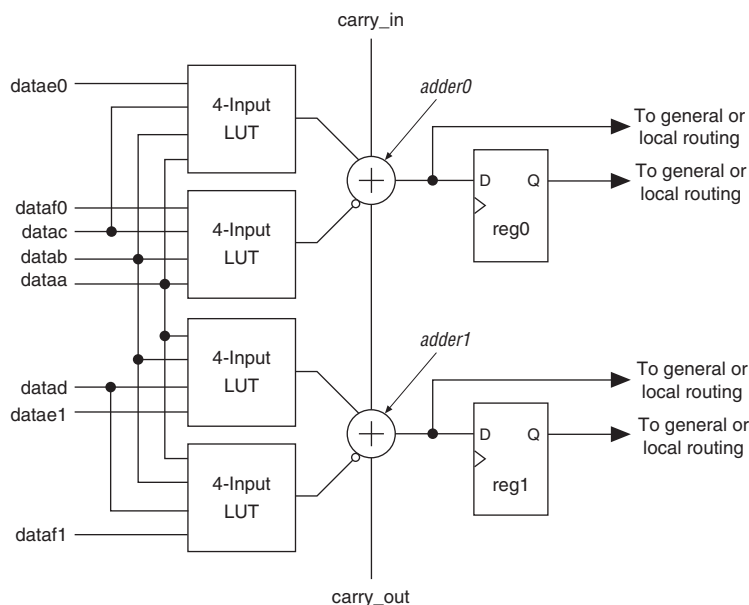
The deserializer converts a serial bitstream into 8, 10, 16, or 20 bits of parallel data. The deserializer receives the LSB first. Figure 2-17 shows the deserializer.

Figure 2–40. Template for Supported Seven-Input Functions in Extended LUT Mode**Note to Figure 2–40:**

- (1) If the seven-input function is un-registered, the unused eighth input is available for register packing. The second register, `reg1`, is not available.

Arithmetic Mode

The arithmetic mode is ideal for implementing adders, counters, accumulators, wide parity functions, and comparators. An ALM in arithmetic mode uses two sets of two four-input LUTs along with two dedicated full adders. The dedicated adders allow the LUTs to be available to perform pre-adder logic; therefore, each adder can add the output of two four-input functions. The four LUTs share the `dataaa` and `datab` inputs. As shown in Figure 2–41, the carry-in signal feeds to `adder0`, and the carry-out from `adder0` feeds to carry-in of `adder1`. The carry-out from `adder1` drives to `adder0` of the next ALM in the LAB. ALMs in arithmetic mode can drive out registered and/or un-registered versions of the adder outputs.

Figure 2–41. ALM in Arithmetic Mode

While operating in arithmetic mode, the ALM can support simultaneous use of the adder's carry output along with combinational logic outputs. In this operation, the adder output is ignored. This usage of the adder with the combinational logic output provides resource savings of up to 50% for functions that can use this ability. An example of such functionality is a conditional operation, such as the one shown in [Figure 2–42](#). The equation for this example is:

$$R = (X < Y) ? Y : X$$

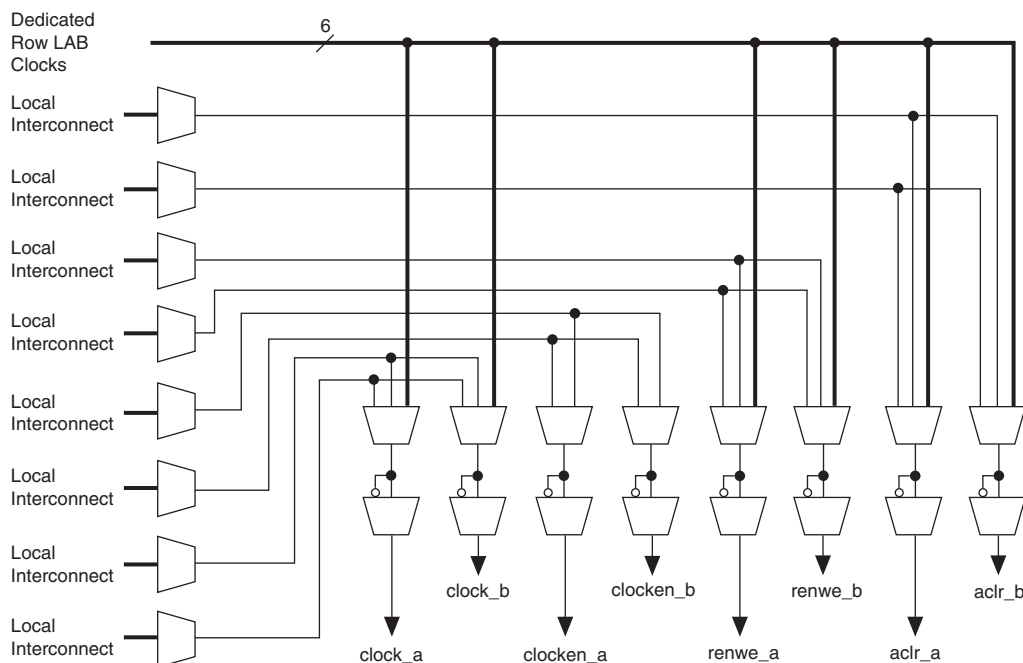
To implement this function, the adder is used to subtract 'Y' from 'X'. If 'X' is less than 'Y', the *carry_out* signal will be '1'. The *carry_out* signal is fed to an adder where it drives out to the LAB local interconnect. It then feeds to the LAB-wide *syncload* signal. When asserted, *syncload* selects the *syncdata* input. In this case, the data 'Y' drives the *syncdata* inputs to the registers. If 'X' is greater than or equal to 'Y', the *syncload* signal is de-asserted and 'X' drives the data port of the registers.

R24 row interconnects span 24 LABs and provide the fastest resource for long row connections between LABs, TriMatrix memory, DSP blocks, and Row IOEs. The R24 row interconnects can cross M-RAM blocks. R24 row interconnects drive to other row or column interconnects at every fourth LAB and do not drive directly to LAB local interconnects. R24 row interconnects drive LAB local interconnects via R4 and C4 interconnects. R24 interconnects can drive R24, R4, C16, and C4 interconnects. The column interconnect operates similarly to the row interconnect and vertically routes signals to and from LABs, TriMatrix memory, DSP blocks, and IOEs. Each column of LABs is served by a dedicated column interconnect.

These column resources include:

- Shared arithmetic chain interconnects in a LAB
- Carry chain interconnects in a LAB and from LAB to LAB
- Register chain interconnects in a LAB
- C4 interconnects traversing a distance of four blocks in an up and down direction
- C16 column interconnects for high-speed vertical routing through the device

Stratix II GX devices include an enhanced interconnect structure in LABs for routing shared arithmetic chains and carry chains for efficient arithmetic functions. The register chain connection allows the register output of one ALM to connect directly to the register input of the next ALM in the LAB for fast shift registers. These ALM-to-ALM connections bypass the local interconnect. The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. [Figure 2–47](#) shows the shared arithmetic chain, carry chain, and register chain interconnects.

Figure 2–51. M4K RAM Block Control Signals

The R4, C4, and direct link interconnects from adjacent LABs drive the M4K RAM block local interconnect. The M4K RAM blocks can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 16 direct link input connections to the M4K RAM block are possible from the left adjacent LABs and another 16 possible from the right adjacent LAB. M4K RAM block outputs can also connect to left and right LABs through direct link interconnect. [Figure 2–52](#) shows the M4K RAM block to logic array interface.

Digital Signal Processing (DSP) Block

The most commonly used DSP functions are finite impulse response (FIR) filters, complex FIR filters, infinite impulse response (IIR) filters, fast Fourier transform (FFT) functions, direct cosine transform (DCT) functions, and correlators. All of these use the multiplier as the fundamental building block. Additionally, some applications need specialized operations such as multiply-add and multiply-accumulate operations. Stratix II GX devices provide DSP blocks to meet the arithmetic requirements of these functions.

Each Stratix II GX device has two to four columns of DSP blocks to efficiently implement DSP functions faster than ALM-based implementations. Stratix II GX devices have up to 24 DSP blocks per column (see [Table 2-21](#)). Each DSP block can be configured to support up to:

- Eight 9×9 -bit multipliers
- Four 18×18 -bit multipliers
- One 36×36 -bit multiplier

As indicated, the Stratix II GX DSP block can support one 36×36 -bit multiplier in a single DSP block, and is true for any combination of signed, unsigned, or mixed sign multiplications.

Table 2–23. DSP Block Signal Sources and Destinations

LAB Row at Interface	Control Signals Generated	Data Inputs	Data Outputs
0	clock0 aclr0 ena0 mult01_saturate addnsub1_round/ accum_round addnsub1 signa sourcea sourceb	A1 [17..0] B1 [17..0]	OA [17..0] OB [17..0]
1	clock1 aclr1 ena1 accum_saturate mult01_round accum_sload sourcea sourceb mode0	A2 [17..0] B2 [17..0]	OC [17..0] OD [17..0]
2	clock2 aclr2 ena2 mult23_saturate addnsub3_round/ accum_round addnsub3 sign_b sourcea sourceb	A3 [17..0] B3 [17..0]	OE [17..0] OF [17..0]
3	clock3 aclr3 ena3 accum_saturate mult23_round accum_sload sourcea sourceb mode1	A4 [17..0] B4 [17..0]	OG [17..0] OH [17..0]

- Differential SSTL-2 class I and II
- 1.2-V HSTL class I and II
- 1.5-V HSTL class I and II
- 1.8-V HSTL class I and II
- SSTL-2 class I and II
- SSTL-18 class I and II

Table 2–33 describes the I/O standards supported by Stratix II GX devices.

Table 2–33. Stratix II GX Supported I/O Standards

I/O Standard	Type	Input Reference Voltage (V_{REF}) (V)	Output Supply Voltage (V_{CCIO}) (V)	Board Termination Voltage (V_{TT}) (V)
LVTTTL	Single-ended	—	3.3	—
LVC MOS	Single-ended	—	3.3	—
2.5 V	Single-ended	—	2.5	—
1.8 V	Single-ended	—	1.8	—
1.5-V LVC MOS	Single-ended	—	1.5	—
3.3-V PCI	Single-ended	—	3.3	—
3.3-V PCI-X mode 1	Single-ended	—	3.3	—
LVDS	Differential	—	2.5 (3)	—
LVPECL (1)	Differential	—	3.3	—
HyperTransport technology	Differential	—	2.5 (3)	—
Differential 1.5-V HSTL class I and II (2)	Differential	0.75	1.5	0.75
Differential 1.8-V HSTL class I and II (2)	Differential	0.90	1.8	0.90
Differential SSTL-18 class I and II (2)	Differential	0.90	1.8	0.90
Differential SSTL-2 class I and II (2)	Differential	1.25	2.5	1.25
1.2-V HSTL (4)	Voltage-referenced	0.6	1.2	0.6
1.5-V HSTL class I and II	Voltage-referenced	0.75	1.5	0.75
1.8-V HSTL class I and II	Voltage-referenced	0.9	1.8	0.9
SSTL-18 class I and II	Voltage-referenced	0.90	1.8	0.90

Table 2–35 summarizes Stratix II GX MultiVolt I/O support.

Table 2–35. Stratix II GX MultiVolt I/O Support <i>Note (1)</i>											
V _{CCIO} (V)	Input Signal (V)					Output Signal (V)					
	1.2	1.5	1.8	2.5	3.3	1.2	1.5	1.8	2.5	3.3	5.0
1.2	(4)	✓ (2)	✓ (2)	✓ (2)	✓ (2)	✓ (4)	—	—	—	—	—
1.5	(4)	✓	✓	✓ (2)	✓ (2)	✓ (3)	✓	—	—	—	—
1.8	(4)	✓	✓	✓ (2)	✓ (2)	✓ (3)	✓ (3)	✓	—	—	—
2.5	(4)	—	—	✓	✓	✓ (3)	✓ (3)	✓ (3)	✓	—	—
3.3	(4)	—	—	✓	✓	✓ (3)	✓ (3)	✓ (3)	✓ (3)	✓	✓

Notes to Table 2–35:

- (1) To drive inputs higher than V_{CCIO} but less than 4.0 V, disable the PCI clamping diode and select the **Allow LVTTTL and LVC MOS input levels to overdrive input buffer** option in the Quartus II software.
- (2) The pin current may be slightly higher than the default value. You must verify that the driving device's V_{OL} maximum and V_{OH} minimum voltages do not violate the applicable Stratix II GX V_{IL} maximum and V_{IH} minimum voltage specifications.
- (3) Although V_{CCIO} specifies the voltage necessary for the Stratix II GX device to drive out, a receiving device powered at a different level can still interface with the Stratix II GX device if it has inputs that tolerate the V_{CCIO} value.
- (4) Stratix II GX devices support 1.2-V HSTL. They do not support 1.2-V LVTTTL and 1.2-V LVC MOS.

The TDO and nCEO pins are powered by V_{CCIO} of the bank that they reside. TDO is in I/O bank 4 and nCEO is in I/O bank 7. Ideally, the V_{CC} supplies for the I/O buffers of any two connected pins are at the same voltage level. This may not always be possible depending on the V_{CCIO} level of TDO and nCEO pins on master devices and the configuration voltage level chosen by V_{CCSEL} on slave devices. Master and slave devices can be in any position in the chain. Master indicates that it is driving out TDO or nCEO to a slave device. For multi-device passive configuration schemes, the nCEO pin of the master device drives the nCE pin of the slave device. The V_{CCSEL} pin on the slave device selects which input buffer is used for nCE. When V_{CCSEL} is logic high, it selects the 1.8-V/1.5-V buffer powered by V_{CCIO}. When V_{CCSEL} is logic low, it selects the 3.3-V/2.5-V input buffer powered by V_{CCPD}. The ideal case is to have the V_{CCIO} of the nCEO bank in a master device match the V_{CCSEL} settings for the nCE input buffer of the slave device it is connected to, but that may not be possible depending on the application.

Table 4–3. Stratix II GX Device Recommended Operating Conditions (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
T_J	Operating junction temperature	For commercial use	0	85	C
		For industrial use	–40	100	C

Notes to Table 4–3:

- (1) Supply voltage specifications apply to voltage readings taken at the device pins, not at the power supply.
- (2) During transitions, the inputs may overshoot to the voltage shown in Table 4–2 based upon the input duty cycle. The DC case is equivalent to 100% duty cycle. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.
- (3) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically from ground to V_{CC} .
- (4) V_{CCPD} must ramp-up from 0 V to 3.3 V within 100 μ s to 100 ms. If V_{CCPD} is not ramped up within this specified time, the Stratix II GX device will not configure successfully. If the system does not allow for a V_{CCPD} ramp-up time of 100 ms or less, hold $nCONFIG$ low until all power supplies are reliable.
- (5) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT} , V_{CCPD} , and V_{CCIO} are powered.
- (6) V_{CCIO} maximum and minimum conditions for PCI and PCI-X are shown in parentheses.

Transceiver Block Characteristics

Tables 4–4 through 4–6 contain transceiver block specifications.

Table 4–4. Stratix II GX Transceiver Block Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{CCA}	Transceiver block supply voltage	Commercial and industrial	–0.5	4.6	V
V_{CCP}	Transceiver block supply voltage	Commercial and industrial	–0.5	1.8	V
V_{CCR}	Transceiver block supply voltage	Commercial and industrial	–0.5	1.8	V
V_{CCT}	Transceiver block supply voltage	Commercial and industrial	–0.5	1.8	V
V_{CCT_B}	Transceiver block supply voltage	Commercial and industrial	–0.5	1.8	V
V_{CCL}	Transceiver block supply voltage	Commercial and industrial	–0.5	1.8	V
V_{CCH_B}	Transceiver block supply voltage	Commercial and industrial	–0.5	2.4	V

Note to Table 4–4:

- (1) The device can tolerate prolonged operation at this absolute maximum, as long as the maximum specification is not violated.

Table 4–19. Stratix II GX Transceiver Block AC Specification *Notes (1), (2), (3) (Part 11 of 19)*

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Combined Deterministic and Random Jitter Tolerance (peak-to-peak)	Data Rate = 6.375 Gbps Pattern = PRBS31 Equalizer Setting = 15 DCGain = 0 dB BER = 10^{-12}	> 0.988			N/A			N/A			UI
Sinusoidal Jitter Tolerance (peak-to-peak)	Jitter Frequency = 38.2 KHz Data Rate = 6.375 Gbps Pattern = PRBS31 Equalizer Setting = 15 DCGain = 0 dB BER = 10^{-12}	> 5			N/A			N/A			UI
	Jitter Frequency = 3.82 MHz Data Rate=6.375 Gbps Pattern = PRBS31 Equalizer Setting = 15 DCGain = 0 dB BER = 10^{-12}	> 0.05			N/A			N/A			UI
	Jitter Frequency = 20 MHz Data Rate = 6.375 Gbps Pattern = PRBS31 Equalizer Setting = 15 DCGain = 0 dB BER = 10^{-12}	> 0.05			N/A			N/A			UI

Table 4–29. 2.5-V LVDS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage for left and right I/O banks (1, 2, 5, and 6)		2.375	2.5	2.625	V
V_{ID}	Input differential voltage swing (single-ended)		100	350	900	mV
V_{ICM}	Input common mode voltage		200	1,250	1,800	mV
V_{OD}	Output differential voltage (single-ended)	$R_L = 100\ \Omega$	250		450	mV
V_{OCM}	Output common mode voltage	$R_L = 100\ \Omega$	1.125		1.375	V
R_L	Receiver differential input discrete resistor (external to Stratix II GX devices)		90	100	110	Ω

Table 4–30. 3.3-V LVDS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO} (1)	I/O supply voltage for top and bottom PLL banks (9, 10, 11, and 12)		3.135	3.3	3.465	V
V_{ID}	Input differential voltage swing (single-ended)		100	350	900	mV
V_{ICM}	Input common mode voltage		200	1,250	1,800	mV
V_{OD}	Output differential voltage (single-ended)	$R_L = 100\ \Omega$	250		710	mV
V_{OCM}	Output common mode voltage	$R_L = 100\ \Omega$	840		1,570	mV
R_L	Receiver differential input discrete resistor (external to Stratix II GX devices)		90	100	110	Ω

Note to Table 4–30:

- (1) The top and bottom clock input differential buffers in I/O banks 3, 4, 7, and 8 are powered by V_{CCINT} , not V_{CCIO} . The PLL clock output/feedback differential buffers are powered by VCC_PLL_OUT . For differential clock output/feedback operation, connect VCC_PLL_OUT to 3.3 V.

Table 4–85. Stratix II GX I/O Input Delay for Row Pins (Part 3 of 3)

I/O Standard	Parameter	Fast Corner Industrial/ Commercial	-3 Speed Grade (2)	-3 Speed Grade (3)	-4 Speed Grade	-5 Speed Grade	Unit
Differential SSTL-18 Class I	t _{PI}	605	960	1006	1070	1285	ps
	t _{PCOUT}	266	433	454	483	580	ps
Differential SSTL-18 Class II	t _{PI}	605	960	1006	1070	1285	ps
	t _{PCOUT}	266	433	454	483	580	ps
1.8-V differential HSTL Class I	t _{PI}	605	960	1006	1070	1285	ps
	t _{PCOUT}	266	433	454	483	580	ps
1.8-V differential HSTL Class II	t _{PI}	605	960	1006	1070	1285	ps
	t _{PCOUT}	266	433	454	483	580	ps
1.5-V differential HSTL Class I	t _{PI}	631	1056	1107	1177	1413	ps
	t _{PCOUT}	292	529	555	590	708	ps
1.5-V differential HSTL Class II	t _{PI}	631	1056	1107	1177	1413	ps
	t _{PCOUT}	292	529	555	590	708	ps

- (1) The parameters are only available on the left side of the device.
(2) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
(3) This column refers to –3 speed grades for EP2SGX130 devices.

Table 4–89. Stratix II GX Maximum Input Clock Rate for Row I/O Pins (Part 2 of 2)

I/O Standard	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
Differential SSTL-2 Class II	500	500	500	MHz
Differential SSTL-18 Class I	500	500	500	MHz
Differential SSTL-18 Class II	500	500	500	MHz
1.8-V differential HSTL Class I	500	500	500	MHz
1.8-V differential HSTL Class II	500	500	500	MHz
1.5-V differential HSTL Class I	500	500	500	MHz
1.5-V differential HSTL Class II	500	500	500	MHz
LVDS (1)	520	520	420	MHz
HyperTransport	520	520	420	MHz

(1) The parameters are only available on the left side of the device.

Table 4–90 shows the maximum input clock toggle rates for Stratix II GX device dedicated clock pins.

Table 4–90. Stratix II GX Maximum Input Clock Rate for Dedicated Clock Pins (Part 1 of 2)

I/O Standard	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
LVTTTL	500	500	400	MHz
2.5 V	500	500	400	MHz
1.8 V	500	500	400	MHz
1.5 V	500	500	400	MHz
LVC MOS	500	500	400	MHz
SSTL-2 Class I	500	500	500	MHz
SSTL-2 Class II	500	500	500	MHz
SSTL-18 Class I	500	500	500	MHz
SSTL-18 Class II	500	500	500	MHz
1.5-V HSTL Class I	500	500	500	MHz
1.5-V HSTL Class II	500	500	500	MHz
1.8-V HSTL Class I	500	500	500	MHz

Table 4–100. Maximum DCD for DDIO Output on Row I/O Pins Without PLL in the Clock Path for -3 Devices
Note (1)

Maximum DCD (ps) for Row DDIO Output I/O Standard	Input I/O Standard (No PLL in Clock Path)					Unit
	TTL/CMOS		SSTL-2	SSTL/HSTL	LVDS	
	3.3 and 2.5 V	1.8 and 1.5 V	2.5 V	1.8 and 1.5 V	3.3 V	
3.3-V LVTTTL	260	380	145	145	110	ps
3.3-V LVCMOS	210	330	100	100	65	ps
2.5 V	195	315	85	85	75	ps
1.8 V	150	265	85	85	120	ps
1.5-V LVCMOS	255	370	140	140	105	ps
SSTL-2 Class I	175	295	65	65	70	ps
SSTL-2 Class II	170	290	60	60	75	ps
SSTL-18 Class I	155	275	55	50	90	ps
1.8-V HSTL Class I	150	270	60	60	95	ps
1.5-V HSTL Class I	150	270	55	55	90	ps
LVDS	180	180	180	180	180	ps

(1) The information in Table 4–100 assumes the input clock has zero DCD.

Here is an example for calculating the DCD in percentage for a DDIO output on a row I/O on a -3 device:

If the input I/O standard is 2.5-V SSTL-2 and the DDIO output I/O standard is SSTL-2 Class= II, the maximum DCD is 60 ps (see Table 4–100). If the clock frequency is 267 MHz, the clock period T is:

$$T = 1 / f = 1 / 267 \text{ MHz} = 3.745 \text{ ns} = 3,745 \text{ ps}$$

Calculate the DCD as a percentage:

$$(T/2 - \text{DCD}) / T = (3,745 \text{ ps}/2 - 60 \text{ ps}) / 3,745 \text{ ps} = 48.4\% \text{ (for low boundary)}$$

$$(T/2 + \text{DCD}) / T = (3,745 \text{ ps}/2 + 60 \text{ ps}) / 3,745 \text{ ps} = 51.6\% \text{ (for high boundary)}$$

Table 4–118. Document Revision History (Part 2 of 5)

Date and Document Version	Changes Made	Summary of Changes
August 2007 v4.4	Removed note “The data in this table is preliminary. Altera will provide a report upon completion of characterization of the Stratix II GX devices. Conditions for testing the silicon have not been determined.” from each table.	
	Removed note “The data in Tables xxx through xxx is preliminary. Altera will provide a report upon completion of characterization of the Stratix II GX devices. Conditions for testing the silicon have not been determined.” in the clock timing parameters sections.	
	Updated clock timing parameter Tables 4–63 through 4–78 (Table 4–75 was unchanged).	
	Updated Table 4–21 and added new Table 4–22.	
	Updated: <ul style="list-style-type: none">● Table 4–6● Table 4–16● Table 4–19● Table 4–49● Table 4–52● Table 4–107	
	Added note to Table 4–50.	
	Added: <ul style="list-style-type: none">● Figure 4–3● Figure 4–4● Figure 4–5	
	Added the “Referenced Documents” section.	
May 2007 v4.3	Changed 1.875 KHz to 1.875 MHz in Table 4–19, XAUI Receiver Jitter Tolerance section.	

