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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	4548
Number of Logic Elements/Cells	90960
Total RAM Bits	4520448
Number of I/O	558
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2sgx90ef1152c4es

There are up to 20 transceiver channels available on a single Stratix II GX device. Table 2–1 shows the number of transceiver channels and their serial bandwidth for each Stratix II GX device.

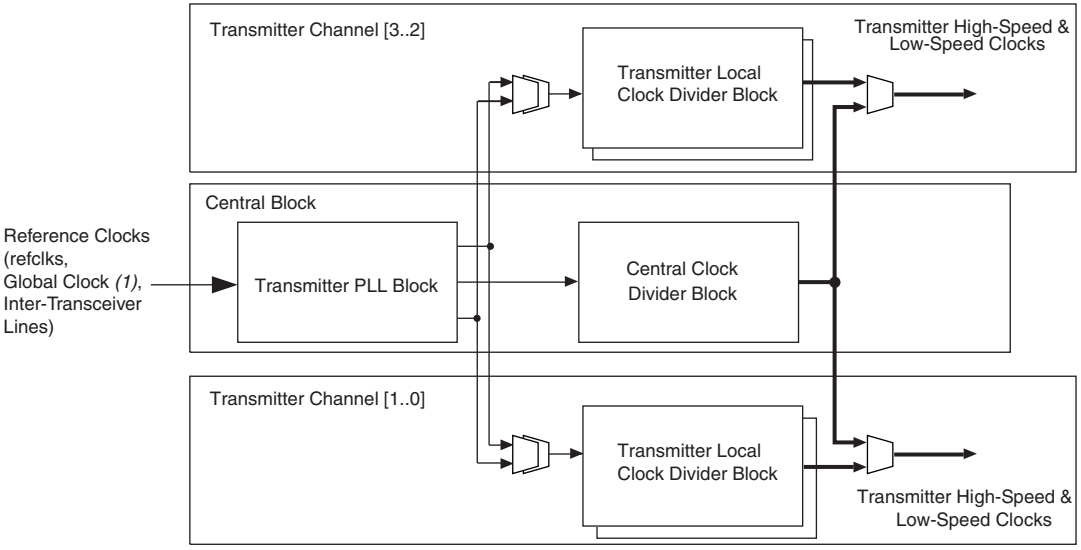
Table 2–1. Stratix II GX Transceiver Channels

Device	Number of Transceiver Channels	Serial Bandwidth (Full Duplex)
EP2SGX30C	4	51 Gbps
EP2SGX60C	4	51 Gbps
EP2SGX30D	8	102 Gbps
EP2SGX60D	8	102 Gbps
EP2SGX60E	12	153 Gbps
EP2SGX90E	12	153 Gbps
EP2SGX90F	16	204 Gbps
EP2SGX130G	20	255 Gbps

Figure 2–2 shows the elements of the transceiver block, including the four transceiver channels, supporting logic, and I/O buffers. Each transceiver channel consists of a receiver and transmitter. The supporting logic contains two transmitter PLLs to generate the high-speed clock(s) used by the four transmitters within that block. Each of the four transmitter channels has its own individual clock divider. The four receiver PLLs within each transceiver block generate four recovered clocks. The transceiver channels can be configured in one of the following functional modes:

- PCI Express (PIPE)
- OIF CEI PHY Interface
- SONET/SDH
- Gigabit Ethernet (GIGE)
- XAUI
- Basic (600 Mbps to 3.125 Gbps single-width mode and 1 Gbps to 6.375 Gbps double-width mode)
- SDI (HD, 3G)
- CPRI (614 Mbps, 1228 Mbps, 2456 Mbps)
- Serial RapidIO (1.25 Gbps, 2.5 Gbps, 3.125 Gbps)

Figure 2–3. Clock Distribution for the Transmitters Note (1)



Note to Figure 2–3:
(1) The global clock line must be driven by an input pin.

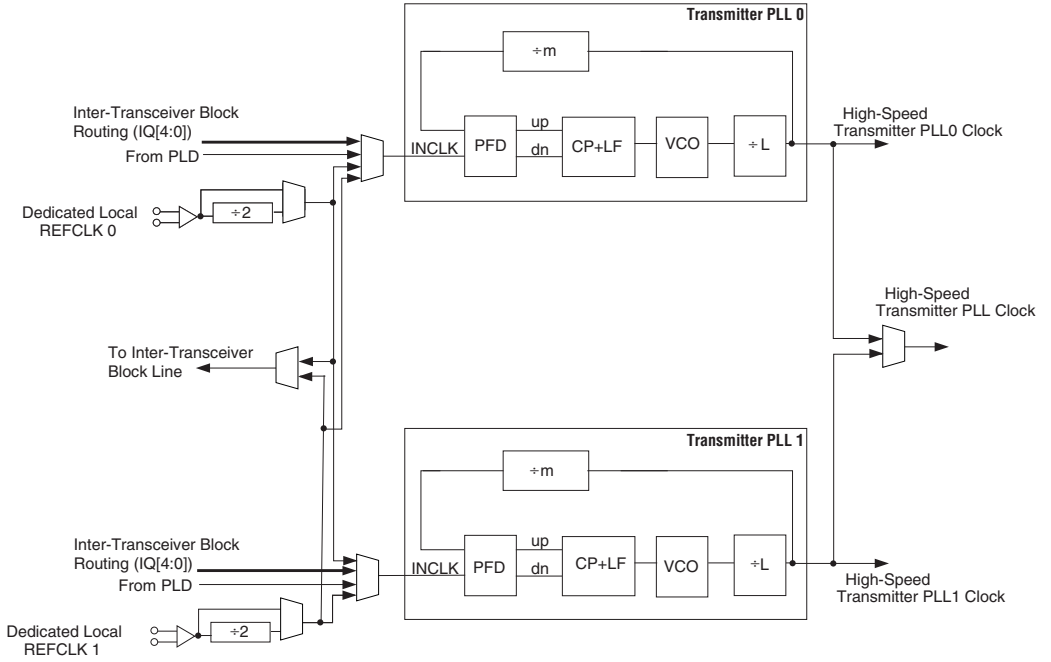
The transmitter PLLs in each transceiver block clock the PMA and PCS circuitry in the transmit path. The Quartus II software automatically powers down the transmitter PLLs that are not used in the design. Figure 2–4 is a block diagram of the transmitter PLL.

The transmitter phase/frequency detector references the clock from one of the following sources:

- Reference clocks
- Reference clock from the adjacent transceiver block
- Inter-transceiver block clock lines
- Global clock line driven by input pin

Two reference clocks, `REFCLK0` and `REFCLK1`, are available per transceiver block. The inter-transceiver block bus allows multiple transceivers to use the same reference clocks. Each transceiver block has one outgoing reference clock which connects to one inter-transceiver block line. The incoming reference clock can be selected from five inter-transceiver block lines `IQ[4..0]` or from the global clock line that is driven by an input pin.

Figure 2–4. Transmitter PLL Block Note (1)



Note to Figure 2–4:
(1) The global clock line must be driven by an input pin.

The transmitter PLLs support data rates up to 6.375 Gbps. The input clock frequency is limited to 622.08 MHz. An optional `pll_locked` port is available to indicate whether the transmitter PLL is locked to the reference clock. Both transmitter PLLs have a programmable loop bandwidth parameter that can be set to low, medium, or high. The loop bandwidth parameter can be statically set in the Quartus II software.

Table 2–2 lists the adjustable parameters in the transmitter PLL.

Table 2–2. Transmitter PLL Specifications

Parameter	Specifications
Input reference frequency range	50 MHz to 622.08 MHz
Data rate support	600 Mbps to 6.375 Gbps
Multiplication factor (W)	1, 4, 5, 8, 10, 16, 20, 25
Bandwidth	Low, medium, or high

Control and Status Signals

The rx_enapatternalign signal is the FPGA control signal that enables word alignment in non-automatic modes. The rx_enapatternalign signal is not used in automatic modes (PCI Express, XAUI, GIGE, CPRI, and Serial RapidIO).

In manual alignment mode, after the rx_enapatternalign signal is activated, the rx_syncstatus signal goes high for one parallel clock cycle to indicate that the alignment pattern has been detected and the word boundary has been locked. If the rx_enapatternalign is deactivated, the rx_syncstatus signal acts as a re-synchronization signal to signify that the alignment pattern has been detected but not locked on a different word boundary.

When using the synchronization state machine, the rx_syncstatus signal indicates the link status. If the rx_syncstatus signal is high, link synchronization is achieved. If the rx_syncstatus signal is low, synchronization has not yet been achieved, or there were enough code group errors to lose synchronization.

In some modes, the rx_enapatternalign signal can be configured to operate as a rising edge signal.

For more information on manual alignment modes, refer to the *Stratix II GX Device Handbook*, volume 2.

When the rx_enapatternalign signal is sensitive to the rising edge, each rising edge triggers a new boundary alignment search, clearing the rx_syncstatus signal.

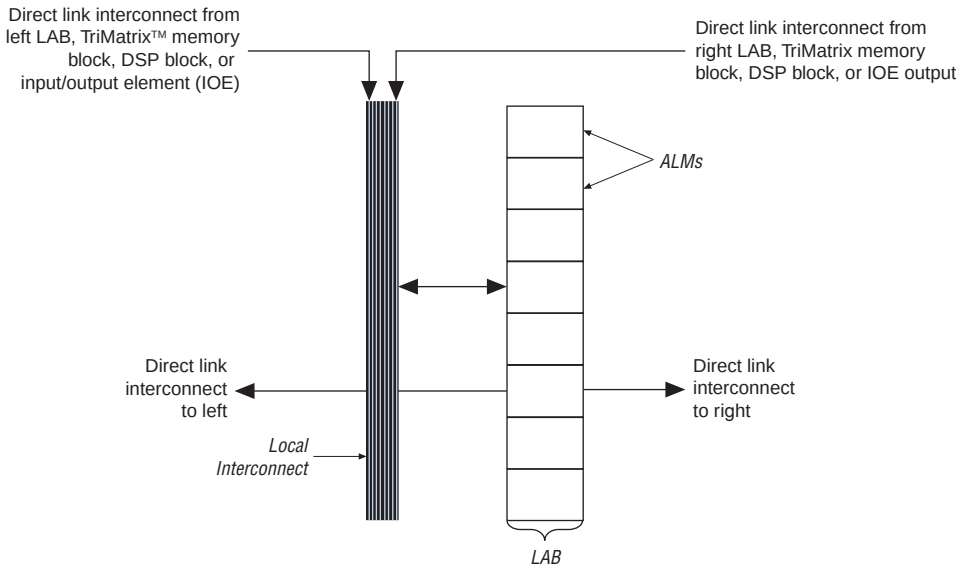
The rx_patterndetect signal pulses high during a new alignment, and also whenever the alignment pattern occurs on the current word boundary.

SONET/SDH

In all the SONET/SDH modes, you can configure the word aligner to either align to A1A2 or A1A1A2A2 patterns. Once the pattern is found, the word boundary is aligned and the word aligner asserts the rx_patterndetect signal for one clock cycle.

Figure 2–33 shows the direct link connection.

Figure 2–33. Direct Link Connection

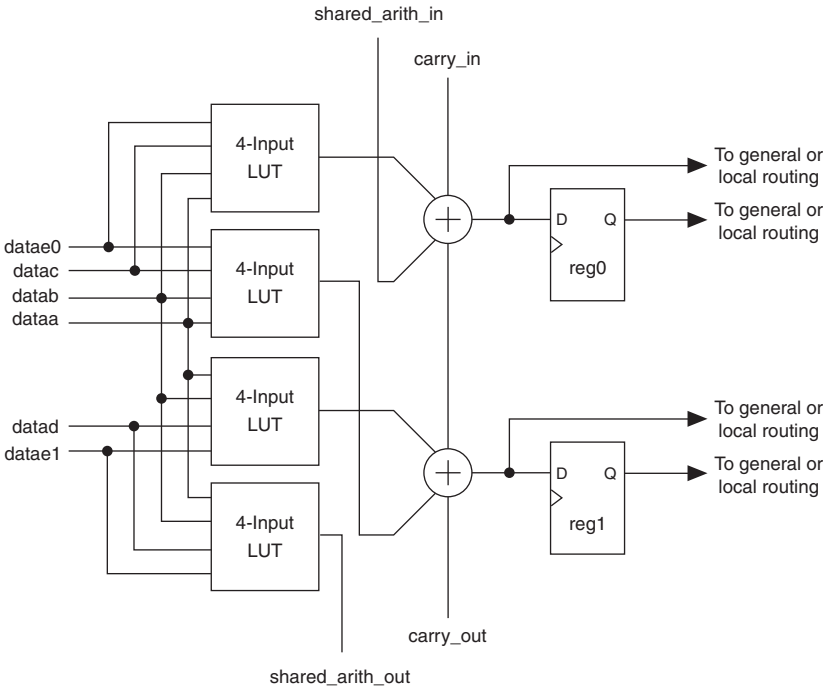


LAB Control Signals

Each LAB contains dedicated logic for driving control signals to its ALMs. The control signals include three clocks, three clock enables, two asynchronous clears, synchronous clear, asynchronous preset/load, and synchronous load control signals, providing a maximum of 11 control signals at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use three clocks and three clock enable signals. However, there can only be up to two unique clocks per LAB, as shown in the LAB control signal generation circuit in Figure 2–34. Each LAB's clock and clock enable signals are linked. For example, any ALM in a particular LAB using the `labclk1` signal also uses `labclkena1`. If the LAB uses both the rising and falling edges of a clock, it also uses two LAB-wide clock signals. De-asserting the clock enable signal turns off the corresponding LAB-wide clock. Each LAB can use two asynchronous clear signals and an asynchronous load/preset signal. The asynchronous

Figure 2–43. ALM in Shared Arithmetic Mode



Note to Figure 2–43:
(1) Inputs `dataf0` and `dataf1` are available for register packing in shared arithmetic mode.

Adder trees are used in many different applications. For example, the summation of the partial products in a logic-based multiplier can be implemented in a tree structure. Another example is a correlator function that can use a large adder tree to sum filtered data samples in a given time frame to recover or to de-spread data which was transmitted utilizing spread spectrum technology. An example of a three-bit add operation utilizing the shared arithmetic mode is shown in Figure 2–44. The partial sum (`S[2..0]`) and the partial carry (`C[2..0]`) is obtained using the LUTs, while the result (`R[2..0]`) is computed using the dedicated adders.

Digital Signal Processing (DSP) Block

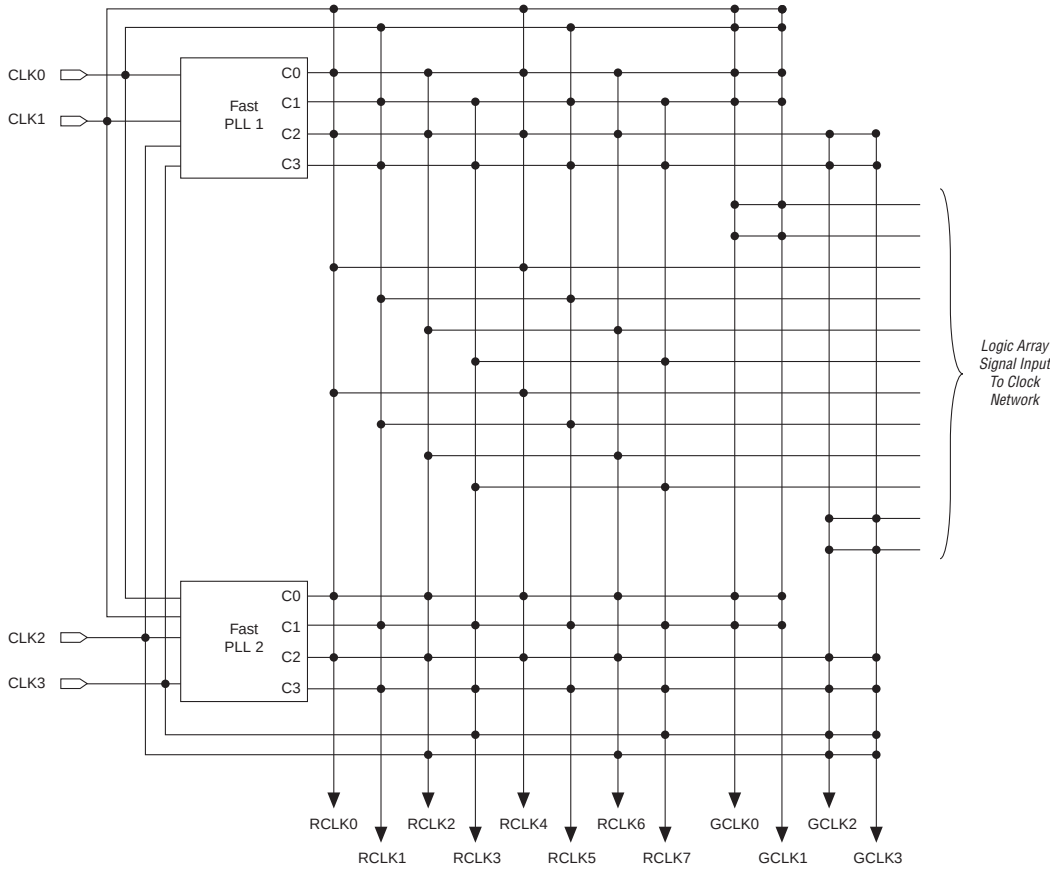
The most commonly used DSP functions are finite impulse response (FIR) filters, complex FIR filters, infinite impulse response (IIR) filters, fast Fourier transform (FFT) functions, direct cosine transform (DCT) functions, and correlators. All of these use the multiplier as the fundamental building block. Additionally, some applications need specialized operations such as multiply-add and multiply-accumulate operations. Stratix II GX devices provide DSP blocks to meet the arithmetic requirements of these functions.

Each Stratix II GX device has two to four columns of DSP blocks to efficiently implement DSP functions faster than ALM-based implementations. Stratix II GX devices have up to 24 DSP blocks per column (see Table 2–21). Each DSP block can be configured to support up to:

- Eight 9 × 9-bit multipliers
- Four 18 × 18-bit multipliers
- One 36 × 36-bit multiplier

As indicated, the Stratix II GX DSP block can support one 36 × 36-bit multiplier in a single DSP block, and is true for any combination of signed, unsigned, or mixed sign multiplications.

Figure 2–71. Global and Regional Clock Connections from Center Clock Pins and Fast PLL Outputs Notes (1), (2)



Notes to Figure 2–71:

(1) EP2SGX30C/D and P2SGX60C/D devices only have two fast PLLs (1 and 2) and two Enhanced PLLs (5 and 6), but the connectivity from these PLLs to the global and regional clock networks remains the same as shown.

(2) The global or regional clocks in a fast PLL's quadrant can drive the fast PLL input. A dedicated clock input pin or other PLL must drive the global or regional source. The source cannot be driven by internally generated logic before driving the fast PLL.

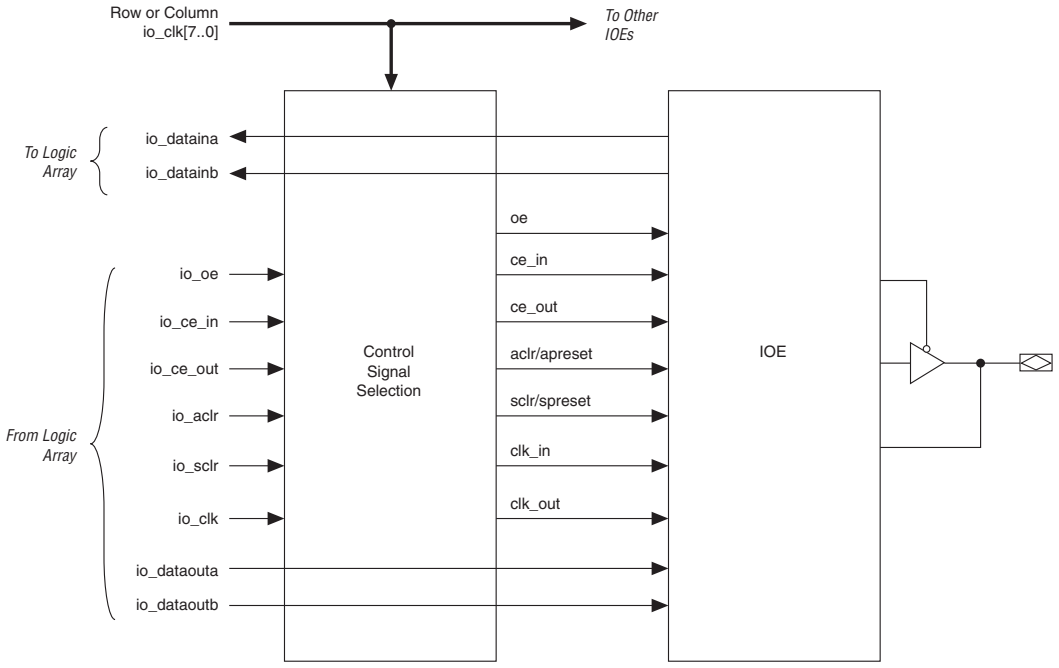
- Open-drain outputs
- DQ and DQS I/O pins
- Double data rate (DDR) registers

The IOE in Stratix II GX devices contains a bidirectional I/O buffer, six registers, and a latch for a complete embedded bidirectional single data rate or DDR transfer. Figure 2–76 shows the Stratix II GX IOE structure. The IOE contains two input registers (plus a latch), two output registers, and two output enable registers. You can use both input registers and the latch to capture DDR input and both output registers to drive DDR outputs. Additionally, you can use the output enable (OE) register for fast clock-to-output enable timing. The negative edge-clocked OE register is used for DDR SDRAM interfacing. The Quartus II software automatically duplicates a single OE register that controls multiple output or bidirectional pins.

There are 32 control and data signals that feed each row or column I/O block. These control and data signals are driven from the logic array. The row or column IOE clocks, `io_clk[7..0]`, provide a dedicated routing resource for low-skew, high-speed clocks. I/O clocks are generated from global or regional clocks. Refer to "PLLs and Clock Networks" on page 2–89 for more information.

Figure 2–79 illustrates the signal paths through the I/O block.

Figure 2–79. Signal Path Through the I/O Block



Each IOE contains its own control signal selection for the following control signals: `oe`, `ce_in`, `ce_out`, `aclr/apreset`, `sclr/spreset`, `clk_in`, and `clk_out`. Figure 2–80 illustrates the control signal selection.

Table 2–34. On-Chip Termination Support by I/O Banks (Part 2 of 2)

On-Chip Termination Support	I/O Standard Support	Top and Bottom Banks (3, 4, 7, 8)	Left Bank (1, 2)
Series termination with calibration	3.3-V LVTTL	✓	—
	3.3-V LVCMOS	✓	—
	2.5-V LVTTL	✓	—
	2.5-V LVCMOS	✓	—
	1.8-V LVTTL	✓	—
	1.8-V LVCMOS	✓	—
	1.5-V LVTTL	✓	—
	1.5-V LVCMOS	✓	—
	SSTL-2 class I and II	✓	—
	SSTL-18 class I and II	✓	—
	1.8-V HSTL class I	✓	—
	1.8-V HSTL class II	✓	—
	1.5-V HSTL class I	✓	—
	1.2-V HSTL	✓	—
Differential termination *(1)*	LVDS	—	✓
	HyperTransport technology	—	✓

Note to Table 2–34:

(1) Clock pins `CLK1` and `CLK3`, and pins `FPLL[7..8]CLK` do not support differential on-chip termination. Clock pins `CLK0` and `CLK2`, do support differential on-chip termination. Clock pins in the top and bottom banks (`CLK[4..7, 12..15]`) do not support differential on-chip termination.

Differential On-Chip Termination

Stratix II GX devices support internal differential termination with a nominal resistance value of 100 for LVDS input receiver buffers. LVPECL input signals (supported on clock pins only) require an external termination resistor. Differential on-chip termination is supported across the full range of supported differential data rates, as shown in the *High-Speed I/O Specifications* section of the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II GX Device Handbook*.

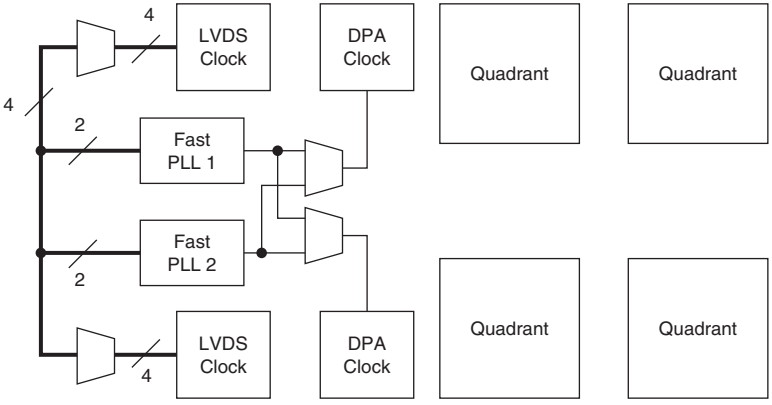
For more information on differential on-chip termination, refer to the *High-Speed Differential I/O Interfaces with DPA in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook*.

For high-speed source synchronous interfaces such as POS-PHY 4 and the Parallel RapidIO standard, the source synchronous clock rate is not a byte- or SERDES-rate multiple of the data rate. Byte alignment is necessary for these protocols because the source synchronous clock does not provide a byte or word boundary since the clock is one half the data rate, not one eighth. The Stratix II GX device's high-speed differential I/O circuitry provides dedicated data realignment circuitry for user-controlled byte boundary shifting. This simplifies designs while saving ALM resources. You can use an ALM-based state machine to signal the shift of receiver byte boundaries until a specified pattern is detected to indicate byte alignment.

Fast PLL and Channel Layout

The receiver and transmitter channels are interleaved such that each I/O bank on the left side of the device has one receiver channel and one transmitter channel per LAB row. Figure 2–90 shows the fast PLL and channel layout in the EP2SGX30C/D and EP2SGX60C/D devices. Figure 2–91 shows the fast PLL and channel layout in EP2SGX60E, EP2SGX90E/F, and EP2SGX130G devices.

Figure 2–90. Fast PLL and Channel Layout in the EP2SGX30C/D and EP2SGX60C/D Devices *Note (1)*



Note to Figure 2–90:
(1) See Table 2–38 for the number of channels each device supports.

Table 3–4. Stratix II GX Configuration Features (Part 2 of 2)

Configuration Scheme	Configuration Method	Design Security	Decompression	Remote System Upgrade
JTAG	Download cable *(4)*			
	MAX II device or microprocessor and flash device			

Notes for Table 3–4:
(1) In these modes, the host system must send a DCLK that is 4× the data rate.
(2) The enhanced configuration device decompression feature is available, while the Stratix II GX decompression feature is not available.
(3) Only remote update mode is supported when using the AS configuration scheme. Local update mode is not supported.
(4) The supported download cables include the Altera USB-Blaster universal serial bus (USB) port download cable, MasterBlaster serial/USB communications cable, ByteBlaster II parallel port download cable, and the ByteBlasterMV parallel port download cable.

Device Security Using Configuration Bitstream Encryption

Stratix II and Stratix II GX FPGAs are the industry's first FPGAs with the ability to decrypt a configuration bitstream using the AES algorithm. When using the design security feature, a 128-bit security key is stored in the Stratix II GX FPGA. To successfully configure a Stratix II GX FPGA that has the design security feature enabled, the device must be configured with a configuration file that was encrypted using the same 128-bit security key. The security key can be stored in non-volatile memory inside the Stratix II GX device. This nonvolatile memory does not require any external devices, such as a battery back up, for storage.

An encrypted configuration file is the same size as a non-encrypted configuration file. When using a serial configuration scheme such as passive serial (PS) or active serial (AS), configuration time is the same whether or not the design security feature is enabled. If the fast passive parallel (FPP) scheme is used with the design security or decompression feature, a 4× DCLK is required. This results in a slower configuration time when compared to the configuration time of an FPGA that has neither the design security nor the decompression feature enabled. For more information about this feature, contact an Altera sales representative.

Device Configuration Data Decompression

Stratix II GX FPGAs support decompression of configuration data, which saves configuration memory space and time. This feature allows you to store compressed configuration data in configuration devices or other

Table 4–19 shows the Stratix II GX transceiver block AC specifications.

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 1 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SONET/SDH Transmit Jitter Generation *(7)*											
Peak-to-peak jitter at 622.08 Mbps	REFCLK = 77.76 MHz Pattern = PRBS23 V_{OD} = 800 mV No Pre-emphasis	-	-	0.1	-	-	0.1	-	-	0.1	UI
RMS jitter at 622.08 Mbps	REFCLK = 77.76 MHz Pattern = PRBS23 V_{OD} = 800 mV No Pre-emphasis	-	-	0.01	-	-	0.01	-	-	0.01	UI
Peak-to-peak jitter at 2488.32 Mbps	REFCLK = 155.52 MHz Pattern = PRBS23 V_{OD} = 800 mV No Pre-emphasis	-	-	0.1	-	-	0.1	-	-	0.1	UI
RMS jitter at 2488.32 Mbps	REFCLK = 155.52 MHz Pattern = PRBS23 V_{OD} = 800 mV No Pre-emphasis	-	-	0.01	-	-	0.01	-	-	0.01	UI

Table 4–20. Recommended Input Clock Jitter (Part 2 of 2)

Mode	Reference Clock (MHz)	Vectron LVPECL XO Type/Model	Frequency Range (MHz)	RMS Jitter (12 kHz to 20 MHz) (ps)	Period Jitter (Peak to Peak) (ps)	Phase Noise at 1 MHz (dB c/Hz)
SONET/SDH OC-48	77.76	VCC6-Q/R	10 to 270	0.3	23	-149.5476
	155.52	VCC6-Q/R	10 to 270	0.3	23	-149.1903
	311.04	VCC6-Q	270 to 800	2	30	Not available
	622.08	VCC6-Q	270 to 800	2	30	Not available
SONET/SDH OC-12	62.2	VCC6-Q/R	10 to 270	0.3	23	-149.6289
	311	VCC6-Q	270 to 800	2	30	Not available
	77.76	VCC6-Q/R	10 to 270	0.3	23	-149.5476
	155.52	VCC6-Q/R	10 to 270	0.3	23	-149.1903
	622.08	VCC6-Q	270 to 800	2	30	Not available

Tables 4–21 and 4–22 show the transmitter and receiver PCS latency for each mode, respectively.

Table 4–21. PCS Latency (Part 1 of 2) *Note (1)*

Functional Mode	Configuration	Transmitter PCS Latency					
		TX PIPE	TX Phase Comp FIFO	Byte Serializer	TX State Machine	8B/10B Encoder	Sum *(2)*
XAUI		-	2-3	1	0.5	0.5	4-5
PIPE	×1, ×4, ×8 8-bit channel width	1	3-4	1	-	1	6-7
	×1, ×4, ×8 16-bit channel width	1	3-4	1	-	0.5	6-7
GIGE		-	2-3	1	-	1	4-5
SONET/SDH	OC-12	-	2-3	1	-	1	4-5
	OC-48	-	2-3	1	-	0.5	4-5
	OC-96	-	2-3	1	-	0.5	4-5
(OIF) CEI PHY		-	2-3	1	-	0.5	4-5
CPRI *(3)*	614 Mbps, 1.228 Gbps	-	2	1	-	1	4
	2.456 Gbps	-	2-3	1	-	1	4-5

Table 4–23. Stratix II GX Device DC Operating Conditions (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Device	Minimum	Typical	Maximum	Unit
R_{CONF} *(4)*	Value of I/O pin pull-up resistor before and during configuration	Vi = 0, V_{CCIO} = 3.3 V		10	25	50	KOhm
		Vi = 0, V_{CCIO} = 2.5 V		15	35	70	KOhm
		Vi = 0, V_{CCIO} = 1.8 V		30	50	100	KOhm
		Vi = 0, V_{CCIO} = 1.5 V		40	75	150	KOhm
		Vi = 0, V_{CCIO} = 1.2 V		50	90	170	KOhm
	Recommended value of I/O pin external pull-down resistor before and during configuration				1	2	KOhm

Notes to Table 4–23:

(1) Typical values are for T_A = 25 °C, V_{CCINT} = 1.2 V, and V_{CCIO} = 1.5 V, 1.8 V, 2.5 V, and 3.3 V.

(2) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3, 2.5, 1.8, and 1.5 V).

(3) Maximum values depend on the actual TJ and design utilization. See *PowerPlay Early Power Estimator (EPE) and Power Analyzer* or the *Quartus II PowerPlay Power Analyzer and Optimization Technology* (available at **www.altera.com**) for maximum values. See the section "Power Consumption" on page 4–59 for more information.

(4) Pin pull-up resistance values will lower if an external source drives the pin higher than V_{CCIO}.

I/O Standard Specifications

Tables 4–24 through 4–47 show the Stratix II GX device family I/O standard specifications.

Table 4–24. LVTTL Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO} *(1)*	Output supply voltage		3.135	3.465	V
V_{IH}	High-level input voltage		1.7	4.0	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	High-level output voltage	I_{OH} = –4 mA *(2)*	2.4		V

Table 4–58. DSP Block Internal Timing Microparameters (Part 2 of 2)

Symbol	Parameter	-3 Speed Grade (1)		-3 Speed Grade (2)		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{INREG2PIPE9}$	Input register to DSP block pipeline register in 9 × 9-bit mode	1312	2030	1312	2131	1312	2266	1312	2720	ps
$t_{INREG2PIPE18}$	Input register to DSP block pipeline register in 18 × 18-bit mode	1302	2010	1302	2110	1302	2244	1302	2693	ps
$t_{INREG2PIPE36}$	Input register to DSP block pipeline register in 36 × 36-bit mode	1302	2010	1302	2110	1302	2244	1302	2693	ps
$t_{PIPE2OUTREG2ADD}$	DSP block pipeline register to output register delay in two-multipliers adder mode	924	1450	924	1522	924	1618	924	1943	ps
$t_{PIPE2OUTREG4ADD}$	DSP block pipeline register to output register delay in four-multipliers adder mode	1134	1850	1134	1942	1134	2065	1134	2479	ps
t_{PD9}	Combinational input to output delay for 9 × 9	2100	2880	2100	3024	2100	3214	2100	3859	ps
t_{PD18}	Combinational input to output delay for 18 × 18	2110	2990	2110	3139	2110	3337	2110	4006	ps
t_{PD36}	Combinational input to output delay for 36 × 36	2939	4450	2939	4672	2939	4967	2939	5962	ps
t_{CLR}	Minimum clear pulse width	2212		2322		2469		2964		ps
t_{CLKL}	Minimum clock low time	1190		1249		1328		1594		ps
t_{CLKH}	Minimum clock high time	1190		1249		1328		1594		ps

(1) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
(2) This column refers to –3 speed grades for EP2SGX130 devices.

Table 4–61. M-RAM Block Internal Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	-3 Speed Grade *(2)*		-3 Speed Grade *(3)*		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{MEGABESU}$	Byte enable setup time before clock	-9		-10		-11		-13		ps
$t_{MEGABEH}$	Byte enable hold time after clock	39		40		43		52		ps
$t_{MEGADATAASU}$	A port data setup time before clock	50		52		55		67		ps
$t_{MEGADATAAH}$	A port data hold time after clock	243		255		271		325		ps
$t_{MEGAADDRASU}$	A port address setup time before clock	589		618		657		789		ps
$t_{MEGAADDRAH}$	A port address hold time after clock	-347		-365		-388		-465		ps
$t_{MEGADATABSU}$	B port setup time before clock	50		52		55		67		ps
$t_{MEGADATABH}$	B port hold time after clock	243		255		271		325		ps
$t_{MEGAADDRBSU}$	B port address setup time before clock	589		618		657		789		ps
$t_{MEGAADDRBH}$	B port address hold time after clock	-347		-365		-388		-465		ps
$t_{MEGADATACO1}$	Clock-to-output delay when using output registers	480	715	480	749	480	797	480	957	ps
$t_{MEGADATACO2}$	Clock-to-output delay without output registers	1950	2899	1950	3042	1950	3235	1950	3884	ps
$t_{MEGACLKL}$	Minimum clock low time	1250		1312		1395		1675		ps
$t_{MEGACLKH}$	Minimum clock high time	1250		1312		1395		1675		ps
$t_{MEGACLR}$	Minimum clear pulse width	144		151		160		192		ps

(1) The M512 block f_{MAX} obtained using the Quartus II software does not necessarily equal to 1/TMEGARC.
(2) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
(3) This column refers to –3 speed grades for EP2SGX130 devices.

Table 4–65. EP2SGX30 Column Pins Regional Clock Timing Parameters

Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.493	1.507	2.522	2.806	3.364	ns
t_{COUT}	1.353	1.372	2.525	2.809	3.364	ns
t_{PLLCIN}	0.087	0.104	0.237	0.253	0.292	ns
$t_{PLLCOUT}$	-0.078	-0.061	0.237	0.253	0.29	ns

Table 4–66. EP2SGX30 Row Pins Regional Clock Timing Parameters

Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.246	1.262	2.437	2.712	3.246	ns
t_{COUT}	1.251	1.267	2.437	2.712	3.246	ns
t_{PLLCIN}	-0.18	-0.167	0.215	0.229	0.263	ns
$t_{PLLCOUT}$	-0.175	-0.162	0.215	0.229	0.263	ns

EP2SGX60 Clock Timing Parameters

Tables 4–67 through 4–70 show the maximum clock timing parameters for EP2SGX60 devices.

Table 4–67. EP2SGX60 Column Pins Global Clock Timing Parameters

Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.722	1.736	2.940	3.275	3.919	ns
t_{COUT}	1.557	1.571	2.698	3.005	3.595	ns
t_{PLLCIN}	0.037	0.051	0.474	0.521	0.613	ns
$t_{PLLCOUT}$	-0.128	-0.114	0.232	0.251	0.289	ns

Tables 4–98 through 4–105 show the maximum DCD in absolution derivation for different I/O standards on Stratix II GX devices. Examples are also provided that show how to calculate DCD as a percentage.

Table 4–98. Maximum DCD for Non-DDIO Output on Row I/O Pins

Row I/O Output Standard	Maximum DCD (ps) for Non-DDIO Output		
	-3 Devices	-4 and -5 Devices	Unit
3.3-V LVTTTL	245	275	ps
3.3-V LVCMOS	125	155	ps
2.5 V	105	135	ps
1.8 V	180	180	ps
1.5-V LVCMOS	165	195	ps
SSTL-2 Class I	115	145	ps
SSTL-2 Class II	95	125	ps
SSTL-18 Class I	55	85	ps
1.8-V HSTL Class I	80	100	ps
1.5-V HSTL Class I	85	115	ps
LVDS	55	80	ps

Here is an example for calculating the DCD as a percentage for a non-DDIO output on a row I/O on a -3 device:

If the non-DDIO output I/O standard is SSTL-2 Class II, the maximum DCD is 95 ps (see Table 4–99). If the clock frequency is 267 MHz, the clock period T is:

T = 1/ f = 1 / 267 MHz = 3.745 ns = 3,745 ps

To calculate the DCD as a percentage:

(T/2 – DCD) / T = (3,745 ps/2 – 95 ps) / 3,745 ps = 47.5% (for low boundary)

(T/2 + DCD) / T = (3,745 ps/2 + 95 ps) / 3,745 ps = 52.5% (for high boundary)