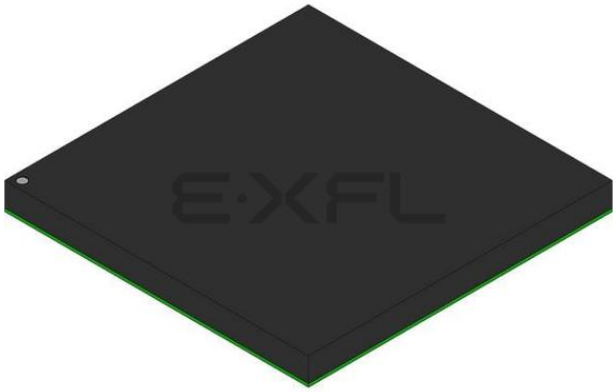
Altera - EP2SGX90EF1152C5 Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	4548
Number of Logic Elements/Cells	90960
Total RAM Bits	4520448
Number of I/O	558
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep2sgx90ef1152c5

Table shows the data path configurations for the Stratix II GX device in single-width and double-width modes.

1 Refer to the section B/B Encoder on page for a description of the single- and double-width modes.

Table 2 4. Data Path Configurations Note (1)

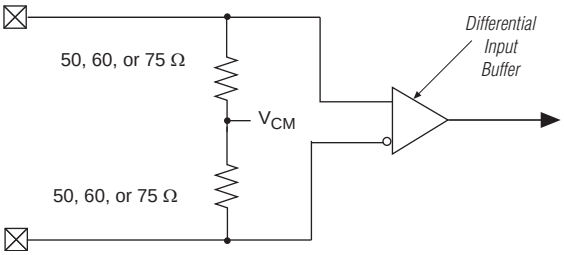
Parameter	Single-Width Mode		Double-Width Mode	
	Without Byte Serialization/ Deserialization	With Byte Serialization/ Deserialization	Without Byte Serialization/ Deserialization	With Byte Serialization/ Deserialization
Fabric to PCS data path width (bits)	8 or 10	16 or 20	16 or 20	32 or 40
Data rate range (Gbps)	0.6 to 2.5	0.6 to 3.125	1 to 5.0	1 to 6.375
PCS to PMA data path width (bits)	8 or 10	8 or 10	16 or 20	16 or 20
Byte ordering (1)		v		v
Data symbol A (MSB)				v
Data symbol B		v		v
Data symbol C			v	v
Data symbol D (LSB)	v	v	v	v

Note to Table 2 4:
() Designs can use byte ordering when byte serialiation and deserialiation are used.

8B/10B Encoder

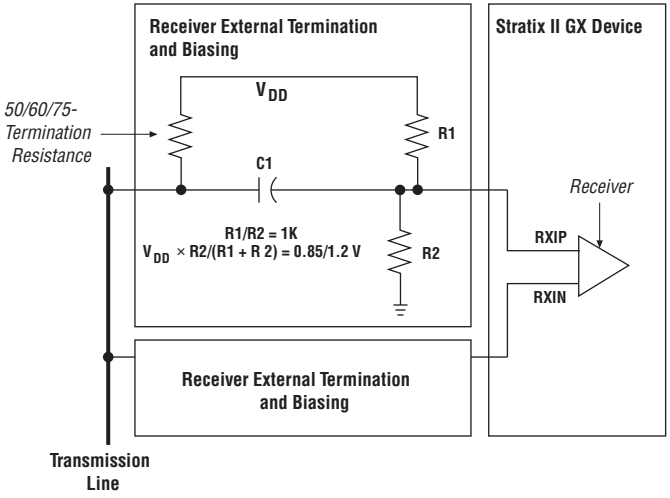
There are two different modes of operation for B/B encoding. Single-width (-bit) mode supports natural data rates from Mbps to . Gbps. Double-width (-bit cascaded) mode supports data rates above . Gbps. The encoded data has a maximum run length of five. The B/B encoder can be bypassed. igure diagrams the -bit encoding process.

Figure 2 13. Programmable Receiver Termination



If a design uses external termination the receiver must be externally terminated and biased to . V or . V. igure shows an example of an external terminaton and biasing circuit.

Figure 2 14. External Terminaion and Biasing Circuit



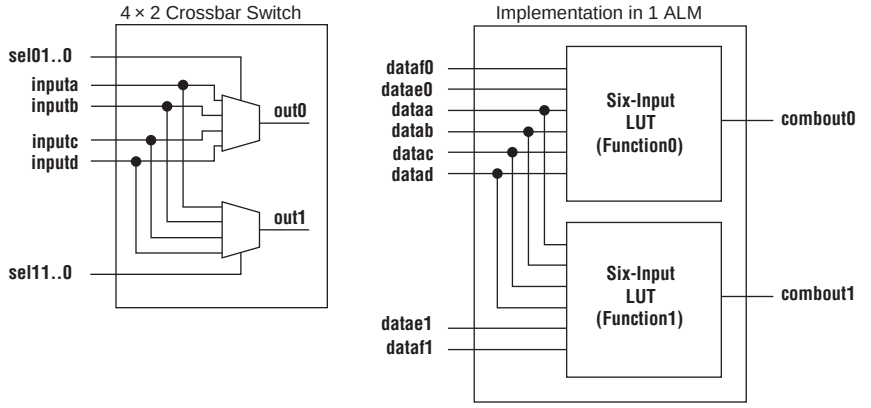
Programmable Equalizer

The Stratix II GX receivers provide a programmable receive eualiation feature to compensate the effects of channel attenuation for high-speed signaling. PCB traces carrying these high-speed signals have low-pass filter characteristics. The impedance mismatch boundaries can also cause signal degradation. The eualiation in the receiver diminishes the lossy attenuation effects of the PCB at high freuencies.

To pack two five-input functions into one ALM the functions must have at least two common inputs. The common inputs are and . The combination of a four-input function with a five-input function reuires one common input (either or).

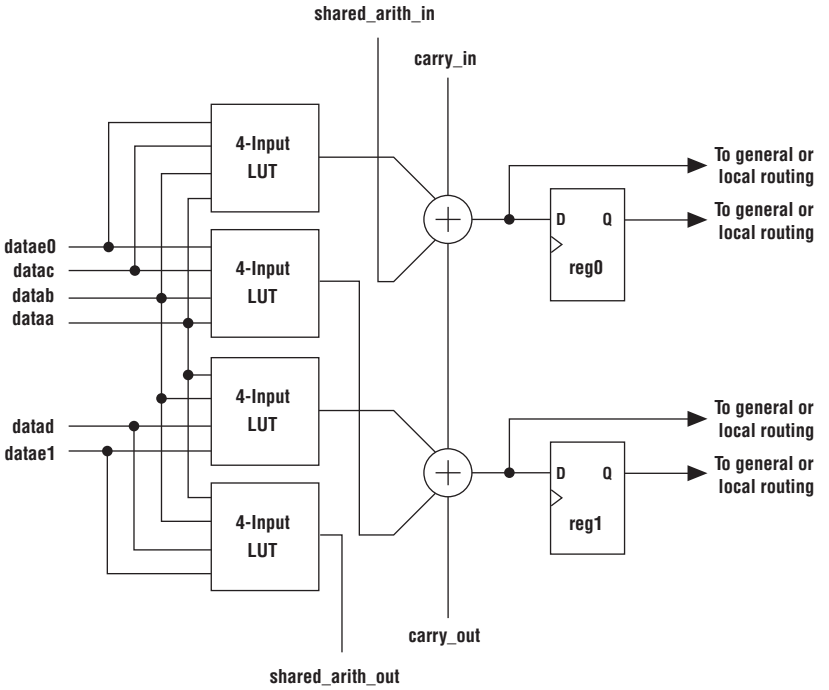
To implement two six-input functions in one ALM four inputs must be shared and the combinational functions must be the same. or example a crossbar switch (two -to- multiplexers with common inputs and uniue select lines) can be implemented in one ALM as shown in igure . The shared inputs are and while the uniue select lines are and for and and for This crossbar switch consumes four LUTs in a four-input LUT-based architecture.

Figure 2 38. 4 ×2 Crossbar Switch Example



In a sparsely used device functions that could be placed into one ALM can be implemented in separate ALMs. The uartus II Compiler spreads a design out to achieve the best possible performance. As a device begins to fill up the uartus II software au tomatically utilies the full potential of the Stratix II GX ALM. The uartu s II Compiler automatically searches for functions of common inputs or completely independent functions to be placed into one ALM and to make effi cient use of the device resources. In addition you can manually control resource usage by setting location assignments. Any six-input function can be implemented utiliing inputs and either and or and . If and are utilied the output is driven to and/or is bypassed and the data drives out to the interconnect using the top set of output drivers (see igure). If and are utilied the output drives to and/or bypasses and drives to the interconnect

Figure 2 43. ALM in Shared Arithmetic Mode



Note to Figure 2 43:
() Inputs and are available for register packing in shared arithmetic mode.

Adder trees are used in many different applications. or example the summation of the partial products in a logic-based multiplier can be implemented in a tree structure. Another example is a correlator function that can use a large adder tree to sum filtered data samples in a given time frame to recover or to de-spread data which was transmitted utiliing spread spectrum technology. An example of a three-bit add operation utiliing the shared arithmetic mode is shown in igure . The partial sum ( ) and the partial carry ( ) is obtained using the LUTs while the result ( ) is computed using the dedicated adders.

C column interconnects span a length of LABs and provide the fastest resource for long columnconnections between LABs TriMatrix memory blocks DSP blocks and IOEs. C interconnects can cross M-RAM blocks and also drive to row and column interconnects at every fourth LAB. C interconnects drive LAB local interconnects via C and R interconnects and do not drive LAB local interconnects directly. All embedded blocks communicate with the logic array similar to LAB-to-LAB interfaces. Each block (that is TriMatrix memory and DSP blocks) connects to row and column interconnects and has local interconnect regions driven by row and column interconnects. These blocks also have direct link interconnects for fast connections to and from a neighboring LAB. All blocks are fed by the row LAB clocks

.

Table shows the Stratix II GX devices routing scheme.

Table 2 18. Stratix II GX Device Routing Scheme (Part 1 of 2)

Source	Destination															
	Shared Arithmetic Chain	Carry Chain	Register Chain	Local Interconnect	Direct Link Interconnect	R4 Interconnect	R24 Interconnect	C4 Interconnect	C16 Interconnect	ALM	M512 RAM Block	M4K RAM Block	M-RAM Block	DSP Blocks	Column IOE	Row IOE
Shared arithmetic chain										v						
Carry chain										v						
Register chain										v						
Local interconnect										v	v	v	v	v	v	v
Direct link interconnect				v												
R4 interconnect				v		v	v	v	v							
R24 interconnect						v	v	v	v							
C4 interconnect				v		v		v								
C16 interconnect						v	v	v	v							
ALM	v	v	v	v	v	v										
M512 RAM block				v	v	v		v								
M4K RAM block				v	v	v		v								
M-RAM block					v	v	v	v								
DSP blocks					v	v		v								

Table shows the input and output data signal connections along with the address and control signal input connections to the row unit interfaces (L to L and R to R).

Table 2 20. M-RAM Row Interface Unit Signals

Unit Interface Block	Input Signals	Output Signals
L0		
L1		
L2		
L3		
L4		
L5		
R0		
R1		
R2		
R3		
R4		
R5		

f Refer to the TriMatrix Embedded Memory Blocks in Stratix II & Stratix II GX Devices chapter in volume of the Stratix II GX Device Handbook for more information on TriMatrix memory.

PLLs and Clock Networks

Stratix II GX devices provide a hierarchical clock structure and multiple phase-locked loops (PLLs) with advanced features. The large number of clocking resources in combination with the clock synthesis precision provided by enhanced and fast PLLs provides a complete clock management solution.

Global and Hierarchical Clocking

Stratix II GX devices provide dedicated global clock networks and regional clock networks (eight per device quadrant). These clocks are organized into a hierarchical clock structure that allows for up to clocks per device region with low skew and delay. This hierarchical clocking scheme provides up to unique clock domains in Stratix II GX devices.

There are dedicated clock pins to drive either the global or regional clock networks. Four clock pins drive each side of the device as shown in Figures and . Internal logic and enhanced and fast PLL outputs can also drive the global and regional clock networks. Each global and regional clock has a clock control block which controls the selection of the clock source and dynamically enables or disables the clock to reduce power consumption. Table shows global and regional clock features.

Table 2 24. Global and Regional Clock Features

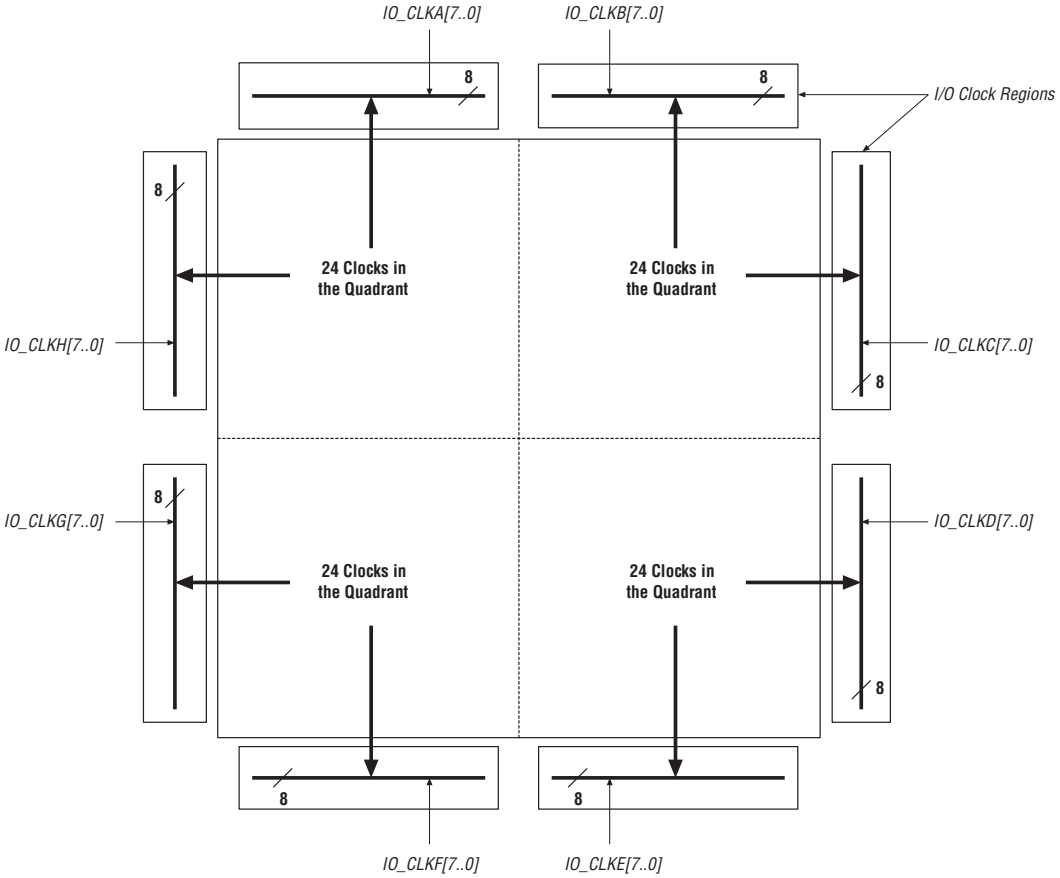
Feature	Global Clocks	Regional Clocks
Number per device	16	32
Number available per quadrant	16	8
Sources	Clock pins, PLL outputs, core routings, inter-transceiver clocks	Clock pins, PLL outputs, core routings, inter-transceiver clocks
Dynamic clock source selection	v	
Dynamic enable/disable	v	v

Global Clock Network

These clocks drive throughout the entire device feeding all device quadrants. The global clock networks can be used as clock sources for all resources in the device IOEs ALMs DSP blocks and all memory blocks. These resources can also be used for control signals such as clock enables and synchronous or asynchronous clears fed from the external pin. The global clock networks can also be driven by internal logic for internally

IOE clocks have row and column block regions that are clocked by I/O clock signals chosen from the quadrant clock resources. Figures and show the quadrant relationship to the I/O clock regions.

Figure 2 65. EP2SGX30 Device I/O Clock Groups



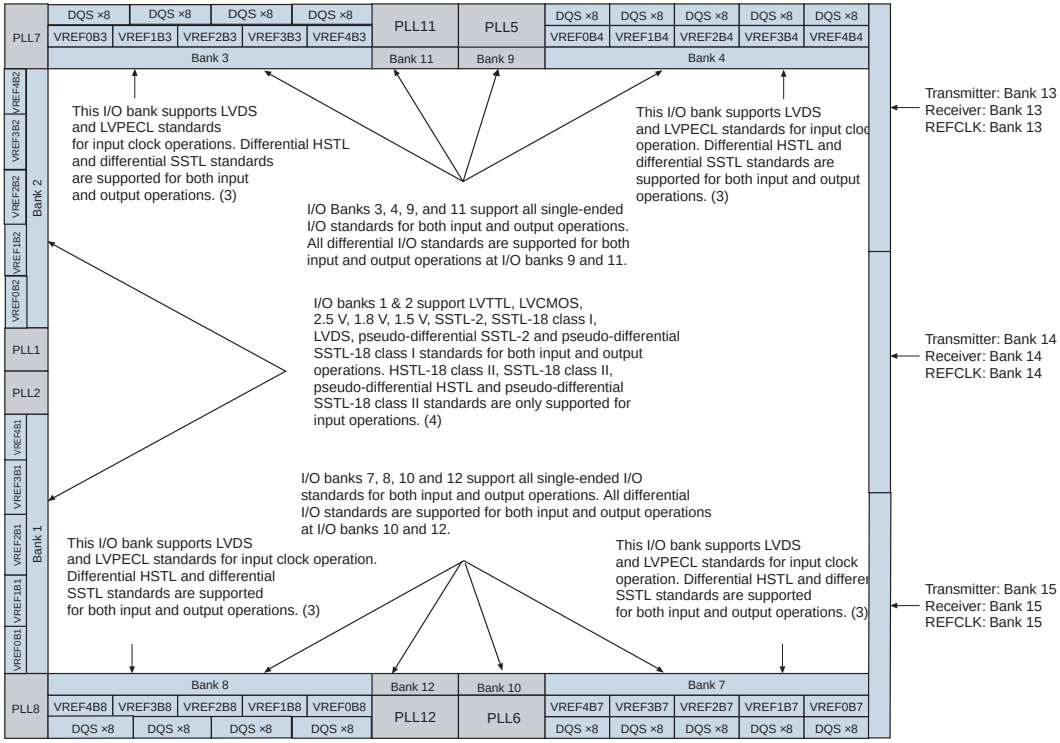
These dedicated circuits combinedwith enhanced PLL clocking and phase-shift ability provide a completehardware solution for interfacing to high-speed memory.

f or more information on external memory interfaces refer to the External Memory Interfaces in Stratix II &Stratix II GX Devices chapter in volume of the Stratix II GX Device Handbook

Programmable Drive Strength

The output buffer for each Stratix II GX device I/O pin has a programmable drive strength control for certain I/O standards. The LVTTL LVCMOS SSTL and HSTL standards have several levels of drive strength that you can control. The default setting used in the uartus II software is the maximum current strength setting that is used to achieve maximum I/O performance. or all I/ O standards the minimum setting is the lowest drive strength that guarantees the I_{OH}/I_{OL} of the standard. Using minimum settings provides signal slew rate control to reduce system noise and signal overshoot.

Figure 2 87. StratixII GX I/O Banks Notes (1), (2)



Notes to Figure 2 87:

() igure is a top view of the silicon die that corresponds to a reverse view for flip-chip packages. It is a graphical representation only.

() Depending on the sie of the device differen t device members have different numbers of V_{REF} groups. Refer to the pin list and the uartus II so ftware for exact locations.

() Banks through are enhanced PLL external clock output banks.

() Horiontal I/O banks feature SERDES and DPA circuitr y for high-speed differenti l I/O standards. See the High-Speed Differential I/O Interfaces with DPA in Stratix II & Stratix II GX Devices chapter in volume of the Stratix II Device Handbook for more information on differential I/O standards.

Each I/O bank has its own pins. A single device can support .- .- .- and .-V interfaces each bank can support a different V_{CCIO} level independently. Each bank also has dedicated pins to support the voltage-referenced standards (such as SSTL-).

Each I/O bank can support multiple standards with the same V_{CCIO} for input and output pins. Each bank can support one V_{REF} voltage level. or example when V_{CCIO} is . V a bank can support LVTTL LVCMOS and .-V PCI for inputs and outputs.

Table 2 42. Document Revision History (Part 5 of 6)

Date and Document Version	Changes Made	Summary of Changes
Previous Chapter 02 changes: **June 2006, v1.2**	**Updated notes 1 and 2 in Figure 2–1.** **Updated Byte Serializer section.** **Updated Tables 2–4, 2–7, and 2–16.** **Updated Programmable Output Driver section.** **Updated Figure 2–12.** **Updated Programmable Pre-Emphasis section.** **Added Table 2–11.** **Added Dynamic Reconfiguration section.** **Added Calibration Block section.** **Updated Programmable Equalizer section, including addition of Figure 2–18.**	**Updated input frequency range in Table 2–4.**
Previous Chapter 02 changes: **April 2006, v1.1**	**Updated Figure 2–3.** **Updated Figure 2–7.** **Updated Table 2–4.** **Updated Transmit Buffer section.**	**Updated input frequency range in Table 2–4.**
Previous Chapter 02 changes: **October 2005 v1.0**	**Added chapter to the** Stratix II GX Device Handbook**.**	
Previous Chapter 03 changes: **August 2006, v1.4**	**Updated Table 3–18 with note.**	
Previous Chapter 03 changes: **June 2006, v1.3**	**Updated note 2 in Figure 3–41.** **Updated column title in Table 3–21.**	
Previous Chapter 03 changes: **April 2006, v1.2**	**Updated note 1 in Table 3–9.** **Updated note 1 in Figure 3–40.** **Updated note 2 in Figure 3–41.** **Updated Table 3–16.** **Updated Figure 3–56.** **Updated Tables 3–19 through 3–22.** **Updated Tables 3–25 and 3–26.** **Updated Fast PLL & Channel Layout section.**	**Added 1,152-pin FineLine BGA package information for EP2SGX60 device in Table 3–16.**

The pin is a dedicated input that chooses whether the internal pull-up resistors on the user I/O pins and dual-purpose configuration I/O pins ( ) are on or off before and during configuration. A logic high (. . . . V) turns off the weak internal pull -up resistors while a logic low turns them on.

Stratix II GX devices also offer a new power supply V_{CCPD} which must be connected to . V in order to power the .-V/.-V buffer available on the configuration input pins and TAG pins. V_{CCPD} applies to all the TAG input pins (and) and the following configuration pins (when used as an input) and . The pin allows the V_{CCIO} setting (of the banks where the configuration inputs reside) to be independent of the voltage reuired by the configuration inputs. Therefore when selecting the V_{CCIO} voltage you do not have to take the V_{IL} and V_{IH} levels driven to the configuration inputs into consideration. The configuration input pins (when used as an input) and have a dual buffer design a .-V/.-V input buffer and a .-V/.-V input buffer. The V_{CCSEL} input pin selects which input buffer is used. The .-V/.-V input buffer is powered by V_{CCPD} while the .-V/.-V input buffer is powered by V_{CCIO}.

V_{CCSEL} is sampled during power-up. Therefore the V_{CCSEL} setting cannot change on-the-fly or during a reconfiguration. The V_{CCSEL} input buffer is powered by V_{CCINT} and must be hardwired to V_{CCPD} or ground. A logic high V_{CCSEL} connection selects the .-V/. -V input buffer a logic low selects the .-V/.-V input buffer. V_{CCSEL} should be set to comply with the logic levels driven out of the configuration device or the MAX II microprocessor.

If the design must support configuration input voltages of . V/. V set V_{CCSEL} to a logic low. ou can set the V_{CCIO} voltage of the I/O bank that contains the configuration inputs to any supported voltage. If the design must support configuration input voltages of . V/. V set V_{CCSEL} to a logic high and the V_{CCIO} of the bank that contains the configuration inputs to . V/. V.

f or more information on multi-volt support including information on using and in multi-volt systems refer to the Stratix II GX Architecture chapter in volume of the Stratix II GX Device Handbook

Table shows the Stratix II GX transceiver block AC specifications.

Table 4 19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 1 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SONET/SDH Transmit Jitter Generation	(7)										
Peak-to-peak jitter at 622.08 Mbps	**= 77.76 MHz Pattern = PRBS23 V_{OD} = 800 mV No Pre-emphasis**	**-**	**-**	**0.1**	**-**	**-**	**0.1**	**-**	**-**	**0.1**	**UI**
RMS jitter at 622.08 Mbps	**= 77.76 MHz Pattern = PRBS23 V_{OD} = 800 mV No Pre-emphasis**	**-**	**-**	**0.01**	**-**	**-**	**0.01**	**-**	**-**	**0.01**	**UI**
Peak-to-peak jitter at 2488.32 Mbps	**= 155.52 MHz Pattern = PRBS23 V_{OD} = 800 mV No Pre-emphasis**	**-**	**-**	**0.1**	**-**	**-**	**0.1**	**-**	**-**	**0.1**	**UI**
RMS jitter at 2488.32 Mbps	**= 155.52 MHz Pattern = PRBS23 V_{OD} = 800 mV No Pre-emphasis**	**-**	**-**	**0.01**	**-**	**-**	**0.01**	**-**	**-**	**0.01**	**UI**

Table 4 19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 6 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Serial RapidIO Receiver Jitter Tolerance	(11)										
Deterministic Jitter Tolerance (peak-to-peak)	**Data Rate = 1.25, 2.5, 3.125 Gbps = 125 MHz Pattern = CJPAT Equalizer Setting = 0 for 1.25 Gbps Equalizer Setting = 6 for 2.5 Gbps Equalizer Setting = 6 for 3.125 Gbps**		**0.37**			**0.37**			**0.37**		**UI**
Combined Deterministic and Random Jitter Tolerance (peak-to-peak)	**Data Rate = 1.25, 2.5, 3.125 Gbps = 125 MHz Pattern = CJPAT Equalizer Setting = 0 for 1.25 Gbps Equalizer Setting = 6 for 2.5 Gbps Equalizer Setting = 6 for 3.125 Gbps**		**0.55**			**0.55**			**0.55**		**UI**

Table 4 19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 13 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
CPRI Receiver Jitter Tolerance (15)											
Deterministic Jitter Tolerance (peak-to-peak)	**Data Rate = 614.4 Mbps, 1.2288 Gbps, 2.4576 Gbps = 61.44 MHz for 614.4 Mbps = 122.88 MHz for 1.2288 Gbps and 2.4576 Gbps Pattern = CJPAT Equalizer Setting = 6 DC Gain = 0 dB**		**0.4**			**0.4**			**N/A**		**UI**
Combined Deterministic and Random Jitter Tolerance (peak-to-peak)	**Data Rate = 614.4 Mbps, 1.2288 Gbps, 2.4576 Gbps = 61.44 MHz for 614.4 Mbps = 122.88 MHz for 1.2288 Gbps and 2.4576 Gbps Pattern = CJPAT Equalizer Setting = 6 DC Gain = 0 dB**		**0.66**			**0.66**			**N/A**		**UI**

Table 4 21. PCS Latency (Part 2 of 2) Note (1)

Functional Mode	Configuration	Transmitter PCS Latency					
		TX PIPE	TX Phase Comp FIFO	Byte Serializer	TX State Machine	8B/10B Encoder	Sum(2)
Serial RapidIO	**1.25 Gbps, 2.5 Gbps, 3.125 Gbps**	**-**	**2-3**	**1**	**-**	**0.5**	**4-5**
SDI	**HD 10-bit channel width**	**-**	**2-3**	**1**	**-**	**1**	**4-5**
	HD, 3G 20-bit channel width	**-**	**2-3**	**1**	**-**	**0.5**	**4-5**
BASIC Single Width	**8-bit/10-bit channel width**	**-**	**2-3**	**1**	**-**	**1**	**4-5**
	16-bit/20-bit channel width	**-**	**2-3**	**1**	**-**	**0.5**	**4-5**
BASIC Double Width	**16-bit/20-bit channel width**	**-**	**2-3**	**1**	**-**	**1**	**4-5**
	32-bit/40-bit channel width	**-**	**2-3**	**1**	**-**	**0.5**	**4-5**
	Parallel Loopback/ BIST	**-**	**2-3**	**1**	**-**	**1**	**4-5**

Notes to Table 4 21:

() **The latency numbers are with respect to the PLD-transceiver interface clock cycles.**

() **The total latency number is rounded off in the Sum column.**

() **or CPRI Mbps and . Gbps data rates the uartus II software customies the PLD-transceiver interface clocking to achieve ero clock cycle uncertainty in the transmitter phase compensation IO latency. or more details refer to the** CPRI Mode **section in the** Stratix II GX Transceiver Architecture Overview **chapter in volume of the** Stratix II GX Device Handbook

Table 4 27. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO} (1)	Output supply voltage		1.71	1.89	V
V_{IH}	High-level input voltage		0.65 × V_{CCIO}	2.25	V
V_{IL}	Low-level input voltage		–0.3	0.35 × V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OH} = –2 mA (2)	V_{CCIO} – 0.45		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA (2)		0.45	V

Notes to Table 4 27:

() The Stratix II GX device V_{CCIO} voltage level support of . to is narrower than defined in the Normal Range of the EIA/EDEC standard.

() This specification is supported across all the programmable drive settings available for this I/O standard as shown in Stratix II GX Architecture chapter in volume of the Stratix II GX Device Handbook

Table 4 28. 1.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO} (1)	Output supply voltage		1.425	1.575	V
V_{IH}	High-level input voltage		0.65 V_{CCIO}	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.35 V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OH} = –2 mA (2)	0.75 V_{CCIO}		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA (2)		0.25 V_{CCIO}	V

Notes to Table 4 28:

() The Stratix II GX device V_{CCIO} voltage level support of . to is narrower than defined in the Normal Range of the EIA/EDEC standard.

() This specification is supported across all the programmable drive settings available for this I/O standard as shown in Stratix II GX Architecture chapter in volume of the Stratix II GX Device Handbook

Figure 4 10. Measurement Setup for t_{zx}

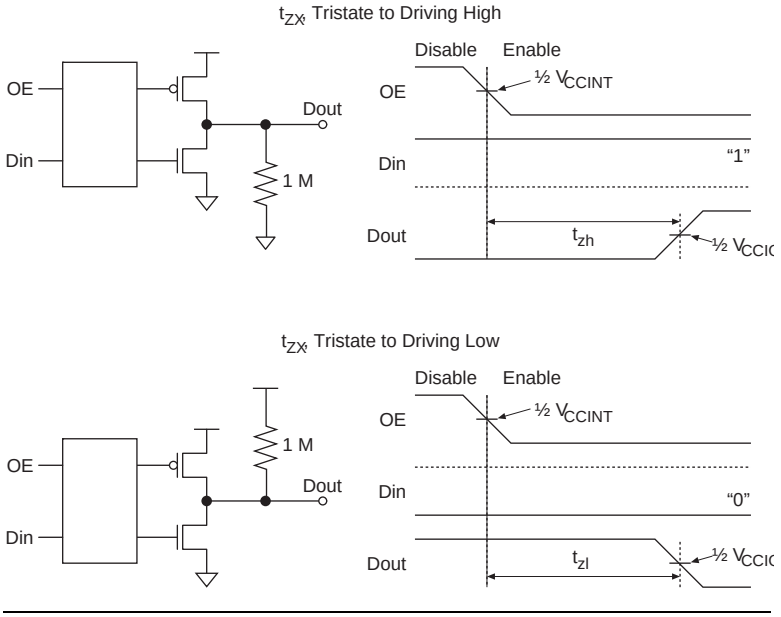


Table specifies the input timing measurement setup.

Table 4 54. Timing Measurement Methodology for Input Pins (Part 1 of 2) Notes (1), (2), (3), (4)

I/O Standard	Measurement Conditions			Measurement Point
	V_{CCIO}(V)	V_{REF}(V)	Edge Rate (ns)	VMEAS (V)
LVTTL (5)	3.135		3.135	1.5675
LVCMOS (5)	3.135		3.135	1.5675
2.5 V (5)	2.375		2.375	1.1875
1.8 V (5)	1.710		1.710	0.855
1.5 V (5)	1.425		1.425	0.7125
PCI (6)	2.970		2.970	1.485
PCI-X (6)	2.970		2.970	1.485
SSTL-2 Class I	2.325	1.163	2.325	1.1625
SSTL-2 Class II	2.325	1.163	2.325	1.1625
SSTL-18 Class I	1.660	0.830	1.660	0.83
SSTL-18 Class II	1.660	0.830	1.660	0.83
1.8-V HSTL Class I	1.660	0.830	1.660	0.83

Table 4 86. Stratix II GX I/O Output Delay for Column Pins (Part 6 of 7)

I/O Standard	Drive Strength	Parameter	Fast Corner Industrial/ Commercial	-3 Speed Grade (3)	-3 Speed Grade (4)	-4 Speed Grade	-5 Speed Grade	Unit
Differential SSTL-18 Class II (2)	**8 mA**	t_{OP}	**925**	**1597**	**1675**	**1782**	**1904**	ps
		t_{DIP}	**947**	**1663**	**1745**	**1856**	**1994**	ps
	16 mA	t_{OP}	**937**	**1578**	**1655**	**1761**	**1882**	ps
		t_{DIP}	**959**	**1644**	**1725**	**1835**	**1972**	ps
	18 mA	t_{OP}	**933**	**1585**	**1663**	**1768**	**1890**	ps
		t_{DIP}	**955**	**1651**	**1733**	**1842**	**1980**	ps
	20 mA	t_{OP}	**933**	**1583**	**1661**	**1766**	**1888**	ps
		t_{DIP}	**955**	**1649**	**1731**	**1840**	**1978**	ps
1.8-V differential HSTL Class I (2)	**4 mA**	t_{OP}	**956**	**1608**	**1687**	**1794**	**1943**	ps
		t_{DIP}	**978**	**1674**	**1757**	**1868**	**2033**	ps
	6 mA	t_{OP}	**962**	**1595**	**1673**	**1779**	**1928**	ps
		t_{DIP}	**984**	**1661**	**1743**	**1853**	**2018**	ps
	8 mA	t_{OP}	**940**	**1586**	**1664**	**1769**	**1917**	ps
		t_{DIP}	**962**	**1652**	**1734**	**1843**	**2007**	ps
	10 mA	t_{OP}	**944**	**1591**	**1669**	**1775**	**1923**	ps
		t_{DIP}	**966**	**1657**	**1739**	**1849**	**2013**	ps
	12 mA	t_{OP}	**936**	**1585**	**1663**	**1768**	**1916**	ps
		t_{DIP}	**958**	**1651**	**1733**	**1842**	**2006**	ps
1.8-V differential HSTL Class II (2)	**16 mA**	t_{OP}	**919**	**1385**	**1453**	**1545**	**1680**	ps
		t_{DIP}	**941**	**1451**	**1523**	**1619**	**1770**	ps
	18 mA	t_{OP}	**921**	**1394**	**1462**	**1555**	**1691**	ps
		t_{DIP}	**943**	**1460**	**1532**	**1629**	**1781**	ps
	20 mA	t_{OP}	**921**	**1402**	**1471**	**1564**	**1700**	ps
		t_{DIP}	**943**	**1468**	**1541**	**1638**	**1790**	ps