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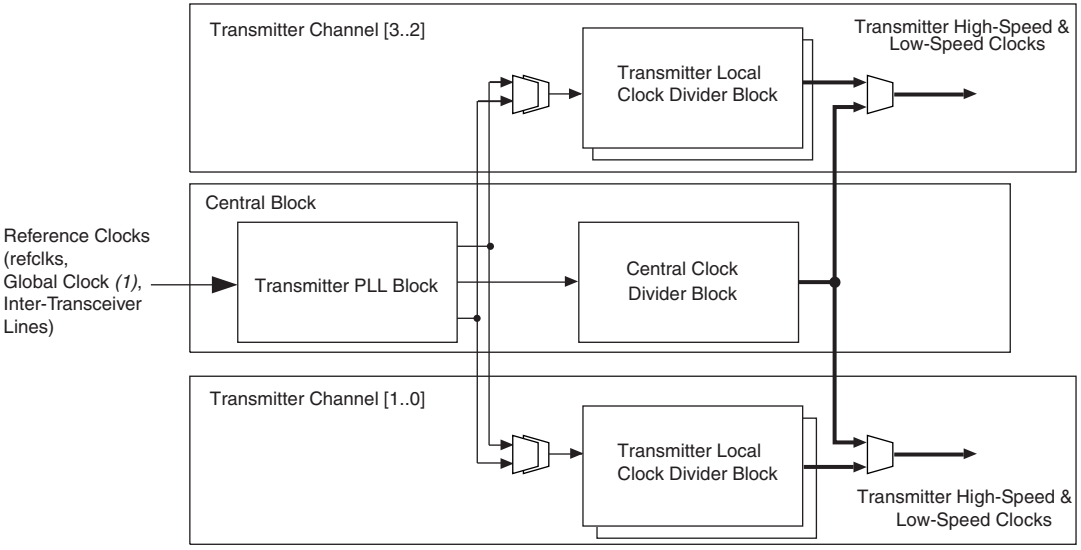
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	4548
Number of Logic Elements/Cells	90960
Total RAM Bits	4520448
Number of I/O	650
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1508-BBGA, FCBGA
Supplier Device Package	1508-FBGA, FC (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2sgx90ff1508c3n

Figure 2–3. Clock Distribution for the Transmitters Note (1)



Note to Figure 2–3:
(1) The global clock line must be driven by an input pin.

The transmitter PLLs in each transceiver block clock the PMA and PCS circuitry in the transmit path. The Quartus II software automatically powers down the transmitter PLLs that are not used in the design. Figure 2–4 is a block diagram of the transmitter PLL.

The transmitter phase/frequency detector references the clock from one of the following sources:

- Reference clocks
- Reference clock from the adjacent transceiver block
- Inter-transceiver block clock lines
- Global clock line driven by input pin

Two reference clocks, `REFCLK0` and `REFCLK1`, are available per transceiver block. The inter-transceiver block bus allows multiple transceivers to use the same reference clocks. Each transceiver block has one outgoing reference clock which connects to one inter-transceiver block line. The incoming reference clock can be selected from five inter-transceiver block lines `IQ[4..0]` or from the global clock line that is driven by an input pin.

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Table 2–15. Available Clocking Connections for Transceivers in 2SGX130G

Region	Clock Resource		Transceiver				
	Global Clock	Regional Clock	Bank 13 8 Clock I/O	Bank 14 8 Clock I/O	Bank 15 8 clock I/O	Bank 16 8 Clock I/O	Bank 17 8 Clock I/O
Region0 8 LRIO clock	✓	RCLK 20-27	✓				
Region1 8 LRIO clock	✓	RCLK 20-27		✓			
Region2 8 LRIO clock	✓	RCLK 12-19			✓	✓	
Region3 8 LRIO clock	✓	RCLK 12-19				✓	✓

Other Transceiver Features

Other important features of the Stratix II GX transceivers are the power down and reset capabilities, external voltage reference and bias circuitry, and hot swapping.

Calibration Block

The Stratix II GX device uses the calibration block to calibrate the on-chip termination for the PLLs and their associated output buffers and the terminating resistors on the transceivers. The calibration block counters the effects of process, voltage, and temperature (PVT). The calibration block references a derived voltage across an external reference resistor to calibrate the on-chip termination resistors on the Stratix II GX device. The calibration block can be powered down. However, powering down the calibration block during operations may yield transmit and receive data errors.

Dynamic Reconfiguration

This feature allows you to dynamically reconfigure the PMA portion and the channel parameters, such as data rate and functional mode, of the Stratix II GX transceiver. The PMA reconfiguration allows you to quickly optimize the settings for the transceiver's PMA to achieve the intended bit error rate (BER).

Table 2–16. Reset Signal Map to Stratix II GX Blocks

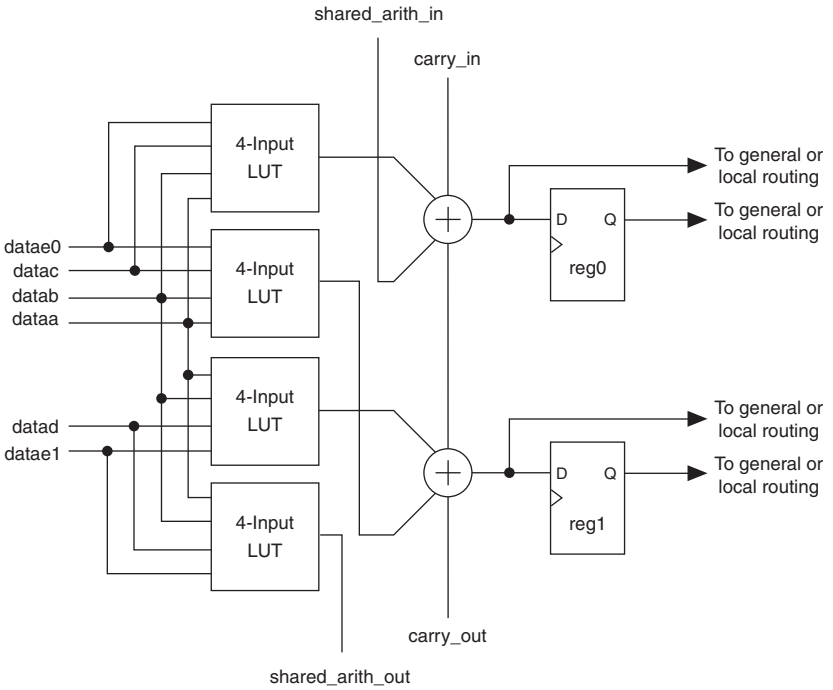
Reset Signal	Transmitter Phase Compensation FIFO Module/ Byte Serializer	Transmitter 8B/10B Encoder	Transmitter Serializer	Transmitter Analog Circuits	Transmitter PLL	Transmitter XAUI State Machine	BIST Generators	Receiver Deserializer	Receiver Word Aligner	Receiver Deskew FIFO Module	Receiver Rate Matcher	Receiver 8B/10B Decoder	Receiver Phase Comp FIFO Module/ Byte Deserializer	Receiver PLL / CRU	Receiver XAUI State Machine	BIST Verifiers	Receiver Analog Circuits
rx_digitalreset									✓	✓	✓	✓	✓		✓	✓	
rx_analogreset								✓						✓			✓
tx_digitalreset	✓	✓				✓	✓										
gxb_powerdown	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
gxb_enable	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Voltage Reference Capabilities

Stratix II GX transceivers provide voltage reference and bias circuitry. To set up internal bias for controlling the transmitter output driver voltage swings, as well as to provide voltage and current biasing for other analog circuitry, the device uses an internal bandgap voltage reference of 0.7 V. An external 2-KΩ resistor connected to ground generates a constant bias current (independent of power supply drift, process changes, or temperature variation). An on-chip resistor generates a tracking current that tracks on-chip resistor variation. These currents are mirrored and distributed to the analog circuitry in each channel.

For more information, refer to the *DC and Switching Characteristics* chapter in volume 1 of the *Stratix II GX Handbook*.

Figure 2–43. ALM in Shared Arithmetic Mode



Note to Figure 2–43:
(1) Inputs `dataf0` and `dataf1` are available for register packing in shared arithmetic mode.

Adder trees are used in many different applications. For example, the summation of the partial products in a logic-based multiplier can be implemented in a tree structure. Another example is a correlator function that can use a large adder tree to sum filtered data samples in a given time frame to recover or to de-spread data which was transmitted utilizing spread spectrum technology. An example of a three-bit add operation utilizing the shared arithmetic mode is shown in Figure 2–44. The partial sum (`S[2..0]`) and the partial carry (`C[2..0]`) is obtained using the LUTs, while the result (`R[2..0]`) is computed using the dedicated adders.

Table 2–18. Stratix II GX Device Routing Scheme (Part 2 of 2)

Source	Destination															
	Shared Arithmetic Chain	Carry Chain	Register Chain	Local Interconnect	Direct Link Interconnect	R4 Interconnect	R24 Interconnect	C4 Interconnect	C16 Interconnect	ALM	M512 RAM Block	M4K RAM Block	M-RAM Block	DSP Blocks	Column IOE	Row IOE
Column IOE					✓			✓	✓							
Row IOE					✓	✓	✓	✓								

TriMatrix Memory

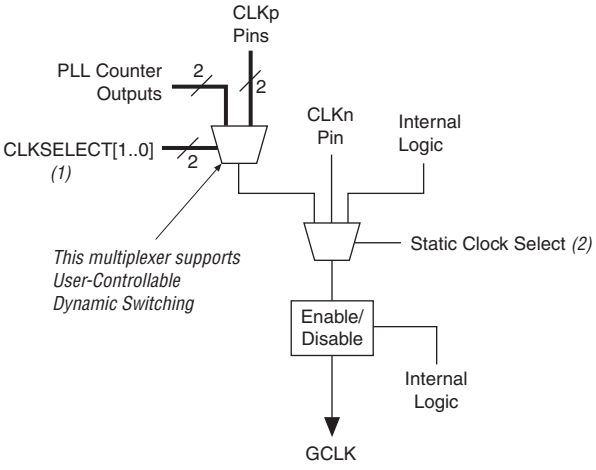
TriMatrix memory consists of three types of RAM blocks: M512, M4K, and M-RAM. Although these memory blocks are different, they can all implement various types of memory with or without parity, including true dual-port, simple dual-port, and single-port RAM, ROM, and FIFO buffers. Table 2–19 shows the size and features of the different RAM blocks.

Table 2–19. TriMatrix Memory Features (Part 1 of 2)

Memory Feature	M512 RAM Block (32 × 18 Bits)	M4K RAM Block (128 × 36 Bits)	M-RAM Block (4K × 144 Bits)
Maximum performance	500 MHz	550 MHz	420 MHz
True dual-port memory		✓	✓
Simple dual-port memory	✓	✓	✓
Single-port memory	✓	✓	✓
Shift register	✓	✓	
ROM	✓	✓	*(1)*
FIFO buffer	✓	✓	✓
Pack mode		✓	✓
Byte enable	✓	✓	✓
Address clock enable		✓	✓
Parity bits	✓	✓	✓
Mixed clock mode	✓	✓	✓
Memory initialization (**.mif**)	✓	✓	

Figures 2–67 through 2–69 show the clock control block for the global clock, regional clock, and PLL external clock output, respectively.

Figure 2–67. Global Clock Control Blocks

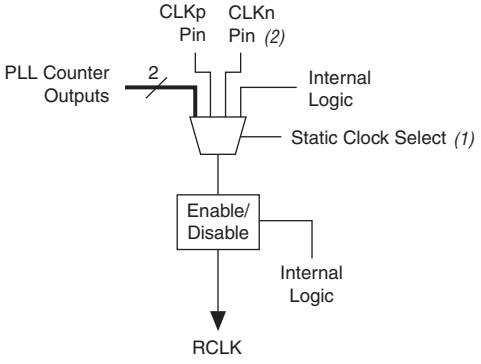


Notes to Figure 2–67:

(1) These clock select signals can be dynamically controlled through internal logic when the device is operating in user mode.

(2) These clock select signals can only be set through a configuration file (SRAM Object File [**.sof**] or Programmer Object File [**.pof**]) and cannot be dynamically controlled during user mode operation.

Figure 2–68. Regional Clock Control Blocks



Notes to Figure 2–68:

(1) These clock select signals can only be set through a configuration file (**.sof** or **.pof**) and cannot be dynamically controlled during user mode operation.

(2) Only the `CLKn` pins on the top and bottom of the device feed to regional clock select.

Table 2–29. Global and Regional Clock Connections from Bottom Clock Pins and Enhanced PLL Outputs (Part 2 of 2)

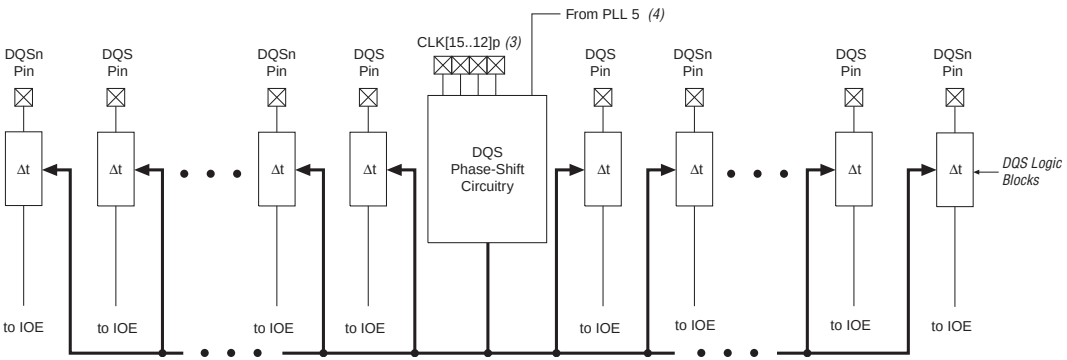
Bottom Side Global and Regional Clock Network Connectivity	DLLCLK	CLK4	CLK5	CLK6	CLK7	RCLK8	RCLK9	RCLK10	RCLK11	RCLK12	RCLK13	RCLK14	RCLK15
GCLKDRV2				✓									
GCLKDRV3					✓								
RCLKDRV0						✓				✓			
RCLKDRV1							✓				✓		
RCLKDRV2								✓				✓	
RCLKDRV3									✓				✓
RCLKDRV4						✓				✓			
RCLKDRV5							✓				✓		
RCLKDRV6								✓				✓	
RCLKDRV7									✓				✓
Enhanced PLL 6 outputs													
c0	✓	✓	✓			✓				✓			
c1	✓	✓	✓				✓				✓		
c2	✓			✓	✓			✓				✓	
c3	✓			✓	✓				✓				✓
c4	✓					✓		✓		✓		✓	
c5	✓						✓		✓		✓		✓
Enhanced PLL 12 outputs													
c0		✓	✓			✓				✓			
c1		✓	✓				✓				✓		
c2				✓	✓			✓				✓	
c3				✓	✓				✓				✓
c4						✓		✓		✓		✓	
c5							✓		✓		✓		✓

A compensated delay element on each DQS pin automatically aligns input DQS synchronization signals with the data window of their corresponding DQ data signals. The DQS signals drive a local DQS bus in the top and bottom I/O banks. This DQS bus is an additional resource to the I/O clocks and is used to clock DQ input registers with the DQS signal.

The Stratix II GX device has two phase-shifting reference circuits, one on the top and one on the bottom of the device. The circuit on the top controls the compensated delay elements for all DQS pins on the top. The circuit on the bottom controls the compensated delay elements for all DQS pins on the bottom.

Each phase-shifting reference circuit is driven by a system reference clock, which must have the same frequency as the DQS signal. Clock pins `CLK[15..12]p` feed the phase circuitry on the top of the device and clock pins `CLK[7..4]p` feed the phase circuitry on the bottom of the device. In addition, PLL clock outputs can also feed the phase-shifting reference circuits. Figure 2–86 shows the phase-shift reference circuit control of each DQS delay shift on the top of the device. This same circuit is duplicated on the bottom of the device.

Figure 2–86. DQS Phase-Shift Circuitry *Notes (1), (2)*



Notes to Figure 2–86:

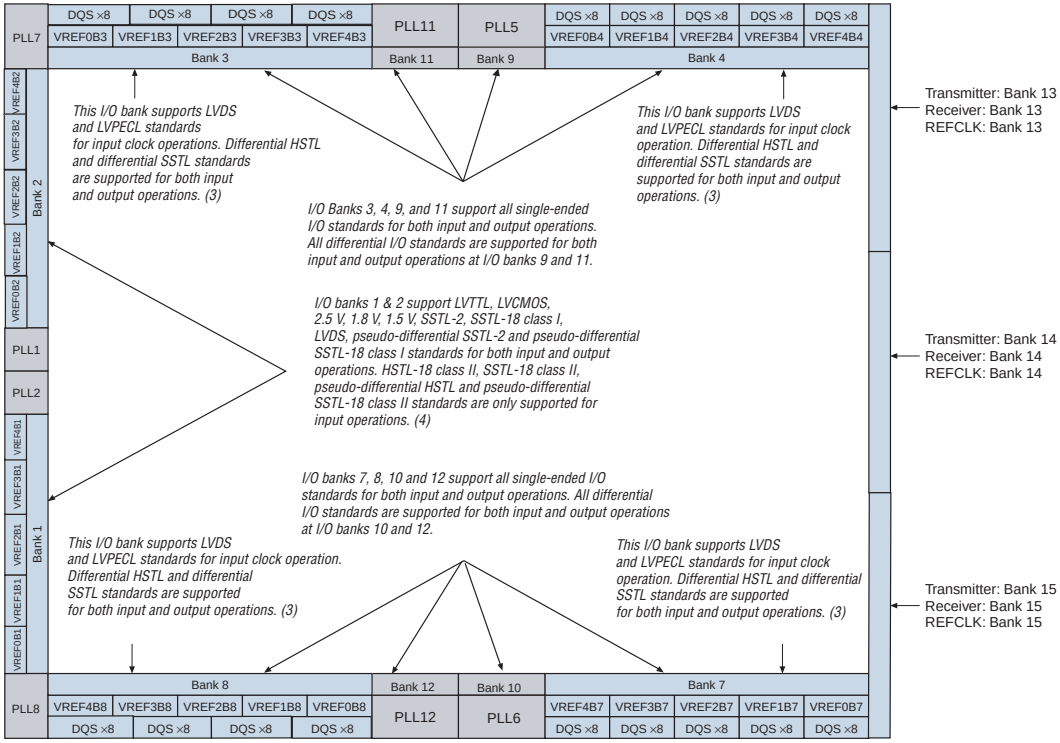
(1) There are up to 18 pairs of DQS and DQSn pins available on the top or the bottom of the Stratix II GX device. There are up to 10 pairs on the right side and 8 pairs on the left side of the DQS phase-shift circuitry.

(2) The "t" module represents the DQS logic block.

(3) Clock pins `CLK[15..12]p` feed the phase-shift circuitry on the top of the device and clock pins `CLK[7..4]p` feed the phase circuitry on the bottom of the device. You can also use a PLL clock output as a reference clock to the phaseshift circuitry.

(4) You can only use PLL 5 to feed the DQS phase-shift circuitry on the top of the device and PLL 6 to feed the DQS phase-shift circuitry on the bottom of the device.

Figure 2–87. Stratix II GX I/O Banks *Notes (1), (2)*



Notes to Figure 2–87:

(1) Figure 2–87 is a top view of the silicon die that corresponds to a reverse view for flip-chip packages. It is a graphical representation only.

(2) Depending on the size of the device, different device members have different numbers of V_{REF} groups. Refer to the pin list and the Quartus II software for exact locations.

(3) Banks 9 through 12 are enhanced PLL external clock output banks.

(4) Horizontal I/O banks feature SERDES and DPA circuitry for high-speed differential I/O standards. See the *High-Speed Differential I/O Interfaces with DPA in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook 2* for more information on differential I/O standards.

Each I/O bank has its own VCCIO pins. A single device can support 1.5-, 1.8-, 2.5-, and 3.3-V interfaces; each bank can support a different V_{CCIO} level independently. Each bank also has dedicated VREF pins to support the voltage-referenced standards (such as SSTL-2).

Each I/O bank can support multiple standards with the same V_{CCIO} for input and output pins. Each bank can support one V_{REF} voltage level. For example, when V_{CCIO} is 3.3 V, a bank can support LVTTL, LVCMOS, and 3.3-V PCI for inputs and outputs.

considerable flexibility for frequency synthesis, allowing real-time variation of the PLL frequency and delay. The rest of the device is functional while reconfiguring the PLL.

See the *PLLs in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook* for more information on Stratix II GX PLLs.

Temperature Sensing Diode (TSD)

Stratix II GX devices include a diode-connected transistor for use as a temperature sensor in power management. This diode is used with an external digital thermometer device. These devices steer bias current through the Stratix II GX diode, measuring forward voltage and converting this reading to temperature in the form of an 8-bit signed number (7 bits plus 1 sign bit). The external device's output represents the junction temperature of the Stratix II GX device and can be used for intelligent power management.

The diode requires two pins (`tempdiodep` and `tempdioden`) on the Stratix II GX device to connect to the external temperature-sensing device, as shown in Figure 3–1. The temperature sensing diode is a passive element and therefore can be used before the Stratix II GX device is powered.

Figure 3–1. External Temperature-Sensing Diode

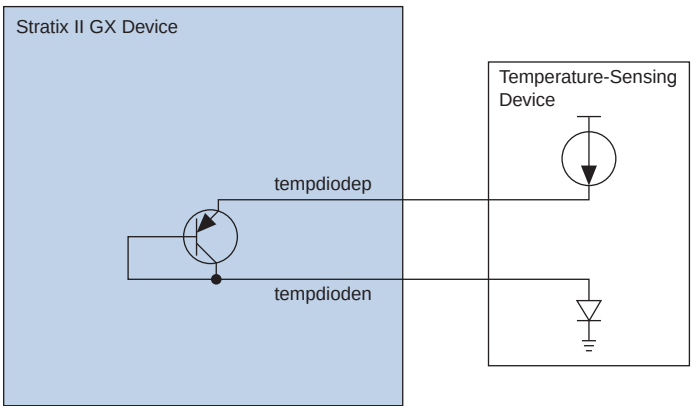


Table 4–15. Typical Pre-Emphasis (First Post-Tap), Note (1) (Part 2 of 2)

V_{CCH} TX = 1.5 V	First Post Tap Pre-Emphasis Level											
V_{OD} Setting (mV)	1	2	3	4	5	6	7	8	9	10	11	12
600		33%	53%	80%	115%	157%	195%	294%	386%			
900		19%	28%	38%	56%	70%	86%	113%	133%	168%	196%	242%
1200			17%	22%	31%	40%	52%	62%	75%	86%	96%	112%

Note to Table 4–15:
(1) Applicable to data rates from 600 Mbps to 6.375 Gbps. Specification is for measurement at the package ball.

Table 4–16. Typical Pre-Emphasis (First Post-Tap), Note (1)

V_{CCH} TX = 1.2 V	First Post Tap Pre-Emphasis Level											
V_{OD} Setting (mV)	1	2	3	4	5	6	7	8	9	10	11	12
	TX Term = 100 Ω											
320	24%	61%	114%									
480		31%	55%	86%	121%	170%	232%	333%				
640		20%	35%	54%	72%	95%	124%	157%	195%	233%	307%	373%
800			23%	36%	49%	64%	81%	97%	117%	140%	161%	195%
960			18%	25%	35%	44%	57%	69%	82%	94%	108%	127%

Note to Table 4–16:
(1) Applicable to data rates from 600 Mbps to 3.125 Gbps. Specification is for measurement at the package ball.

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 7 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Sinusoidal Jitter Tolerance (peak-to-peak)	Jitter Frequency = 22.1 KHz Data Rate = 1.25, 2.5, 3.125 Gbps REFCLK = 125 MHz Pattern = CJPAT Equalizer Setting = 0 for 1.25 Gbps Equalizer Setting = 6 for 2.5 Gbps Equalizer Setting = 6 for 3.125 Gbps		> 8.5			> 8.5			> 8.5		UI
	Jitter Frequency = 1.875 MHz Data Rate = 1.25, 2.5, 3.125 Gbps REFCLK = 125 MHz Pattern = CJPAT Equalizer Setting = 0 for 1.25 Gbps Equalizer Setting = 6 for 2.5 Gbps Equalizer Setting = 6 for 3.125 Gbps		> 0.1			> 0.1			> 0.1		UI
	Jitter Frequency = 20 MHz Data Rate = 1.25, 2.5, 3.125 Gbps REFCLK = 125 MHz Pattern = CJPAT Equalizer Setting = 0 for 1.25 Gbps Equalizer Setting = 6 for 2.5 Gbps Equalizer Setting = 6 for 3.125 Gbps		> 0.1			> 0.1			> 0.1		UI

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 8 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
GIGE Transmit Jitter Generation *(12)*											
Deterministic Jitter (peak-to-peak)	Data Rate = 1.25 Gbps REFCLK = 125 MHz Pattern = CRPAT V_{OD} = 1400 mV No Pre-emphasis	-	-	0.14	-	-	0.14	-	-	0.14	UI
Total Jitter (peak-to-peak)	Data Rate = 1.25 Gbps REFCLK = 125 MHz Pattern = CRPAT V_{OD} = 1400 mV No Pre-emphasis	-	-	0.279	-	-	0.279	-	-	0.279	UI
GIGE Receiver Jitter Tolerance *(12)*											
Deterministic Jitter Tolerance (peak-to-peak)	Data Rate = 1.25 Gbps REFCLK = 125 MHz Pattern = CJPAT No Equalization	> 0.4			> 0.4			> 0.4			UI
Combined Deterministic and Random Jitter Tolerance (peak-to-peak)	Data Rate = 1.25 Gbps REFCLK = 125 MHz Pattern = CJPAT No Equalization	> 0.66			> 0.66			> 0.66			UI
HiGig Transmit Jitter Generation *(4), (13)*											
Deterministic Jitter (peak-to-peak)	Data Rate = 3.75 Gbps REFCLK = 187.5 MHz Pattern = CJPAT V_{OD} = 1200 mV No Pre-emphasis	-	-	0.17	-						UI
Total Jitter (peak-to-peak)	Data Rate = 3.75 Gbps REFCLK = 187.5 MHz Pattern = CJPAT V_{OD} = 1200 mV No Pre-emphasis	-	-	0.35	-						UI

Table 4–21. PCS Latency (Part 2 of 2) Note (1)

Functional Mode	Configuration	Transmitter PCS Latency					
		TX PIPE	TX Phase Comp FIFO	Byte Serializer	TX State Machine	8B/10B Encoder	Sum (2)
Serial RapidIO	1.25 Gbps, 2.5 Gbps, 3.125 Gbps	-	2-3	1	-	0.5	4-5
SDI	HD 10-bit channel width	-	2-3	1	-	1	4-5
	HD, 3G 20-bit channel width	-	2-3	1	-	0.5	4-5
BASIC Single Width	8-bit/10-bit channel width	-	2-3	1	-	1	4-5
	16-bit/20-bit channel width	-	2-3	1	-	0.5	4-5
BASIC Double Width	16-bit/20-bit channel width	-	2-3	1	-	1	4-5
	32-bit/40-bit channel width	-	2-3	1	-	0.5	4-5
	Parallel Loopback/ BIST	-	2-3	1	-	1	4-5

Notes to Table 4–21:

(1) The latency numbers are with respect to the PLD-transceiver interface clock cycles.

(2) The total latency number is rounded off in the Sum column.

(3) For CPRI 614 Mbps and 1.228 Gbps data rates, the Quartus II software customizes the PLD-transceiver interface clocking to achieve zero clock cycle uncertainty in the transmitter phase compensation FIFO latency. For more details, refer to the *CPRI Mode* section in the *Stratix II GX Transceiver Architecture Overview* chapter in volume 2 of the *Stratix II GX Device Handbook*.

Table 4–41. 1.2-V HSTL Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{OH}	High-level output voltage	I_{OH} = 8 mA	V_{REF} + 0.15		V_{CCIO} + 0.15	V
V_{OL}	Low-level output voltage	I_{OH} = –8 mA	–0.15		V_{REF} – 0.15	V

Table 4–42. 1.5-V HSTL Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.425	1.5	1.575	V
V_{REF}	Input reference voltage		0.713	0.75	0.788	V
V_{TT}	Termination voltage		0.713	0.75	0.788	V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 8 mA *(1)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OH} = –8 mA *(1)*			0.4	V

Note to Table 4–42:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Table 4–43. 1.5-V HSTL Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.425	1.50	1.575	V
V_{REF}	Input reference voltage		0.713	0.75	0.788	V
V_{TT}	Termination voltage		0.713	0.75	0.788	V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = 16 mA *(1)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OH} = –16 mA *(1)*			0.4	V

Note to Table 4–43:

(1) This specification is supported across all the programmable drive settings available for this I/O standard as shown in the *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Table 4–58. DSP Block Internal Timing Microparameters (Part 2 of 2)

Symbol	Parameter	-3 Speed Grade (1)		-3 Speed Grade (2)		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{INREG2PIPE9}$	Input register to DSP block pipeline register in 9 × 9-bit mode	1312	2030	1312	2131	1312	2266	1312	2720	ps
$t_{INREG2PIPE18}$	Input register to DSP block pipeline register in 18 × 18-bit mode	1302	2010	1302	2110	1302	2244	1302	2693	ps
$t_{INREG2PIPE36}$	Input register to DSP block pipeline register in 36 × 36-bit mode	1302	2010	1302	2110	1302	2244	1302	2693	ps
$t_{PIPE2OUTREG2ADD}$	DSP block pipeline register to output register delay in two-multipliers adder mode	924	1450	924	1522	924	1618	924	1943	ps
$t_{PIPE2OUTREG4ADD}$	DSP block pipeline register to output register delay in four-multipliers adder mode	1134	1850	1134	1942	1134	2065	1134	2479	ps
t_{PD9}	Combinational input to output delay for 9 × 9	2100	2880	2100	3024	2100	3214	2100	3859	ps
t_{PD18}	Combinational input to output delay for 18 × 18	2110	2990	2110	3139	2110	3337	2110	4006	ps
t_{PD36}	Combinational input to output delay for 36 × 36	2939	4450	2939	4672	2939	4967	2939	5962	ps
t_{CLR}	Minimum clear pulse width	2212		2322		2469		2964		ps
t_{CLKL}	Minimum clock low time	1190		1249		1328		1594		ps
t_{CLKH}	Minimum clock high time	1190		1249		1328		1594		ps

(1) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
(2) This column refers to –3 speed grades for EP2SGX130 devices.

Table 4–89. Stratix II GX Maximum Input Clock Rate for Row I/O Pins (Part 2 of 2)				
I/O Standard	**-3 Speed Grade**	**-4 Speed Grade**	**-5 Speed Grade**	**Unit**
Differential SSTL-2 Class II	500	500	500	MHz
Differential SSTL-18 Class I	500	500	500	MHz
Differential SSTL-18 Class I I	500	500	500	MHz
1.8-V differential HSTL Class I	500	500	500	MHz
1.8-V differential HSTL Class I I	500	500	500	MHz
1.5-V differential HSTL Class I	500	500	500	MHz
1.5-V differential HSTL Class II	500	500	500	MHz
LVDS *(1)*	520	520	420	MHz
HyperTransport	520	520	420	MHz

(1) The parameters are only available on the left side of the device.

Table 4–90 shows the maximum input clock toggle rates for Stratix II GX device dedicated clock pins.

Table 4–90. Stratix II GX Maximum Input Clock Rate for Dedicated Clock Pins (Part 1 of 2)				
I/O Standard	**-3 Speed Grade**	**-4 Speed Grade**	**-5 Speed Grade**	**Unit**
LVTTL	500	500	400	MHz
2.5 V	500	500	400	MHz
1.8 V	500	500	400	MHz
1.5 V	500	500	400	MHz
LVCMOS	500	500	400	MHz
SSTL-2 Class I	500	500	500	MHz
SSTL-2 Class II	500	500	500	MHz
SSTL-18 Class I	500	500	500	MHz
SSTL-18 Class II	500	500	500	MHz
1.5-V HSTL Class I	500	500	500	MHz
1.5-V HSTL Class II	500	500	500	MHz
1.8-V HSTL CLass I	500	500	500	MHz

Table 4–97. Maximum Output Clock Toggle Rate Derating Factors (Part 5 of 5)

I/O Standard	Drive Strength	Maximum Output Clock Toggle Rate Derating Factors (ps/pF)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Outputs		
		-3	-4	-5	-3	-4	-5	-3	-4	-5
1.5-V differential HSTL Class II *(3)*	16 mA	95	101	101	-	-	-	96	101	101
	18 mA	95	100	100	-	-	-	101	100	100
	20 mA	94	101	101	-	-	-	104	101	101
3.3-V PCI		134	177	177	-	-	-	143	177	177
3.3-V PCI-X		134	177	177	-	-	-	143	177	177
LVDS		-	-	-	155 *(1)*	155 *(1)*	155 *(1)*	134	134	134
LVPECL *(4)*		-	-	-	-	-	-	134	134	134
3.3-V LVTTL	OCT 50 Ω	133	152	152	133	152	152	147	152	152
2.5-V LVTTL	OCT 50 Ω	207	274	274	207	274	274	235	274	274
1.8-V LVTTL	OCT 50 Ω	151	165	165	151	165	165	153	165	165
3.3-V LVCMOS	OCT 50 Ω	300	316	316	300	316	316	263	316	316
1.5-V LVCMOS	OCT 50 Ω	157	171	171	157	171	171	174	171	171
SSTL-2 Class I	OCT 50 Ω	121	134	134	121	134	134	77	134	134
SSTL-2 Class II	OCT 25 Ω	56	101	101	56	101	101	58	101	101
SSTL-18 Class I	OCT 50 Ω	100	123	123	100	123	123	106	123	123
SSTL-18 Class II	OCT 25 Ω	61	110	110	-	-	-	59	110	110
1.2-V HSTL *(2)*	OCT 50 Ω	95	-	-	-	-	-	95	-	-

(1) For LVDS output on row I/O pins the toggle rate derating factors apply to loads larger than 5 pF. In the derating calculation, subtract 5 pF from the intended load value in pF for the correct result. For a load less than or equal to 5 pF, refer to Tables 4–91 through 4–95 for output toggle rates.
(2) 1.2-V HSTL is only supported on column I/O pins on -3 devices.
(3) Differential HSTL and SSTL is only supported on column clock and DQS outputs.
(4) LVPECL is only supported on column clock outputs.

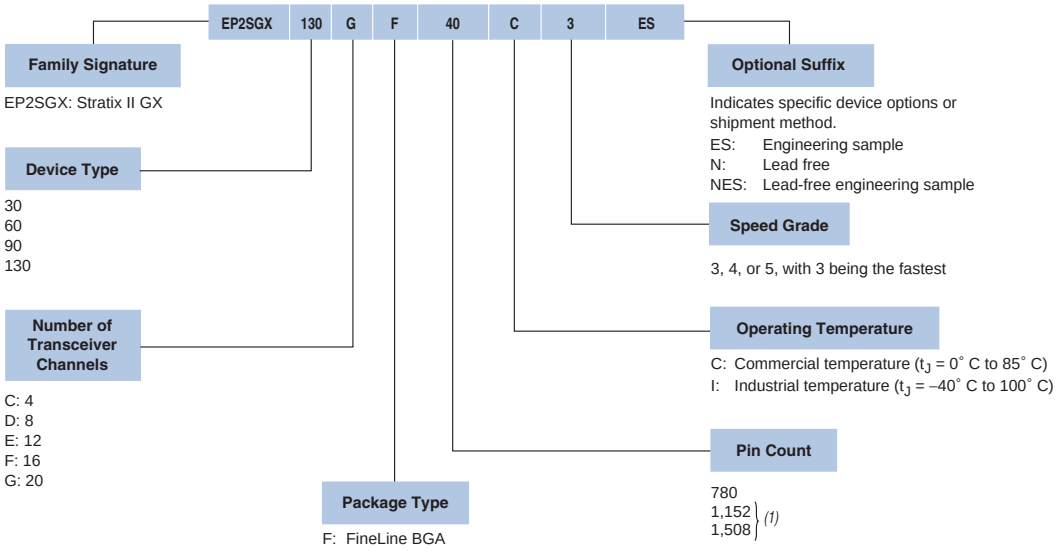
Table 4–104. Maximum DCD for DDIO Output on Row I/O Pins With PLL in the Clock Path

Maximum DCD (ps) for Row DDIO Output I/O Standard	Stratix II GX Devices (PLL Output Feeding DDIO)		Unit
	-3 Device	-4 and -5 Device	
3.3-V LVTTL	110	105	ps
3.3-V LVCMOS	65	75	ps
2.5V	75	90	ps
1.8V	85	100	ps
1.5-V LVCMOS	105	100	ps
SSTL-2 Class I	65	75	ps
SSTL-2 Class II	60	70	ps
SSTL-18 Class I	50	65	ps
1.8-V HSTL Class I	50	70	ps
1.5-V HSTL Class I	55	70	ps
LVDS	180	180	ps

Table 4–105. Maximum DCD for DDIO Output on Column I/O Pins With PLL in the Clock Path (Part 1 of 2)

Maximum DCD (ps) for Column DDIO Output I/O Standard	Stratix II GX Devices (PLL Output Feeding DDIO)		Unit
	-3 Device	-4 and -5 Device	
3.3-V LVTTL	145	160	ps
3.3-V LVCMOS	100	110	ps
2.5V	85	95	ps
1.8V	85	100	ps
1.5-V LVCMOS	140	155	ps
SSTL-2 Class I	65	75	ps
SSTL-2 Class II	60	70	ps
SSTL-18 Class I	50	65	ps
SSTL-18 Class II	70	80	ps
1.8-V HSTL Class I	60	70	ps
1.8-V HSTL Class II	60	70	ps
1.5-V HSTL Class I	55	70	ps
1.5-V HSTL Class II	85	100	ps

Figure 5–1. Stratix II GX Device Packaging Ordering Information



(1) Product code notations for ES silicon for all EP2SGX130 family members (standard and lead free) and EP2SGX90 (lead free) use the following codings to denote pin count: 35 for 1152-pin devices and 40 for 1508-pin devices

Referenced Documents

This chapter references the following documents:

- *Package Information for Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook*
- *Pin-Out Files for Altera Devices*
- *Quartus II Development Software Handbook*

Document Revision History

Table 5–1 shows the revision history for this chapter.

Table 5–1. Document Revision History (Part 1 of 2)

Date and Document Version	Changes Made	Summary of Changes
August 2007 v1.3	Added the "Referenced Documents" section.	
	Minor text edits.	