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Understanding Embedded - FPGAs (Field Programmable Gate Array)

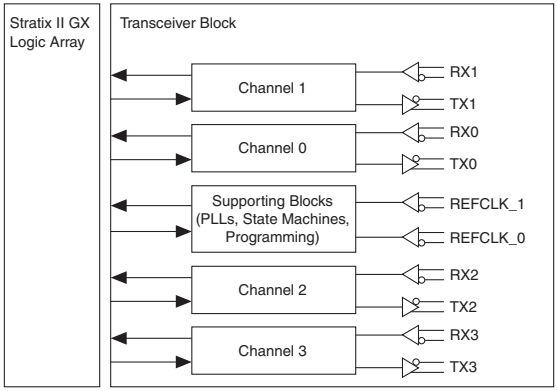
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	4548
Number of Logic Elements/Cells	90960
Total RAM Bits	4520448
Number of I/O	650
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1508-BBGA, FCBGA
Supplier Device Package	1508-FBGA, FC (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2sgx90ff1508c4

Figure 2–2. Elements of the Transceiver Block



Each Stratix II GX transceiver channel consists of a transmitter and receiver. The transceivers are grouped in four and share PLL resources. Each transmitter has access to one of two PLLs. The transmitter contains the following:

- Transmitter phase compensation first-in first-out (FIFO) buffer
- Byte serializer (optional)
- 8B/10B encoder (optional)
- Serializer (parallel-to-serial converter)
- Transmitter differential output buffer

The receiver contains the following:

- Receiver differential input buffer
- Receiver lock detector and run length checker
- Clock recovery unit (CRU)
- Deserializer
- Pattern detector
- Word aligner
- Lane deskew
- Rate matcher (optional)
- 8B/10B decoder (optional)
- Byte deserializer (optional)
- Byte ordering
- Receiver phase compensation FIFO buffer

Designers can preset Stratix II GX transceiver functions using the Quartus® II software. In addition, pre-emphasis, equalization, and differential output voltage (V_{OD}) are dynamically programmable. Each Stratix II GX transceiver channel supports various loopback modes and is

Transmit State Machine

The transmit state machine operates in either PCI Express mode, XAUI mode, or GIGE mode, depending on the protocol used. The state machine is not utilized for certain protocols, such as SONET.

GIGE Mode

In GIGE mode, the transmit state machine converts all idle ordered sets (/K28.5/, /Dx.y/) to either /I1/ or /I2/ ordered sets. /I1/ consists of a negative-ending disparity /K28.5/ (denoted by /K28.5/-) followed by a neutral /D5.6/. /I2/ consists of a positive-ending disparity /K28.5/ (denoted by /K28.5/+) and a negative-ending disparity /D16.2/ (denoted by /D16.2/-). The transmit state machines do not convert any of the ordered sets to match /C1/ or /C2/, which are the configuration ordered sets. (/C1/ and /C2/ are defined by [/K28.5/, /D21.5/] and [/K28.5/, /D2.2/], respectively). Both the /I1/ and /I2/ ordered sets guarantee a negative-ending disparity after each ordered set.

XAUI Mode

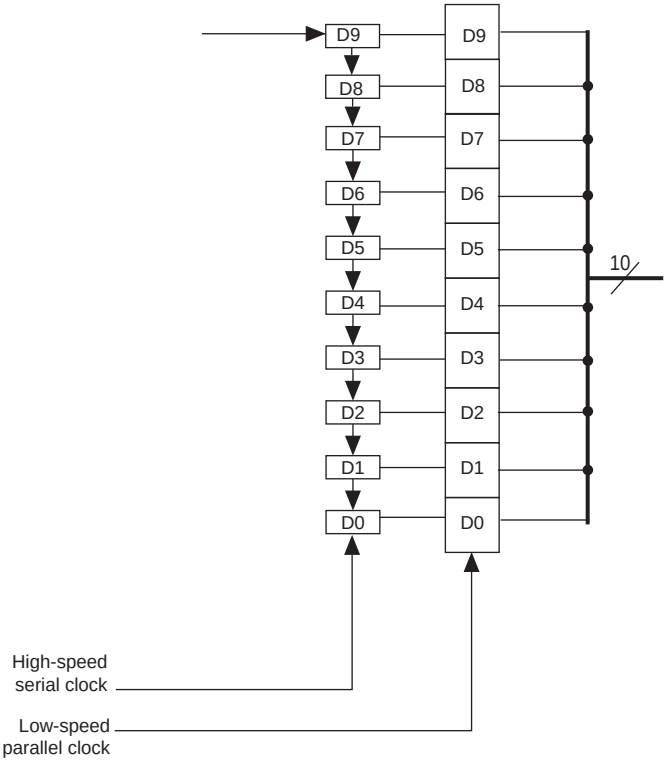
The transmit state machine translates the XAUI XGMII code group to the XAUI PCS code group. Table 2–5 shows the code conversion.

Table 2–5. Code Conversion

XGMII TXC	XGMII TXD	PCS Code-Group	Description
0	00 through FF	Dxx.y	Normal data
1	07	K28.0 or K28.3 or K28.5	Idle in ||**I**||
1	07	K28.5	Idle in ||**T**||
1	9C	K28.4	Sequence
1	FB	K27.7	Start
1	FD	K29.7	Terminate
1	FE	K30.7	Error
1	See IEEE 802.3 reserved code groups	See IEEE 802.3 reserved code groups	Reserved code groups
1	Other value	K30.7	Invalid XGMII character

The XAUI PCS idle code groups, /K28.0/ (/R/) and /K28.5/ (/K/), are automatically randomized based on a PRBS7 pattern with an $x^7 + x^6 + 1$ polynomial. The /K28.3/ (/A/) code group is automatically generated between 16 and 31 idle code groups. The idle randomization on the /A/, /K/, and /R/ code groups is done automatically by the transmit state machine.

Figure 2–17. Deserializer Note (1)



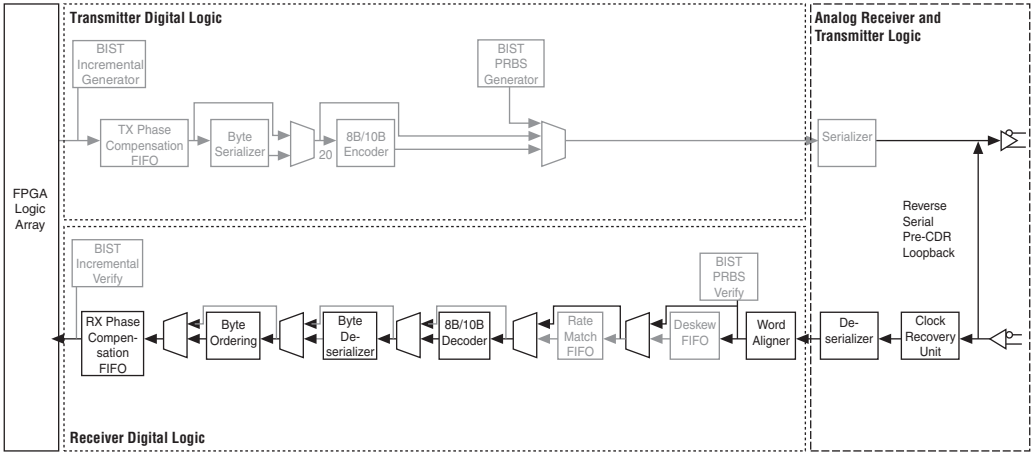
Note to Figure 2–17:
(1) This is a 10-bit deserializer. The deserializer can also convert 8, 16, or 20 bits of data.

Word Aligner

The deserializer block creates 8-, 10-, 16-, or 20-bit parallel data. The deserializer ignores protocol symbol boundaries when converting this data. Therefore, the boundaries of the transferred words are arbitrary. The word aligner aligns the incoming data based on specific byte or word boundaries. The word alignment module is clocked by the local receiver recovered clock during normal operation. All the data and programmed patterns are defined as big-endian (most significant word followed by least significant word). Most-significant-bit-first protocols such as SONET/SDH should reverse the bit order of word align patterns programmed.

Figure 2–27 show the Stratix II GX block in reverse serial pre-CDR loopback mode.

Figure 2–27. Stratix II GX Block in Reverse Serial Pre-CDR Loopback Mode



PCI Express PIPE Reverse Parallel Loopback

This loopback mode, available only in PIPE mode, can be dynamically enabled by the `tx_detectrxloopback` port of the PIPE interface. Figure 2–28 shows the datapath for this mode.

Figure 2–28. Stratix II GX Block in PCI Express PIPE Reverse Parallel Loopback Mode

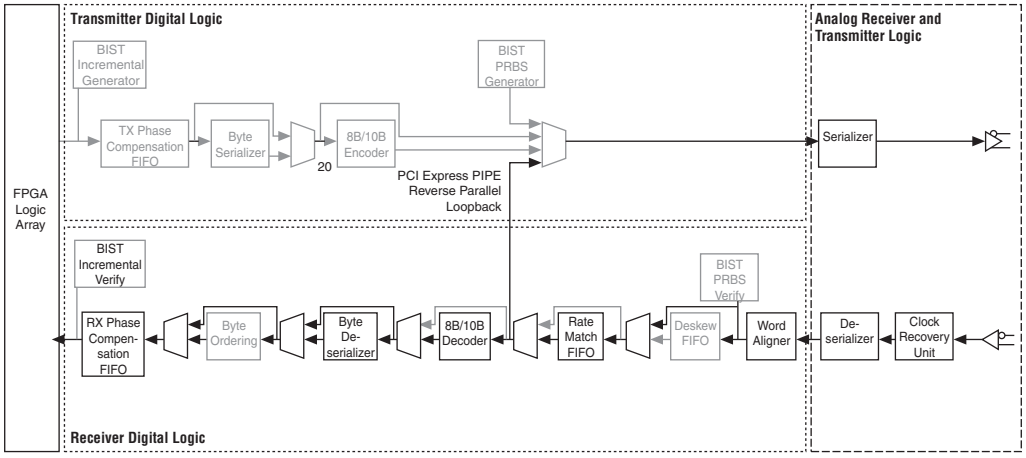
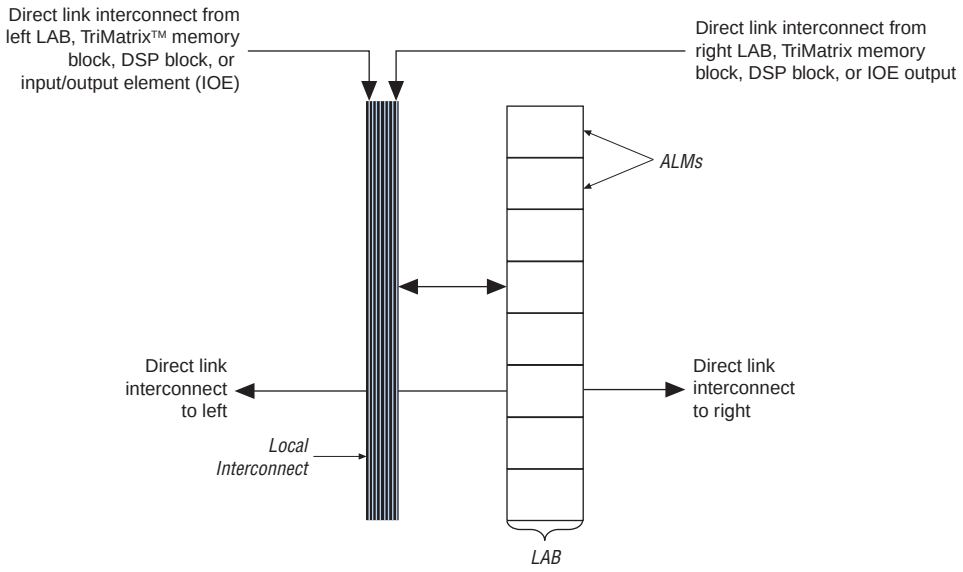


Figure 2–33 shows the direct link connection.

Figure 2–33. Direct Link Connection



LAB Control Signals

Each LAB contains dedicated logic for driving control signals to its ALMs. The control signals include three clocks, three clock enables, two asynchronous clears, synchronous clear, asynchronous preset/load, and synchronous load control signals, providing a maximum of 11 control signals at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use three clocks and three clock enable signals. However, there can only be up to two unique clocks per LAB, as shown in the LAB control signal generation circuit in Figure 2–34. Each LAB's clock and clock enable signals are linked. For example, any ALM in a particular LAB using the `labclk1` signal also uses `labclkena1`. If the LAB uses both the rising and falling edges of a clock, it also uses two LAB-wide clock signals. De-asserting the clock enable signal turns off the corresponding LAB-wide clock. Each LAB can use two asynchronous clear signals and an asynchronous load/preset signal. The asynchronous

One ALM contains two programmable registers. Each register has data, clock, clock enable, synchronous and asynchronous clear, asynchronous load data, and synchronous and asynchronous load/preset inputs.

Global signals, general-purpose I/O pins, or any internal logic can drive the register's clock and clear control signals. Either general-purpose I/O pins or internal logic can drive the clock enable, preset, asynchronous load, and asynchronous load data. The asynchronous load data input comes from the `datae` or `dataf` input of the ALM, which are the same inputs that can be used for register packing. For combinational functions, the register is bypassed and the output of the LUT drives directly to the outputs of the ALM.

Each ALM has two sets of outputs that drive the local, row, and column routing resources. The LUT, adder, or register output can drive these output drivers independently (see Figure 2–36). For each set of output drivers, two ALM outputs can drive column, row, or direct link routing connections, and one of these ALM outputs can also drive local interconnect resources. This allows the LUT or adder to drive one output while the register drives another output. This feature, called register packing, improves device utilization because the device can use the register and the combinational logic for unrelated functions. Another special packing mode allows the register output to feed back into the LUT of the same ALM so that the register is packed with its own fan-out LUT. This feature provides another mechanism for improved fitting. The ALM can also drive out registered and unregistered versions of the LUT or adder output.

See the *Stratix II Performance and Logic Efficiency Analysis White Paper* for more information on the efficiencies of the Stratix II GX ALM and comparisons with previous architectures.

ALM Operating Modes

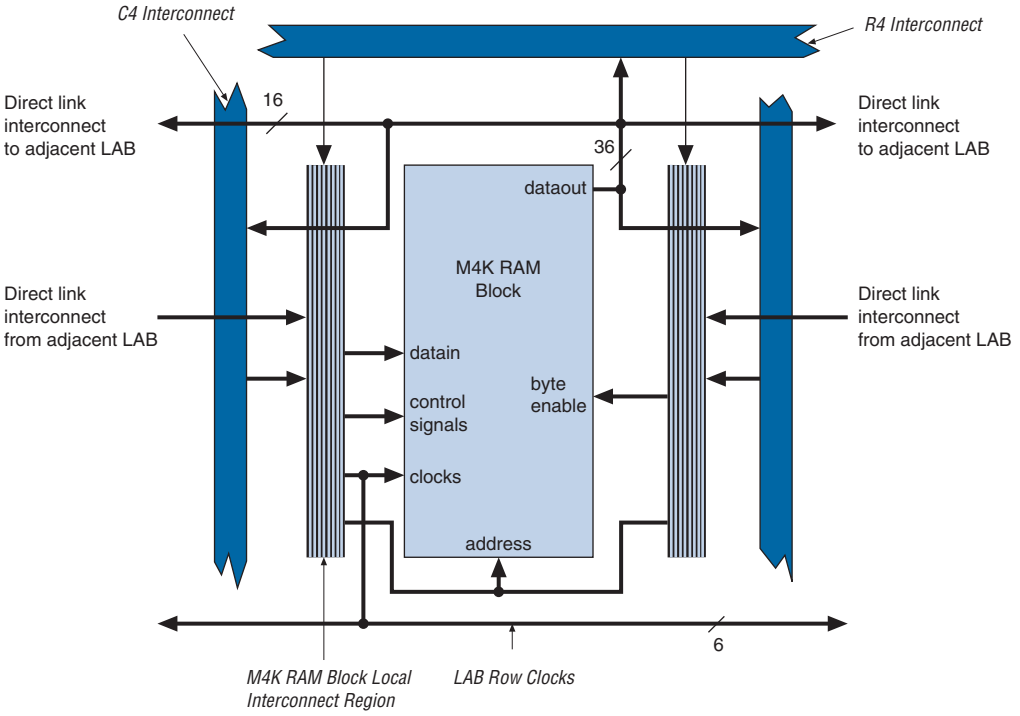
The Stratix II GX ALM can operate in one of the following modes:

- Normal mode
- Extended LUT mode
- Arithmetic mode
- Shared arithmetic mode

Each mode uses ALM resources differently. Each mode has 11 available inputs to the ALM (see Figure 2–35)—the eight data inputs from the LAB local interconnect; carry-in from the previous ALM or LAB; the shared arithmetic chain connection from the previous ALM or LAB; and the register chain connection—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock,

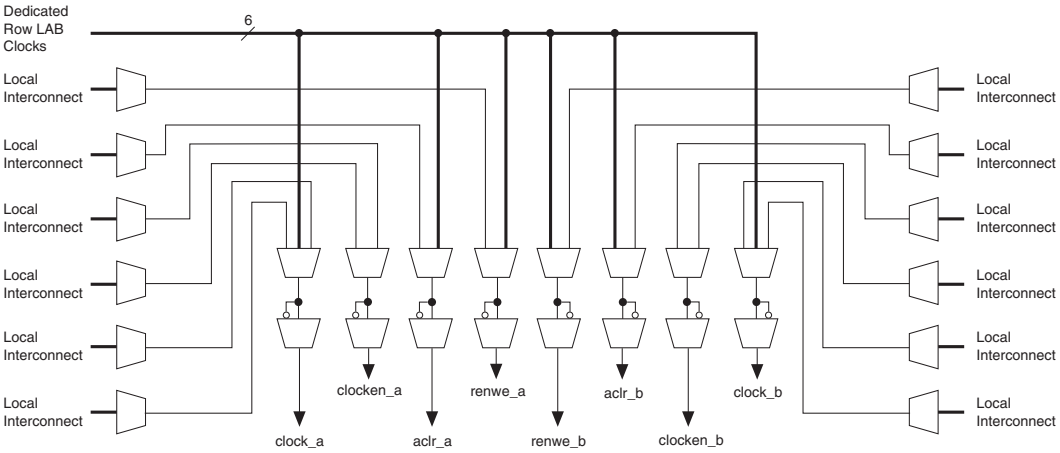
The RAM blocks in Stratix II GX devices have local interconnects to allow ALMs and interconnects to drive into RAM blocks. The M512 RAM block local interconnect is driven by the R4, C4, and direct link interconnects from adjacent LABs. The M512 RAM blocks can communicate with LABs on either the left or right side through these row interconnects or with LAB columns on the left or right side with the column interconnects. The M512 RAM block has up to 16 direct link input connections from the left adjacent LABs and another 16 from the right adjacent LAB. M512 RAM outputs can also connect to left and right LABs through direct link interconnect. The M512 RAM block has equal opportunity for access and performance to and from LABs on either its left or right side. Figure 2–50 shows the M512 RAM block to logic array interface.

Figure 2–50. M512 RAM Block LAB Row Interface



Similar to all RAM blocks, M-RAM blocks can have different clocks on their inputs and outputs. Either of the two clocks feeding the block can clock M-RAM block registers (renwe, address, byte enable, datain, and output registers). The output register can be bypassed. The six labclk signals or local interconnect can drive the control signals for the A and B ports of the M-RAM block. ALMs can also control the clock_a, clock_b, renwe_a, renwe_b, clr_a, clr_b, clocken_a, and clocken_b signals, as shown in Figure 2–53.

Figure 2–53. M-RAM Block Control Signals



The R4, R24, C4, and direct link interconnects from adjacent LABs on either the right or left side drive the M-RAM block local interconnect. Up to 16 direct link input connections to the M-RAM block are possible from the left adjacent LABs and another 16 possible from the right adjacent LAB. M-RAM block outputs can also connect to left and right LABs through direct link interconnect. Figure 2–54 shows an example floorplan for the EP2SGX130 device and the location of the M-RAM interfaces. Figures 2–55 and 2–56 show the interface between the M-RAM block and the logic array.

Table 2–21 shows the number of DSP blocks in each Stratix II GX device. DSP block multipliers can optionally feed an adder/subtractor or accumulator in the block, depending on the configuration, which makes routing to ALMs easier, saves ALM routing resources, and increases performance because all connections and blocks are in the DSP block.

Table 2–21. DSP Blocks in Stratix II GX Devices *Note (1)*

Device	DSP Blocks	Total 9 × 9 Multipliers	Total 18 × 18 Multipliers	Total 36 × 36 Multipliers
EP2SGX30	16	128	64	16
EP2SGX60	36	288	144	36
EP2SGX90	48	384	192	48
EP2SGX130	63	504	252	63

Note to Table 2–21:

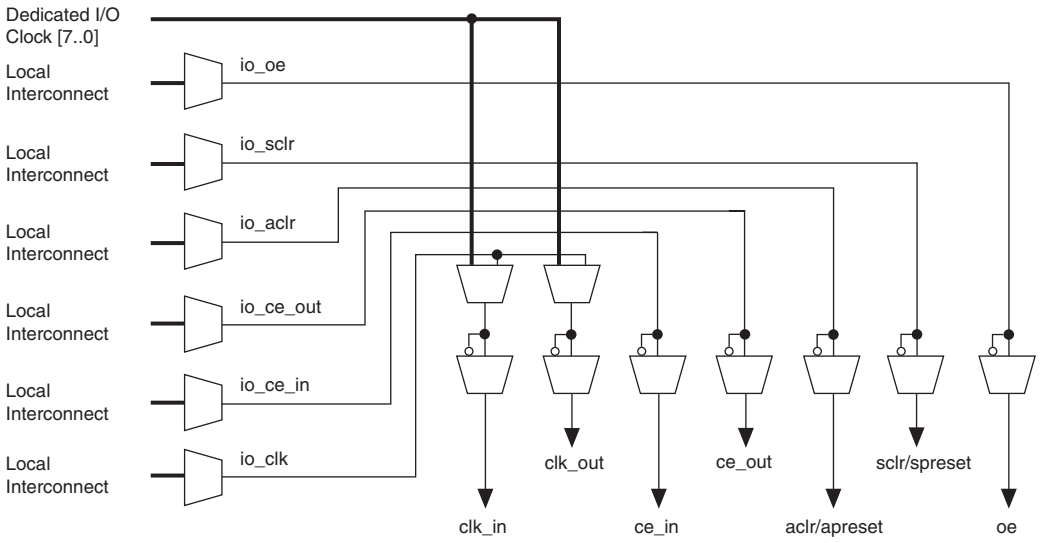
(1) This list only shows functions that can fit into a single DSP block. Multiple DSP blocks can support larger multiplication functions.

Additionally, the DSP block input registers can efficiently implement shift registers for FIR filter applications, and DSP blocks support Q1.15 format rounding and saturation. Figure 2–58 shows the top-level diagram of the DSP block configured for 18 × 18-bit multiplier mode.

Table 2–27. Global and Regional Clock Connections from Left Side Clock Pins and Fast PLL Outputs (Part 2 of 3)

Left Side Global and Regional Clock Network Connectivity	CLK0	CLK1	CLK2	CLK3	RCLK0	RCLK1	RCLK2	RCLK3	RCLK4	RCLK5	RCLK6	RCLK7
Drivers from internal logic												
GCLKDRV0	✓	✓										
GCLKDRV1	✓	✓										
GCLKDRV2			✓	✓								
GCLKDRV3			✓	✓								
RCLKDRV0					✓				✓			
RCLKDRV1						✓				✓		
RCLKDRV2							✓				✓	
RCLKDRV3								✓				✓
RCLKDRV4					✓				✓			
RCLKDRV5						✓				✓		
RCLKDRV6							✓				✓	
RCLKDRV7								✓				✓
PLL 1 outputs												
c0	✓	✓			✓		✓		✓		✓	
c1	✓	✓				✓		✓		✓		✓
c2			✓	✓	✓		✓		✓		✓	
c3			✓	✓		✓		✓		✓		✓
PLL 2 outputs												
c0	✓	✓				✓		✓		✓		✓
c1	✓	✓			✓		✓		✓		✓	
c2			✓	✓		✓		✓		✓		✓
c3			✓	✓	✓		✓		✓		✓	
PLL 7 outputs												
c0			✓	✓		✓		✓				
c1			✓	✓	✓		✓					
c2	✓	✓				✓		✓				
c3	✓	✓			✓		✓					

Figure 2–80. Control Signal Selection per IOE *Note (1)*



Note to Figure 2–80:

(1) Control signals `ce_in`, `ce_out`, `aclr/apreset`, `sclr/spreset`, and `oe` can be global signals even though their control selection multiplexers are not directly fed by the `ioe_clk[7..0]` signals. The `ioe_clk` signals can drive the I/O local interconnect, which then drives the control selection multiplexers.

In normal bidirectional operation, you can use the input register for input data requiring fast setup times. The input register can have its own clock input and clock enable separate from the OE and output registers. The output register can be used for data requiring fast clock-to-output performance. You can use the OE register for fast clock-to-output enable timing. The OE and output register share the same clock source and the same clock enable source from local interconnect in the associated LAB, dedicated I/O clocks, and the column and row interconnects. Figure 2–81 shows the IOE in bidirectional configuration.

Table 2–42. Document Revision History (Part 2 of 6)

Date and Document Version	Changes Made	Summary of Changes
February 2007 v2.0	Added Chapter 02 “Stratix II GX Transceivers” to the beginning of Chapter 03 “Stratix II GX Architecture”. • Changed chapter number to Chapter 02.	Combined Chapter 02 “Stratix II GX Transceivers” and Chapter 03 “Stratix II GX Architecture” in the new Chapter 02 “Stratix II GX Architecture”
	Added the “Document Revision History” section to this chapter.	
	Moved the “Stratix II GX Transceiver Clocking” section to after the “Receiver Path” section.	

generated by the Quartus II software. JRunner is targeted for embedded JTAG configuration. The source code is developed for the Windows NT operating system (OS), but can be customized to run on other platforms.

For more information on the JRunner software driver, refer to the *AN 414: An Embedded Solution for PLD JTAG Configuration* and the source files on the Altera web site (www.altera.com).

Programming Serial Configuration Devices with SRunner

A serial configuration device can be programmed in-system by an external microprocessor using SRunner. SRunner is a software driver developed for embedded serial configuration device programming that can be easily customized to fit into different embedded systems. SRunner reads a Raw Programming Data file (**.rpd**) and writes to serial configuration devices. The serial configuration device programming time using SRunner is comparable to the programming time when using the Quartus II software.

For more information about SRunner, refer to the *AN 418 SRunner: An Embedded Solution for Serial Configuration Device Programming* and the source code on the Altera web site.

For more information on programming serial configuration devices, refer to the *Serial Configuration Devices (EPCS1, EPCS4, EPCS64, and EPCS128) Data Sheet* in the *Configuration Handbook*.

Configuring Stratix II FPGAs with the MicroBlaster Driver

The MicroBlaster software driver supports an RBF programming input file and is ideal for embedded FPP or PS configuration. The source code is developed for the Windows NT operating system, although it can be customized to run on other operating systems.

For more information on the MicroBlaster software driver, refer to the *Configuring the MicroBlaster Fast Passive Parallel Software Driver White Paper* or the *Configuring the MicroBlaster Passive Serial Software Driver White Paper* on the Altera web site.

PLL Reconfiguration

The phase-locked loops (PLLs) in the Stratix II GX device family support reconfiguration of their multiply, divide, VCO-phase selection, and bandwidth selection settings without reconfiguring the entire device. You can use either serial data from the logic array or regular I/O pins to program the PLL's counter settings in a serial chain. This option provides

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 14 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Sinusoidal Jitter Tolerance (peak-to-peak) *(6)*	Jitter Frequency = 22.1 KHz Data Rate = 614.4 Mbps, 1.2288 Gbps, 2.4576 Gbps REFCLK = 61.44 MHz for 614.4 Mbps REFCLK = 122.88 MHz for 1.2288 Gbps and 2.4576 Gbps Pattern = CJPAT Equalizer Setting = 6 DC Gain = 0 dB		> 8.5			> 8.5			N/A		UI
	Jitter Frequency = 1.875 MHz Data Rate = 614.4 Mbps, 1.2288 Gbps, 2.4576 Gbps REFCLK = 61.44 MHz for 614.4 Mbps REFCLK = 122.88 MHz for 1.2288 Gbps and 2.4576 Gbps Pattern = CJPAT Equalizer Setting = 6 DC Gain = 0 dB		> 0.1			> 0.1			N/A		UI

Power Consumption

Altera offers two ways to calculate power for a design: the Excel-based PowerPlay early power estimator power calculator and the Quartus® II PowerPlay power analyzer feature.

The interactive Excel-based PowerPlay early power estimator is typically used prior to designing the FPGA in order to get an estimate of device power. The Quartus II PowerPlay power analyzer provides better quality estimates based on the specifics of the design after place-and-route is complete. The power analyzer can apply a combination of user-entered, simulation-derived and estimated signal activities which, combined with detailed circuit models, can yield very accurate power estimates.

In both cases, these calculations should only be used as an estimation of power, not as a specification.

For more information on PowerPlay tools, refer to the *PowerPlay Early Power Estimators (EPE) and Power Analyzer,* the *Quartus II PowerPlay Analysis and Optimization Technology*, and the *PowerPlay Power Analyzer* chapter in volume 3 of the *Quartus II Handbook*. The PowerPlay early power estimators are available on the Altera web site at **www.altera. com**.

See Table 4–23 on page 42 for typical I_{CC} standby specifications.

Timing Model

The DirectDrive technology and MultiTrack interconnect ensure predictable performance, accurate simulation, and accurate timing analysis across all Stratix II GX device densities and speed grades. This section describes and specifies the performance, internal, external, and PLL timing specifications.

All specifications are representative of worst-case supply voltage and junction temperature conditions.

Preliminary and Final Timing

Timing models can have either preliminary or final status. The Quartus II software issues an informational message during the design compilation if the timing models are preliminary. Table 4–52 shows the status of the Stratix II GX device timing models.

Preliminary status means the timing model is subject to change. Initially, timing numbers are created using simulation results, process data, and other known parameters. These tests are used to make the preliminary numbers as close to the actual timing parameters as possible.

Table 4–54. Timing Measurement Methodology for Input Pins (Part 2 of 2) *Notes (1), (2), (3), (4)*

I/O Standard	Measurement Conditions			Measurement Point
	V_{CCIO} (V)	V_{REF} (V)	Edge Rate (ns)	VMEAS (V)
1.8-V HSTL Class II	1.660	0.830	1.660	0.83
1.5-V HSTL Class I	1.375	0.688	1.375	0.6875
1.5-V HSTL Class II	1.375	0.688	1.375	0.6875
1.2-V HSTL with OCT	1.140	0.570	1.140	0.570
Differential SSTL-2 Class I	2.325	1.163	2.325	1.1625
Differential SSTL-2 Class II	2.325	1.163	2.325	1.1625
Differential SSTL-18 Class I	1.660	0.830	1.660	0.83
Differential SSTL-18 Class II	1.660	0.830	1.660	0.83
1.5-V differential HSTL Class I	1.375	0.688	1.375	0.6875
1.5-V differential HSTL Class II	1.375	0.688	1.375	0.6875
1.8-V differential HSTL Class I	1.660	0.830	1.660	0.83
1.8-V differential HSTL Class II	1.660	0.830	1.660	0.83
LVDS	2.325		0.100	1.1625
LVPECL	3.135		0.100	1.5675

Notes to Table 4–54:

(1) Input buffer sees no load at buffer input.
(2) Input measuring point at buffer input is 0.5 V_{CCIO}.
(3) Output measuring point is 0.5 V_{CC} at internal node.
(4) Input edge rate is 1 V/ns.
(5) Less than 50-mV ripple on V_{CCIO} and V_{CCPD}, V_{CCINT} = 1.15 V with less than 30-mV ripple.
(6) V_{CCPD} = 2.97 V, less than 50-mV ripple on V_{CCIO} and V_{CCPD}, V_{CCINT} = 1.15 V.

Table 4–55. Stratix II GX Performance Notes (Part 3 of 3) *Note (1)*

Applications		Resources Used			Performance				
		ALUTs	TriMatrix Memory Blocks	DSP Blocks	-3 Speed Grade *(2)*	-3 Speed Grade *(3)*	-4 Speed Grade	-5 Speed Grade	Units
TriMatrix Memory MegaRAM block (cont.)	Single port RAM 64K x 9 bit	0	1	0	364.96	347.22	325.73	271.73	MHz
	Simple dual-port RAM 64K x 9 bit	0	1	0	420.16	400.0	375.93	313.47	MHz
	True dual-port RAM 64K x 9 bit	0	1	0	359.71	342.46	322.58	268.09	MHz
DSP block	9 x 9-bit multiplier *(5)*	0	0	1	430.29	409.16	385.2	320.1	MHz
	18 x 18-bit multiplier *(5)*	0	0	1	410.17	390.01	367.1	305.06	MHz
	18 x 18-bit multiplier *(7)*	0	0	1	450.04	428.08	403.22	335.12	MHz
	36 x 36-bit multiplier *(5)*	0	0	1	250.0	238.15	224.01	186.6	MHz
	36 x 36-bit multiplier *(6)*	0	0	1	410.17	390.01	367.1	305.06	MHz
	18-bit, 4-tap FIR filter	0	0	1	410.17	390.01	367.1	305.06	MHz

Notes to Table 4–55:

(1) These design performance numbers were obtained using the Quartus II software.
(2) This column refers to -3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
(3) This column refers to -3 speed grades for EP2SGX130 devices.
(4) This application uses registered inputs and outputs.
(5) This application uses registered multiplier input and output stages within the DSP block.
(6) This application uses registered multiplier input, pipeline, and output stages within the DSP block.
(7) This application uses registered multiplier inputs with outputs of the multiplier stage feeding the accumulator or subtractor within the DSP block.

Table 4–86. Stratix II GX I/O Output Delay for Column Pins (Part 3 of 7)								
I/O Standard	Drive Strength	Parameter	Fast Corner Industrial/ Commercial	-3 Speed Grade *(3)*	-3 Speed Grade *(4)*	-4 Speed Grade	-5 Speed Grade	Unit
SSTL-2 Class I	8 mA	t_{OP}	957	1715	1799	1913	2041	ps
		t_{DIP}	979	1781	1869	1987	2131	ps
	12 mA *(1)*	t_{OP}	940	1672	1754	1865	1991	ps
		t_{DIP}	962	1738	1824	1939	2081	ps
SSTL-2 Class II	16 mA	t_{OP}	918	1609	1688	1795	1918	ps
		t_{DIP}	940	1675	1758	1869	2008	ps
	20 mA	t_{OP}	919	1598	1676	1783	1905	ps
		t_{DIP}	941	1664	1746	1857	1995	ps
	24 mA *(1)*	t_{OP}	915	1596	1674	1781	1903	ps
		t_{DIP}	937	1662	1744	1855	1993	ps
SSTL-18 Class I	4 mA	t_{OP}	953	1690	1773	1886	2012	ps
		t_{DIP}	975	1756	1843	1960	2102	ps
	6 mA	t_{OP}	958	1656	1737	1848	1973	ps
		t_{DIP}	980	1722	1807	1922	2063	ps
	8 mA	t_{OP}	937	1640	1721	1830	1954	ps
		t_{DIP}	959	1706	1791	1904	2044	ps
	10 mA	t_{OP}	942	1638	1718	1827	1952	ps
		t_{DIP}	964	1704	1788	1901	2042	ps
	12 mA *(1)*	t_{OP}	936	1626	1706	1814	1938	ps
		t_{DIP}	958	1692	1776	1888	2028	ps
SSTL-18 Class II	8 mA	t_{OP}	925	1597	1675	1782	1904	ps
		t_{DIP}	947	1663	1745	1856	1994	ps
	16 mA	t_{OP}	937	1578	1655	1761	1882	ps
		t_{DIP}	959	1644	1725	1835	1972	ps
	18 mA	t_{OP}	933	1585	1663	1768	1890	ps
		t_{DIP}	955	1651	1733	1842	1980	ps
	20 mA *(1)*	t_{OP}	933	1583	1661	1766	1888	ps
		t_{DIP}	955	1649	1731	1840	1978	ps

Table 4–95. Stratix II GX Maximum Output Clock Rate for Row Pins (Series Termination) (Part 2 of 2)					
I/O Standard	**Drive Strength**	**-3 Speed Grade**	**-4 Speed Grade**	**-5 Speed Grade**	**Unit**
SSTL-2 Class I	OCT_50_OHMS	600	500	500	MHz
SSTL-2 Class II	OCT_25_OHMS	600	550	500	MHz
SSTL-18 Class I	OCT_50_OHMS	590	400	350	MHz
1.5-V HSTL Class I	OCT_50_OHMS	600	550	500	MHz
1.8-V HSTL Class I	OCT_50_OHMS	650	600	600	MHz
Differential SSTL-2 Class I	OCT_50_OHMS	600	500	500	MHz
Differential SSTL-2 Class II	OCT_25_OHMS	600	550	500	MHz
Differential SSTL-18 Class I	OCT_50_OHMS	590	400	350	MHz
Differential HSTL-18 Class I	OCT_50_OHMS	650	600	600	MHz
Differential HSTL-15 Class I	OCT_50_OHMS	600	550	500	

Table 4–96 shows the maximum output clock toggle rate for Stratix II GX device series-terminated dedicated clock pins.

Table 4–96. Stratix II GX Maximum Output Clock Rate for Dedicated Clock Pins (Series Termination) (Part 1 of 2)					
I/O Standard	**Drive Strength**	**-3 Speed Grade**	**-4 Speed Grade**	**-5 Speed Grade**	**Unit**
LVTTL	OCT_25_OHMS	400	400	350	MHz
	OCT_50_OHMS	400	400	350	MHz
LVCMOS	OCT_25_OHMS	350	350	300	MHz
	OCT_50_OHMS	350	350	300	MHz
2.5 V	OCT_25_OHMS	350	350	300	MHz
	OCT_50_OHMS	350	350	300	MHz
1.8 V	OCT_25_OHMS	700	550	450	MHz
	OCT_50_OHMS	700	550	450	MHz
1.5 V	OCT_50_OHMS	550	450	400	MHz
SSTL-2 Class I	OCT_50_OHMS	600	500	500	MHz
SSTL-2 Class II	OCT_25_OHMS	600	550	500	MHz
SSTL-18 Class I	OCT_50_OHMS	450	400	350	MHz

Table 4–108 shows the high-speed I/O timing specifications for -4 speed grade Stratix II GX devices.

Table 4–108. High-Speed I/O Specifications for -4 Speed Grade *Notes (1), (2)*

Symbol	Conditions			-4 Speed Grade			Unit
				Min	Typ	Max	
$f_{IN} = f_{HSDR} / W$	W = 2 to 32 (LVDS, HyperTransport technology) *(3)*			16		520	MHz
	W = 1 (SERDES bypass, LVDS only)			16		500	MHz
	W = 1 (SERDES used, LVDS only)			150		717	MHz
f_{HSDR} (data rate)	J = 4 to 10 (LVDS, HyperTransport technology)			150		1,040	Mbps
	J = 2 (LVDS, HyperTransport technology)			*(4)*		760	Mbps
	J = 1 (LVDS only)			*(4)*		500	Mbps
$f_{HSDRDPA}$ (DPA data rate)	J = 4 to 10 (LVDS, HyperTransport technology)			150		1,040	Mbps
TCCS	All differential standards			-		200	ps
SW	All differential standards			330		-	ps
Output jitter						190	ps
Output t_{RISE}	All differential I/O standards					160	ps
Output t_{FALL}	All differential I/O standards					180	ps
t_{DUTY}				45	50	55	%
DPA run length						6,400	UI
DPA jitter tolerance	Data channel peak-to-peak jitter			0.44			UI
DPA lock time							Number of repetitions
	SPI-4	0000000000 1111111111	10%	256			
	Parallel Rapid I/O	00001111	25%	256			
		10010000	50%	256			
	Miscellaneous	10101010	100%	256			
		01010101		256			

(1) When J = 4 to 10, the SERDES block is used.
(2) When J = 1 or 2, the SERDES block is bypassed.
(3) The input clock frequency and the W factor must satisfy the following fast PLL VCO specification: 150 ≤nput clock frequency × W ≤1,040.
(4) The minimum specification is dependent on the clock source (fast PLL, enhanced PLL, clock pin, and so on) and the clock routing resource (global, regional, or local) utilized. The I/O differential buffer and input register do not have a minimum toggle rate.