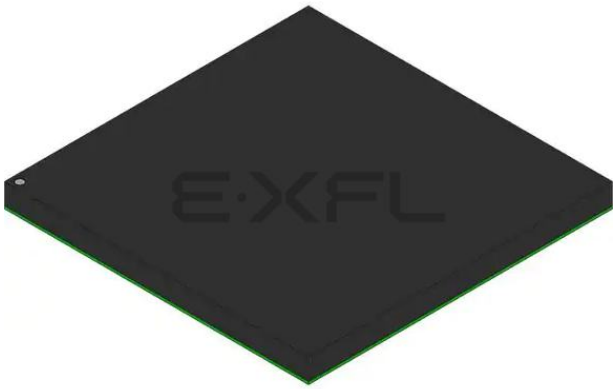
Altera - EP2SGX90FF1508C5 Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	650
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1508-BBGA, FCBGA
Supplier Device Package	1508-FBGA (30x30)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=ep2sgx90ff1508c5

Table 2–4 shows the data path configurations for the Stratix II GX device in single-width and double-width modes.

Refer to the section "8B/10B Encoder" on page 2–8 for a description of the single- and double-width modes.

Table 2–4. Data Path Configurations *Note (1)*

Parameter	Single-Width Mode		Double-Width Mode	
	Without Byte Serialization/ Deserialization	With Byte Serialization/ Deserialization	Without Byte Serialization/ Deserialization	With Byte Serialization/ Deserialization
Fabric to PCS data path width (bits)	8 or 10	16 or 20	16 or 20	32 or 40
Data rate range (Gbps)	0.6 to 2.5	0.6 to 3.125	1 to 5.0	1 to 6.375
PCS to PMA data path width (bits)	8 or 10	8 or 10	16 or 20	16 or 20
Byte ordering *(1)*		✓		✓
Data symbol A (MSB)				✓
Data symbol B		✓		✓
Data symbol C			✓	✓
Data symbol D (LSB)	✓	✓	✓	✓

Note to Table 2–4:
(1) Designs can use byte ordering when byte serialization and deserialization are used.

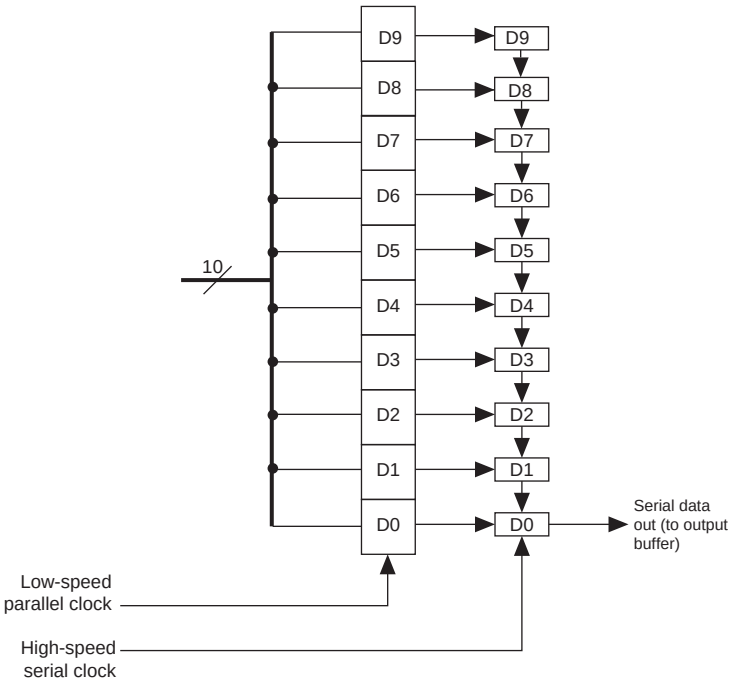
8B/10B Encoder

There are two different modes of operation for 8B/10B encoding. Single-width (8-bit) mode supports natural data rates from 622 Mbps to 3.125 Gbps. Double-width (16-bit cascaded) mode supports data rates above 3.125 Gbps. The encoded data has a maximum run length of five. The 8B/10B encoder can be bypassed. Figure 2–5 diagrams the 10-bit encoding process.

Serializer (Parallel-to-Serial Converter)

The serializer converts the parallel 8, 10, 16, or 20-bit data into a serial data bit stream, transmitting the least significant bit (LSB) first. The serialized data stream is then fed to the high-speed differential transmit buffer. Figure 2–7 is a diagram of the serializer.

Figure 2–7. Serializer *Note (1)*



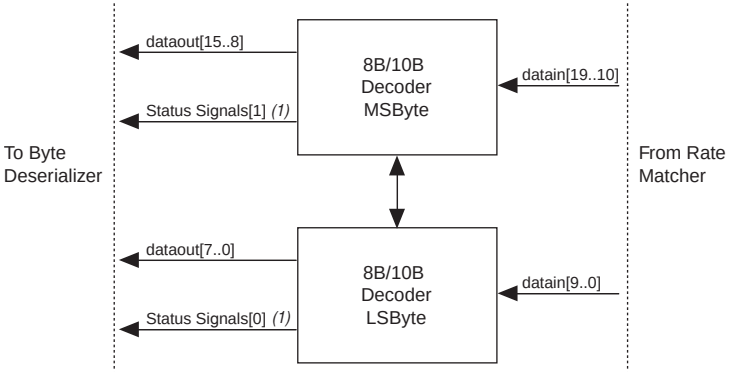
Note to Figure 2–7:
(1) This is a 10-bit serializer. The serializer can also convert 8, 16, and 20 bits of data.

Transmit Buffer

The Stratix II GX transceiver buffers support the 1.2- and 1.5-V PCML I/O standard at rates up to 6.375 Gbps. The common mode voltage (V_{CM}) of the output driver is programmable. The following V_{CM} values are available when the buffer is in 1.2- and 1.5-V PCML.

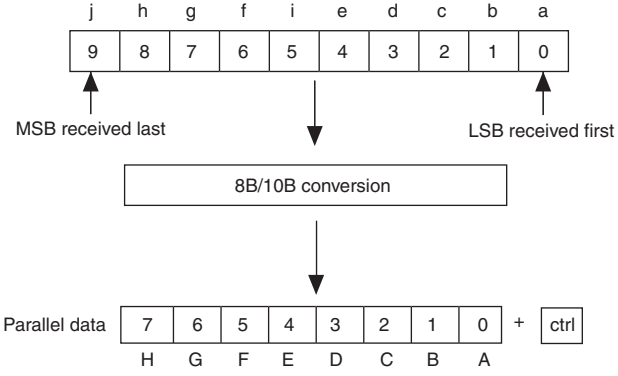
- V_{CM} = 0.6 V
- V_{CM} = 0.7 V

Figure 2–21. 8B/10B Decoder



The 8B/10B decoder in single-width mode translates the 10-bit encoded data into the 8-bit equivalent data or control code. The 10-bit code received must be from the supported Dx.y or Kx.y list with the proper disparity or error flags asserted. All 8B/10B control signals, such as disparity error or control detect, are pipelined with the data and edge-aligned with the data. Figure 2–22 shows how the 10-bit symbol is decoded in the 8-bit data + 1-bit control indicator.

Figure 2–22. 8B/10B Decoder Conversion



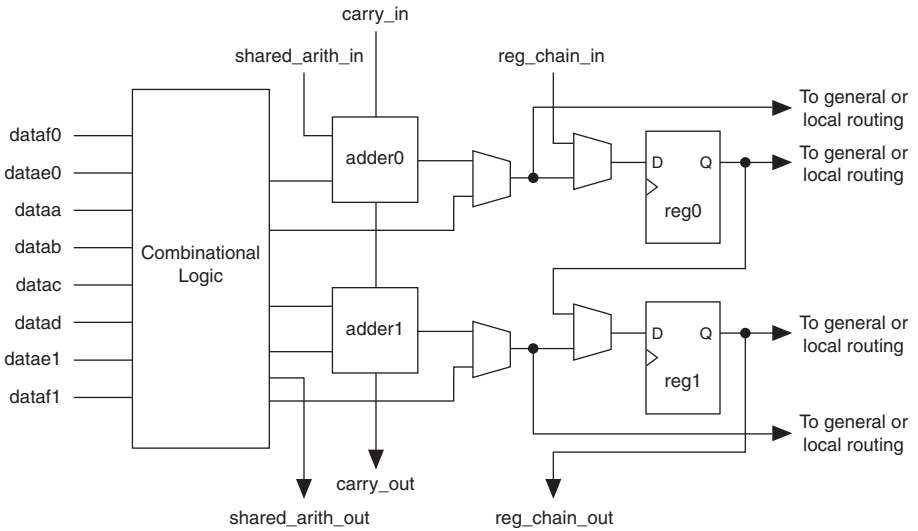
The 8B/10B decoder in double-width mode translates the 20-bit (2 × 10-bits) encoded code into the 16-bit (2 × 8-bits) equivalent data or control code. The 20-bit upper and lower symbols received must be from the supported Dx.y or Kx.y list with the proper disparity or error flags

Adaptive Logic Modules

The basic building block of logic in the Stratix II GX architecture is the ALM. The ALM provides advanced features with efficient logic utilization. Each ALM contains a variety of look-up table (LUT)-based resources that can be divided between two adaptive LUTs (ALUTs). With up to eight inputs to the two ALUTs, one ALM can implement various combinations of two functions. This adaptability allows the ALM to be completely backward-compatible with four-input LUT architectures. One ALM can also implement any function of up to six inputs and certain seven-input functions.

In addition to the adaptive LUT-based resources, each ALM contains two programmable registers, two dedicated full adders, a carry chain, a shared arithmetic chain, and a register chain. Through these dedicated resources, the ALM can efficiently implement various arithmetic functions and shift registers. Each ALM drives all types of interconnects: local, row, column, carry chain, shared arithmetic chain, register chain, and direct link interconnects. Figure 2–35 shows a high-level block diagram of the Stratix II GX ALM while Figure 2–36 shows a detailed view of all the connections in the ALM.

Figure 2–35. High-Level Block Diagram of the Stratix II GX ALM

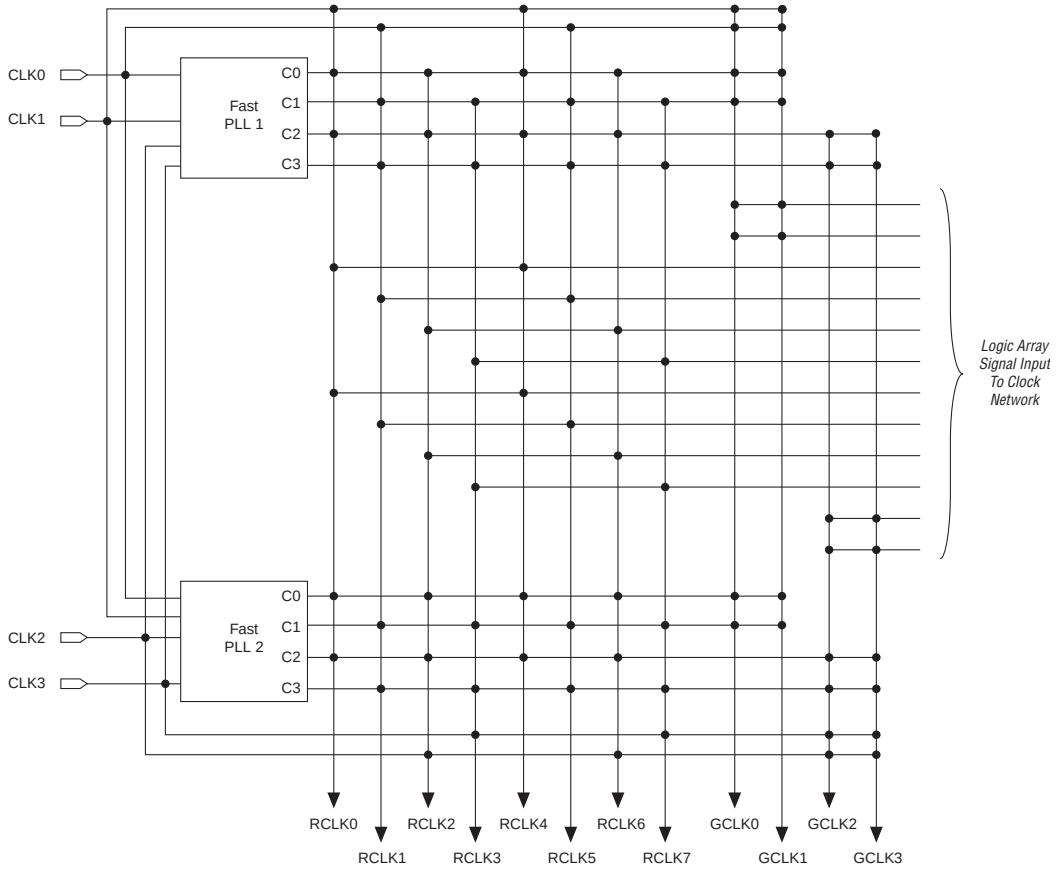


allowing fast horizontal connections to TriMatrix memory and DSP blocks. A shared arithmetic chain can continue as far as a full column. Similar to the carry chains, the shared arithmetic chains are also top- or bottom-half bypassable. This capability allows the shared arithmetic chain to cascade through half of the ALMs in a LAB while leaving the other half available for narrower fan-in functionality. Every other LAB column is top-half bypassable, while the other LAB columns are bottom-half bypassable. Refer to "MultiTrack Interconnect" on page 2–63 for more information on shared arithmetic chain interconnect.

Register Chain

In addition to the general routing outputs, the ALMs in a LAB have register chain outputs. The register chain routing allows registers in the same LAB to be cascaded together. The register chain interconnect allows a LAB to use LUTs for a single combinational function and the registers to be used for an unrelated shift register implementation. These resources speed up connections between ALMs while saving local interconnect resources (see Figure 2–45). The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. See "MultiTrack Interconnect" on page 2–63 for more information about register chain interconnect.

Figure 2–71. Global and Regional Clock Connections from Center Clock Pins and Fast PLL Outputs Notes (1), (2)

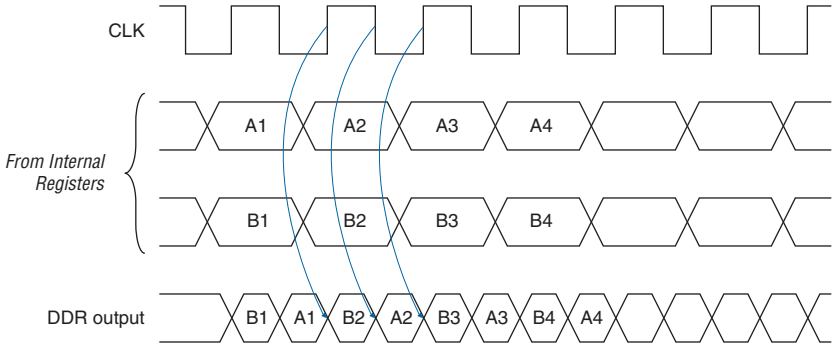


Notes to Figure 2–71:

(1) EP2SGX30C/D and P2SGX60C/D devices only have two fast PLLs (1 and 2) and two Enhanced PLLs (5 and 6), but the connectivity from these PLLs to the global and regional clock networks remains the same as shown.

(2) The global or regional clocks in a fast PLL's quadrant can drive the fast PLL input. A dedicated clock input pin or other PLL must drive the global or regional source. The source cannot be driven by internally generated logic before driving the fast PLL.

Figure 2–85. Output Timing Diagram in DDR Mode



The Stratix II GX IOE operates in bidirectional DDR mode by combining the DDR input and DDR output configurations. The negative-edge-clocked OE register holds the OE signal inactive until the falling edge of the clock to meet DDR SDRAM timing requirements.

External RAM Interfacing

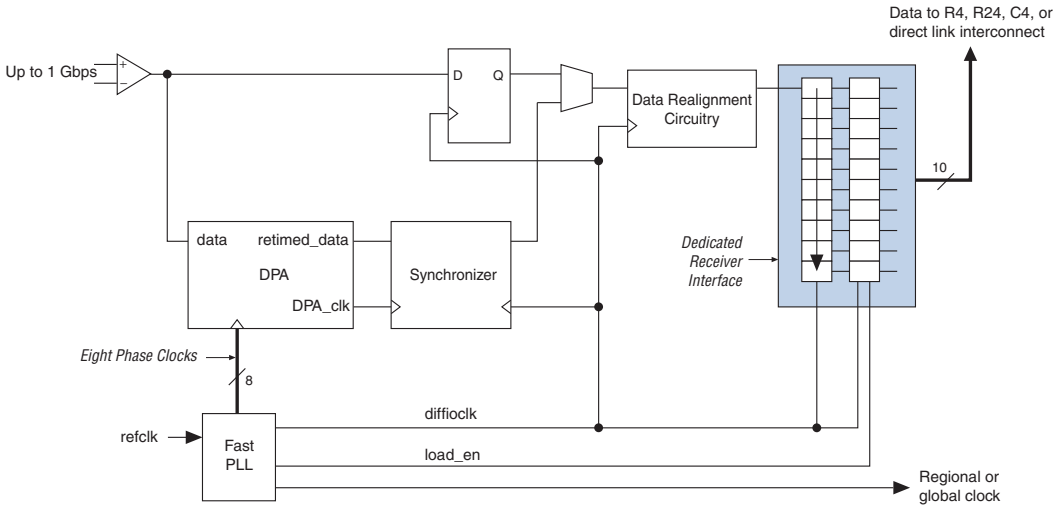
In addition to the six I/O registers in each IOE, Stratix II GX devices also have dedicated phase-shift circuitry for interfacing with external memory interfaces, including DDR and DDR2 SDRAM, QDR II SRAM, RLDRAM II, and SDR SDRAM. In every Stratix II GX device, the I/O banks at the top (banks 3 and 4) and bottom (banks 7 and 8) of the device support DQ and DQS signals with DQ bus modes of ×4, ×8/×9, ×16/×18, or ×32/×36. Table 2–31 shows the number of DQ and DQS buses that are supported per device.

Table 2–31. DQS and DQ Bus Mode Support

Device	Package	Number of ×4 Groups	Number of ×8/×9 Groups	Number of ×16/×18 Groups	Number of ×32/×36 Groups
EP2SGX30	780-pin FineLine BGA	18	8	4	0
EP2SGX60	780-pin FineLine BGA	18	8	4	0
	1,152-pin FineLine BGA	36	18	8	4
EP2SGX90	1,152-pin FineLine BGA	36	18	8	4
	1,508-pin FineLine BGA	36	18	8	4
EP2SGX130	1,508-pin FineLine BGA	36	18	8	4

Figure 2–89 shows the block diagram of the Stratix II GX receiver channel.

Figure 2–89. Stratix II GX Receiver Channel



An external pin or global or regional clock can drive the fast PLLs, which can output up to three clocks: two multiplied high-speed clocks to drive the SERDES block and/or external pin, and a low-speed clock to drive the logic array. In addition, eight phase-shifted clocks from the VCO can feed to the DPA circuitry.

For more information on the fast PLL, see the *PLLs in Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Handbook*.

The eight phase-shifted clocks from the fast PLL feed to the DPA block. The DPA block selects the closest phase to the center of the serial data eye to sample the incoming data. This allows the source-synchronous circuitry to capture incoming data correctly regardless of the channel-to-channel or clock-to-channel skew. The DPA block locks to a phase closest to the serial data phase. The phase-aligned DPA clock is used to write the data into the synchronizer.

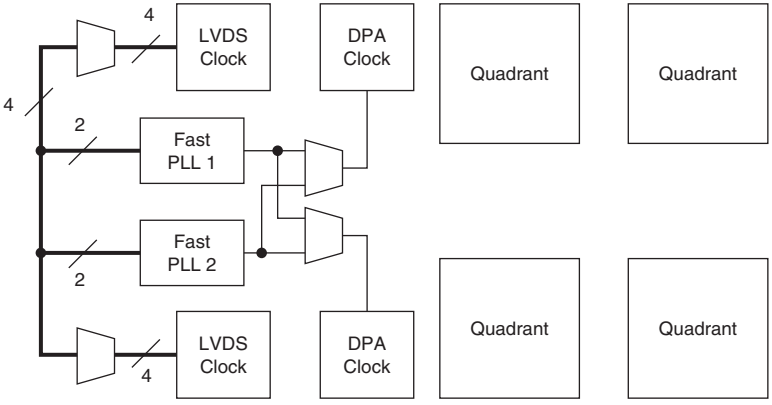
The synchronizer sits between the DPA block and the data realignment and SERDES circuitry. Since every channel utilizing the DPA block can have a different phase selected to sample the data, the synchronizer is needed to synchronize the data to the high-speed clock domain of the data realignment and the SERDES circuitry.

For high-speed source synchronous interfaces such as POS-PHY 4 and the Parallel RapidIO standard, the source synchronous clock rate is not a byte- or SERDES-rate multiple of the data rate. Byte alignment is necessary for these protocols because the source synchronous clock does not provide a byte or word boundary since the clock is one half the data rate, not one eighth. The Stratix II GX device's high-speed differential I/O circuitry provides dedicated data realignment circuitry for user-controlled byte boundary shifting. This simplifies designs while saving ALM resources. You can use an ALM-based state machine to signal the shift of receiver byte boundaries until a specified pattern is detected to indicate byte alignment.

Fast PLL and Channel Layout

The receiver and transmitter channels are interleaved such that each I/O bank on the left side of the device has one receiver channel and one transmitter channel per LAB row. Figure 2–90 shows the fast PLL and channel layout in the EP2SGX30C/D and EP2SGX60C/D devices. Figure 2–91 shows the fast PLL and channel layout in EP2SGX60E, EP2SGX90E/F, and EP2SGX130G devices.

Figure 2–90. Fast PLL and Channel Layout in the EP2SGX30C/D and EP2SGX60C/D Devices *Note (1)*



Note to Figure 2–90:
(1) See Table 2–38 for the number of channels each device supports.

Table 2–42. Document Revision History (Part 6 of 6)

Date and Document Version	Changes Made	Summary of Changes
Previous Chapter 03 changes: December 2005 v1.1	Updated Figure 3–56.	
Previous Chapter 03 changes: October 2005 v1.0	Added chapter to the *Stratix II GX Device Handbook*.	

Table 4–6. Stratix II GX Transceiver Block AC Specification (Part 4 of 6)

Symbol / Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Bandwidth at 3.125 Gbps	BW = Low	-	30	-	-	30	-	-	30	-	MHz
	BW = Med	-	40	-	-	40	-	-	40	-	MHz
	BW = High	-	50	-	-	50	-	-	50	-	MHz
Bandwidth at 2.5 Gbps	BW = Low	-	35	-	-	35	-	-	35	-	MHz
	BW = Med	-	50	-	-	50	-	-	50	-	MHz
	BW = High	-	60	-	-	60	-	-	60	-	MHz
Return loss differential mode		100 MHz to 2.5 GHz (XAUI): -10 dB 50 MHz to 1.25 GHz (PCI-E): -10 dB 100 MHz to 4.875 GHz (OIF/CEI): -8dB 4.875 GHz to 10 GHz (OIF/CEI): 16.6 dB/decade slope									
Return loss common mode		100 MHz to 2.5 GHz (XAUI): -6 dB 50 MHz to 1.25 GHz (PCI-E): -6 dB 100 MHz to 4.875 GHz (OIF/CEI): -6dB 4.875 GHz to 10 GHz (OIF/CEI): 16.6 dB/decade slope									
Programmable PPM detector *(2)*		±62.5, 100, 125, 200, 250, 300, 500, 1000			±62.5, 100, 125, 200, 250, 300, 500, 1000			±62.5, 100, 125, 200, 250, 300, 500, 1000			ppm
Run length *(3)*, *(9)*		80			80			80			UI
Programmable equalization		-	-	16	-	-	16	-	-	16	dB
Signal detect/loss threshold *(4)*		65	-	175	65	-	175	65	-	175	mV
CDR LTR TIme *(5)*, *(9)*		-	-	75	-	-	75	-	-	75	us
CDR Minimum T1b *(6)*, *(9)*		15	-	-	15	-	-	15	-	-	us
LTD lock time *(7)*, *(9)*		0	100	4000	0	100	4000	0	100	4000	ns
Data lock time from `rx_freqlocked` *(8)*, *(9)*		-	-	4	-	-	4	-	-	4	us
Programmable DC gain		0, 3, 6			0, 3, 6			0, 3, 6			dB
Transmitter											

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 8 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
GIGE Transmit Jitter Generation *(12)*											
Deterministic Jitter (peak-to-peak)	Data Rate = 1.25 Gbps REFCLK = 125 MHz Pattern = CRPAT V_{OD} = 1400 mV No Pre-emphasis	-	-	0.14	-	-	0.14	-	-	0.14	UI
Total Jitter (peak-to-peak)	Data Rate = 1.25 Gbps REFCLK = 125 MHz Pattern = CRPAT V_{OD} = 1400 mV No Pre-emphasis	-	-	0.279	-	-	0.279	-	-	0.279	UI
GIGE Receiver Jitter Tolerance *(12)*											
Deterministic Jitter Tolerance (peak-to-peak)	Data Rate = 1.25 Gbps REFCLK = 125 MHz Pattern = CJPAT No Equalization	> 0.4			> 0.4			> 0.4			UI
Combined Deterministic and Random Jitter Tolerance (peak-to-peak)	Data Rate = 1.25 Gbps REFCLK = 125 MHz Pattern = CJPAT No Equalization	> 0.66			> 0.66			> 0.66			UI
HiGig Transmit Jitter Generation *(4), (13)*											
Deterministic Jitter (peak-to-peak)	Data Rate = 3.75 Gbps REFCLK = 187.5 MHz Pattern = CJPAT V_{OD} = 1200 mV No Pre-emphasis	-	-	0.17	-						UI
Total Jitter (peak-to-peak)	Data Rate = 3.75 Gbps REFCLK = 187.5 MHz Pattern = CJPAT V_{OD} = 1200 mV No Pre-emphasis	-	-	0.35	-						UI

DC Electrical Characteristics

Table 4–23 shows the Stratix II GX device family DC electrical characteristics.

Table 4–23. Stratix II GX Device DC Operating Conditions (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions	Device	Minimum	Typical	Maximum	Unit
I_I	Input pin leakage current	$V_I = V_{CCIOmax}$ to 0 V *(2)*	All	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CCIOmax}$ to 0 V *(2)*	All	–10		10	µA
I_{CCINT0}	V_{CCINT} supply current (standby)	V_I = ground, no load, no toggling inputs T_J = 25 °C	EP2SGX30		0.30	*(3)*	A
			EP2SGX60		0.50	*(3)*	A
			EP2SGX90		0.62	*(3)*	A
			EP2SGX130		0.82	*(3)*	A
I_{CCPD0}	V_{CCPD} supply current (standby)	V_I = ground, no load, no toggling inputs T_J = 25 °C, V_{CCPD} = 3.3V	EP2SGX30		2.7	*(3)*	mA
			EP2SGX60		3.6	*(3)*	mA
			EP2SGX90		4.3	*(3)*	mA
			EP2SGX130		5.4	*(3)*	mA
I_{CCIO0}	V_{CCIO} supply current (standby)	V_I = ground, no load, no toggling inputs T_J = 25 °C	EP2SGX30		4.0	*(3)*	mA
			EP2SGX60		4.0	*(3)*	mA
			EP2SGX90		4.0	*(3)*	mA
			EP2SGX130		4.0	*(3)*	mA

Final timing numbers are based on actual device operation and testing. These numbers reflect the actual performance of the device under worst-case voltage and junction temperature conditions.

Table 4–52. Stratix II GX Device Timing Model Status

Device	Preliminary	Final
EP2SGX30		✓
EP2SGX60		✓
EP2SGX90		✓
EP2SGX130		✓

I/O Timing Measurement Methodology

Different I/O standards require different baseline loading techniques for reporting timing delays. Altera characterizes timing delays with the required termination for each I/O standard and with 0 pF (except for PCI and PCI-X which use 10 pF) loading and the timing is specified up to the output pin of the FPGA device. The Quartus II software calculates the I/O timing for each I/O standard with a default baseline loading as specified by the I/O standards.

The following measurements are made during device characterization. Altera measures clock-to-output delays (t_{CO}) at worst-case process, minimum voltage, and maximum temperature (PVT) for default loading conditions shown in Table 4–53. Use the following equations to calculate clock pin to output pin timing for Stratix II GX devices.

t_{CO} from clock pin to I/O pin = delay from clock pad to I/O output register + IOE output register clock-to-output delay + delay from output register to output pin + I/O output delay

t_{xz}/t_{zx} from clock pin to I/O pin = delay from clock pad to I/O output register + IOE output register clock-to-output delay + delay from output register to output pin + I/O output delay + output enable pin delay

Simulation using IBIS models is required to determine the delays on the PCB traces in addition to the output pin delay timing reported by the Quartus II software and the timing model in the device handbook.

1. Simulate the output driver of choice into the generalized test setup, using values from Table 4–53.
2. Record the time to V_{MEAS}.

Table 4–65. EP2SGX30 Column Pins Regional Clock Timing Parameters

Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.493	1.507	2.522	2.806	3.364	ns
t_{COUT}	1.353	1.372	2.525	2.809	3.364	ns
t_{PLLCIN}	0.087	0.104	0.237	0.253	0.292	ns
$t_{PLLCOUT}$	-0.078	-0.061	0.237	0.253	0.29	ns

Table 4–66. EP2SGX30 Row Pins Regional Clock Timing Parameters

Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.246	1.262	2.437	2.712	3.246	ns
t_{COUT}	1.251	1.267	2.437	2.712	3.246	ns
t_{PLLCIN}	-0.18	-0.167	0.215	0.229	0.263	ns
$t_{PLLCOUT}$	-0.175	-0.162	0.215	0.229	0.263	ns

EP2SGX60 Clock Timing Parameters

Tables 4–67 through 4–70 show the maximum clock timing parameters for EP2SGX60 devices.

Table 4–67. EP2SGX60 Column Pins Global Clock Timing Parameters

Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.722	1.736	2.940	3.275	3.919	ns
t_{COUT}	1.557	1.571	2.698	3.005	3.595	ns
t_{PLLCIN}	0.037	0.051	0.474	0.521	0.613	ns
$t_{PLLCOUT}$	-0.128	-0.114	0.232	0.251	0.289	ns

Table 4–81. Stratix II GX IOE Programmable Delay on Row Pins Note (1)													
Parameter	Paths Affected	Available Settings	Minimum Timing		-3 Speed Grade		-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		Unit
			Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	
Input delay from pin to internal cells	Pad to I/O dataout to logic array	8	0	1782	0	2876	0	3020	0	3212	0	3853	ps
Input delay from pin to input register	Pad to I/O input register	64	0	2054	0	3270	0	3434	0	3652	0	4381	ps
Delay from output register to output pin	I/O output register to pad	2	0	332	0	500	0	525	0	559	0	670	ps
Output enable pin delay	t_{XZ}, t_{ZX}	2	0	320	0	483	0	507	0	539	0	647	ps

(1) The incremental values for the settings are generally linear. For the exact delay associated with each setting, use the latest version of the Quartus II software.

Default Capacitive Loading of Different I/O Standards

See Table 4–82 for default capacitive loading of different I/O standards.

Table 4–82. Default Loading of Different I/O Standards for Stratix II GX Devices (Part 1 of 2)		
I/O Standard	Capacitive Load	Unit
LVTTL	0	pF
LVCMOS	0	pF
2.5 V	0	pF
1.8 V	0	pF
1.5 V	0	pF
PCI	10	pF
PCI-X	10	pF
SSTL-2 Class I	0	pF
SSTL-2 Class II	0	pF

Table 4–87. Stratix II GX I/O Output Delay for Row Pins (Part 3 of 4)

I/O Standard	Drive Strength	Parameter	Fast Corner Industrial/ Commercial	-3 Speed Grade *(3)*	-3 Speed Grade *(4)*	-4 Speed Grade	-5 Speed Grade	Unit
SSTL-18 Class I	4 mA	t_{OP}	1038	1709	1793	1906	2046	ps
		t_{DIP}	995	1654	1736	1846	1973	ps
	6 mA	t_{OP}	1042	1648	1729	1838	1975	ps
		t_{DIP}	999	1593	1672	1778	1902	ps
	8 mA	t_{OP}	1018	1633	1713	1821	1958	ps
		t_{DIP}	975	1578	1656	1761	1885	ps
	10 mA *(1)*	t_{OP}	1021	1615	1694	1801	1937	ps
		t_{DIP}	978	1560	1637	1741	1864	ps
1.8-V HSTL Class I	4 mA	t_{OP}	1019	1610	1689	1795	1956	ps
		t_{DIP}	976	1555	1632	1735	1883	ps
	6 mA	t_{OP}	1022	1580	1658	1762	1920	ps
		t_{DIP}	979	1525	1601	1702	1847	ps
	8 mA	t_{OP}	1004	1576	1653	1757	1916	ps
		t_{DIP}	961	1521	1596	1697	1843	ps
	10 mA	t_{OP}	1008	1567	1644	1747	1905	ps
		t_{DIP}	965	1512	1587	1687	1832	ps
	12 mA *(1)*	t_{OP}	999	1566	1643	1746	1904	ps
		t_{DIP}	956	1511	1586	1686	1831	ps
1.5-V HSTL Class I	4 mA	t_{OP}	1018	1591	1669	1774	1933	ps
		t_{DIP}	975	1536	1612	1714	1860	ps
	6 mA	t_{OP}	1021	1579	1657	1761	1919	ps
		t_{DIP}	978	1524	1600	1701	1846	ps
	8 mA *(1)*	t_{OP}	1006	1572	1649	1753	1911	ps
		t_{DIP}	963	1517	1592	1693	1838	ps
Differential SSTL-2 Class I	8 mA	t_{OP}	1050	1759	1846	1962	2104	ps
		t_{DIP}	1007	1704	1789	1902	2031	ps
	12 mA	t_{OP}	1026	1694	1777	1889	2028	ps
		t_{DIP}	983	1639	1720	1829	1955	ps
Differential SSTL-2 Class II	16 mA	t_{OP}	992	1581	1659	1763	1897	ps
		t_{DIP}	949	1526	1602	1703	1824	ps

Table 4–90. Stratix II GX Maximum Input Clock Rate for Dedicated Clock Pins (Part 2 of 2)				
I/O Standard	**-3 Speed Grade**	**-4 Speed Grade**	**-5 Speed Grade**	**Unit**
1.8-V HSTL CLass I	500	500	500	MHz
PCI	500	500	400	MHz
PCI-X	500	500	400	MHz
Differential SSTL-2 Class I	500	500	500	MHz
Differential SSTL-2 Class II	500	500	500	MHz
Differential SSTL-18 Class I	500	500	500	MHz
Differential SSTL-18 Class II	500	500	500	MHz
1.8-V differential HSTL Class I	500	500	500	MHz
1.8-V differential HSTL Class II	500	500	500	MHz
1.5-V differential HSTL Class I	500	500	500	MHz
1.5-V differential HSTL Class I I	500	500	500	MHz
HyperTransport *(1)*	717	717	640	MHz
	450	450	400	MHz
LVPECL *(1)*, *(2)*	717	717	640	MHz
	450	450	400	MHz
LVDS *(1)*	717	717	640	MHz
	450	450	400	MHz

(1) The first set of numbers refers to the HIO dedicated clock pins. The second set of numbers refers to the VIO dedicated clock pins.
(2) LVPECL is only supported on column clock pins.

Table 4–93. Stratix II GX Maximum Output Clock Rate for Dedicated Clock Pins (Part 4 of 4)					
I/O Standard	Drive Strength	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
1.8-V differential Class II	16 mA	500	500	450	MHz
	18 mA	550	500	500	MHz
	20 mA	550	550	550	MHz
1.5-V differential Class I	4 mA	350	300	300	MHz
	6 mA	500	500	450	MHz
	8 mA	700	650	600	MHz
	10 mA	700	700	650	MHz
	12 mA	700	700	700	MHz
1.5-V differential Class II	16 mA	600	600	550	MHz
	18 mA	650	600	600	MHz
	20 mA	700	650	600	MHz
HyperTransport	-	300	250	125	MHz
LVPECL	-	450	400	300	MHz

(1) This is the default setting in Quartus II software.

Table 4–94 shows the maximum output clock toggle rate for Stratix II GX device series-terminated column pins.

Table 4–94. Stratix II GX Maximum Output Clock Rate for Column Pins (Series Termination) (Part 1 of 2)					
I/O Standard	Drive Strength	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
LVTTL	OCT_25_OHMS	400	400	350	MHz
	OCT_50_OHMS	400	400	350	MHz
LVCMOS	OCT_25_OHMS	350	350	300	MHz
	OCT_50_OHMS	350	350	300	MHz
2.5 V	OCT_25_OHMS	350	350	300	MHz
	OCT_50_OHMS	350	350	300	MHz
1.8 V	OCT_25_OHMS	700	550	450	MHz
	OCT_50_OHMS	700	550	450	MHz
1.5 V	OCT_50_OHMS	550	450	400	MHz
SSTL-2 Class I	OCT_50_OHMS	600	500	500	MHz
SSTL-2 Class II	OCT_25_OHMS	600	550	500	MHz

Table 4–100. Maximum DCD for DDIO Output on Row I/O Pins Without PLL in the Clock Path for -3 Devices *Note (1)*

Maximum DCD (ps) for Row DDIO Output I/O Standard	Input I/O Standard (No PLL in Clock Path)					Unit
	TTL/CMOS		SSTL-2	SSTL/HSTL	LVDS	
	3.3 and 2.5 V	1.8 and 1.5 V	2.5 V	1.8 and 1.5 V	3.3 V	
3.3-V LVTTL	260	380	145	145	110	ps
3.3-V LVCMOS	210	330	100	100	65	ps
2.5 V	195	315	85	85	75	ps
1.8 V	150	265	85	85	120	ps
1.5-V LVCMOS	255	370	140	140	105	ps
SSTL-2 Class I	175	295	65	65	70	ps
SSTL-2 Class II	170	290	60	60	75	ps
SSTL-18 Class I	155	275	55	50	90	ps
1.8-V HSTL Class I	150	270	60	60	95	ps
1.5-V HSTL Class I	150	270	55	55	90	ps
LVDS	180	180	180	180	180	ps

(1) The information in Table 4–100 assumes the input clock has zero DCD.

Here is an example for calculating the DCD in percentage for a DDIO output on a row I/O on a -3 device:

If the input I/O standard is 2.5-V SSTL-2 and the DDIO output I/O standard is SSTL-2 Class= II, the maximum DCD is 60 ps (see Table 4–100). If the clock frequency is 267 MHz, the clock period T is:

T = 1/ f = 1 / 267 MHz = 3.745 ns = 3,745 ps

Calculate the DCD as a percentage:

(T/2 – DCD) / T = (3,745 ps/2 – 60 ps) / 3745 ps = 48.4% (for low boundary)

(T/2 + DCD) / T = (3,745 ps/2 + 60 ps) / 3745 ps = 51.6% (for high boundary)