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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	4548
Number of Logic Elements/Cells	90960
Total RAM Bits	4520448
Number of I/O	650
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1508-BBGA, FCBGA
Supplier Device Package	1508-FBGA, FC (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2sgx90ff1508c5n

1. Introduction

SIIGX51001-1.6

The Stratix® II GX family of devices is Altera's third generation of FPGAs to combine high-speed serial transceivers with a scalable, high-performance logic array. Stratix II GX devices include 4 to 20 high-speed transceiver channels, each incorporating clock and data recovery unit (CRU) technology and embedded SERDES capability at data rates of up to 6.375 gigabits per second (Gbps). The transceivers are grouped into four-channel transceiver blocks and are designed for low power consumption and small die size. The Stratix II GX FPGA technology is built upon the Stratix II architecture and offers a 1.2-V logic array with unmatched performance, flexibility, and time-to-market capabilities. This scalable, high-performance architecture makes Stratix II GX devices ideal for high-speed backplane interface, chip-to-chip, and communications protocol-bridging applications.

Features

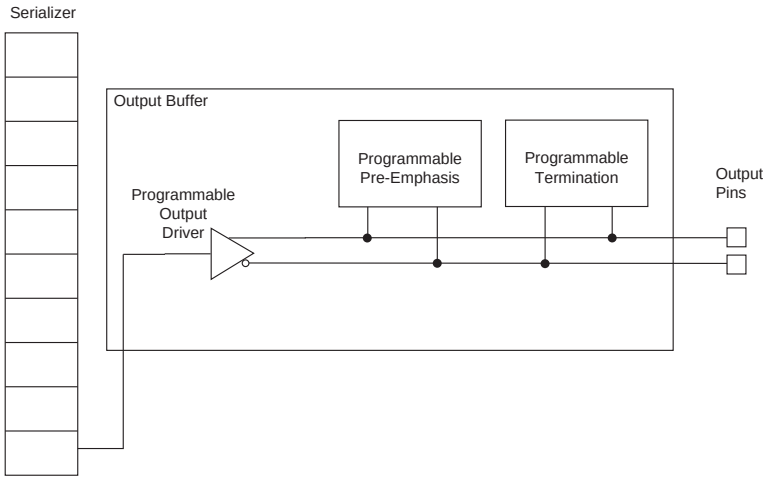
This section lists the Stratix II GX device features.

- Main device features:
  - TriMatrix memory consisting of three RAM block sizes to implement true dual-port memory and first-in first-out (FIFO) buffers with performance up to 550 MHz
  - Up to 16 global clock networks with up to 32 regional clock networks per device region
  - High-speed DSP blocks provide dedicated implementation of multipliers (at up to 450 MHz), multiply-accumulate functions, and finite impulse response (FIR) filters
  - Up to four enhanced PLLs per device provide spread spectrum, programmable bandwidth, clock switch-over, real-time PLL reconfiguration, and advanced multiplication and phase shifting
  - Support for numerous single-ended and differential I/O standards
  - High-speed source-synchronous differential I/O support on up to 71 channels
  - Support for source-synchronous bus standards, including SPI-4 Phase 2 (POS-PHY Level 4), SFI-4.1, XSBI, UTOPIA IV, NPSI, and CSIX-L1
  - Support for high-speed external memory, including quad data rate (QDR and QDRII) SRAM, double data rate (DDR and DDR2) SDRAM, and single data rate (SDR) SDRAM

Refer to the *Stratix II GX Transceiver Architecture Overview* chapter in volume 2 of the *Stratix II GX Handbook*.

The output buffer, as shown in Figure 2–8, is directly driven by the high-speed data serializer and consists of a programmable output driver, a programmable pre-emphasis circuit, a programmable termination, and a programmable V_{CM}.

Figure 2–8. Output Buffer



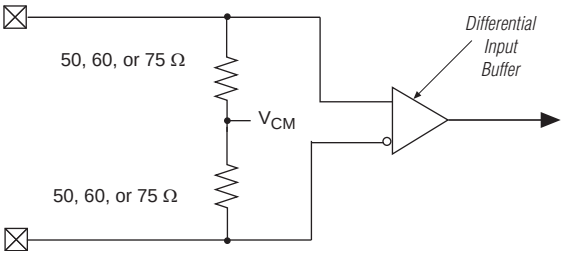
Programmable Output Driver

The programmable output driver can be set to drive out differentially 200 to 1,400 mV. The differential output voltage (V_{OD}) can be changed dynamically, or statically set by using the ALT2GXB megafunction or through I/O pins.

The output driver may be programmed with four different differential termination values:

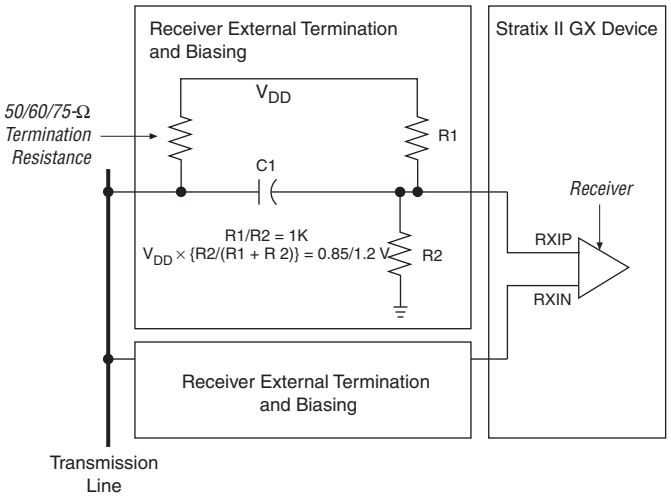
- 100 Ω
- 120 Ω
- 150 Ω
- External termination

Figure 2–13. Programmable Receiver Termination



If a design uses external termination, the receiver must be externally terminated and biased to 0.85 V or 1.2 V. Figure 2–14 shows an example of an external termination and biasing circuit.

Figure 2–14. External Termination and Biasing Circuit



Programmable Equalizer

The Stratix II GX receivers provide a programmable receive equalization feature to compensate the effects of channel attenuation for high-speed signaling. PCB traces carrying these high-speed signals have low-pass filter characteristics. The impedance mismatch boundaries can also cause signal degradation. The equalization in the receiver diminishes the lossy attenuation effects of the PCB at high frequencies.

Transceiver Clocking

Each Stratix II GX device transceiver block contains two transmitter PLLs and four receiver PLLs. These PLLs can be driven by either of the two reference clocks per transceiver block. These REFCLK signals can drive all global clocks, transmitter PLL inputs, and all receiver PLL inputs. Subsequently, the transmitter PLL output can only drive global clock lines and the receiver PLL reference clock port. Only one of the two reference clocks in a quad can drive the Inter Quad (I/Q) lines to clock the PLLs in the other quads.

Figure 2–29 shows the inter-transceiver line connections as well as the global clock connections for the EP2SGX130 device.

Modes of Operation

The adder, subtractor, and accumulate functions of a DSP block have four modes of operation:

- Simple multiplier
- Multiply-accumulator
- Two-multipliers adder
- Four-multipliers adder

Table 2–22 shows the different number of multipliers possible in each DSP block mode according to size. These modes allow the DSP blocks to implement numerous applications for DSP including FFTs, complex FIR, FIR, 2D FIR filters, equalizers, IIR, correlators, matrix multiplication, and many other functions. The DSP blocks also support mixed modes and mixed multiplier sizes in the same block. For example, half of one DSP block can implement one 18 × 18-bit multiplier in multiply-accumulator mode, while the other half of the DSP block implements four 9 × 9-bit multipliers in simple multiplier mode.

Table 2–22. Multiplier Size and Configurations per DSP Block

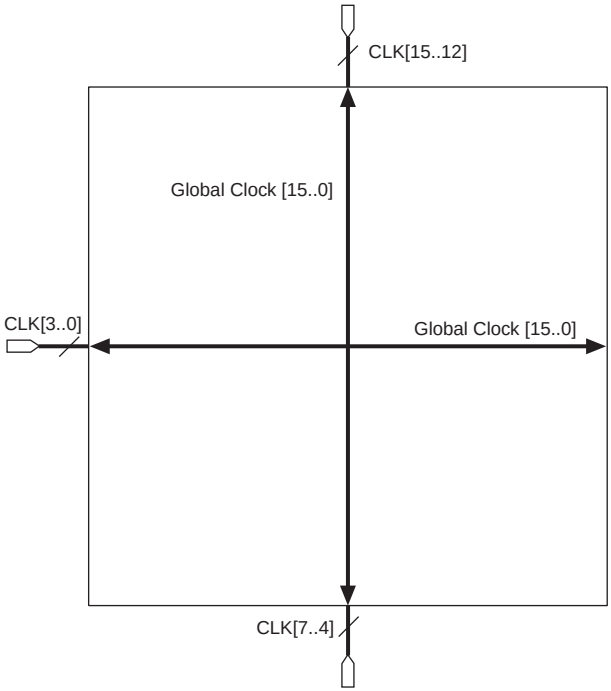
DSP Block Mode	9 × 9	18 × 18	36 × 36
Multiplier	Eight multipliers with eight product outputs	Four multipliers with four product outputs	One multiplier with one product output
Multiply-accumulator	—	Two 52-bit multiply-accumulate blocks	—
Two-multipliers adder	Four two-multiplier adder (two 9 × 9 complex multiply)	Two two-multiplier adder (one 18 × 18 complex multiply)	—
Four-multipliers adder	Two four-multiplier adder	One four-multiplier adder	—

DSP Block Interface

The Stratix II GX device DSP block input registers can generate a shift register that can cascade down in the same DSP block column. Dedicated connections between DSP blocks provide fast connections between the shift register inputs to cascade the shift register chains. You can cascade registers within multiple DSP blocks for 9 × 9- or 18 × 18-bit FIR filters larger than four taps, with additional adder stages implemented in ALMs. If the DSP block is configured as 36 × 36 bits, the adder, subtractor, or accumulator stages are implemented in ALMs. Each DSP block can route the shift register chain out of the block to cascade multiple columns of DSP blocks.

generated global clocks and asynchronous clears, clock enables, or other control signals with large fanout. Figure 2–61 shows the 12 dedicated CLK pins driving global clock networks.

Figure 2–61. Global Clocking

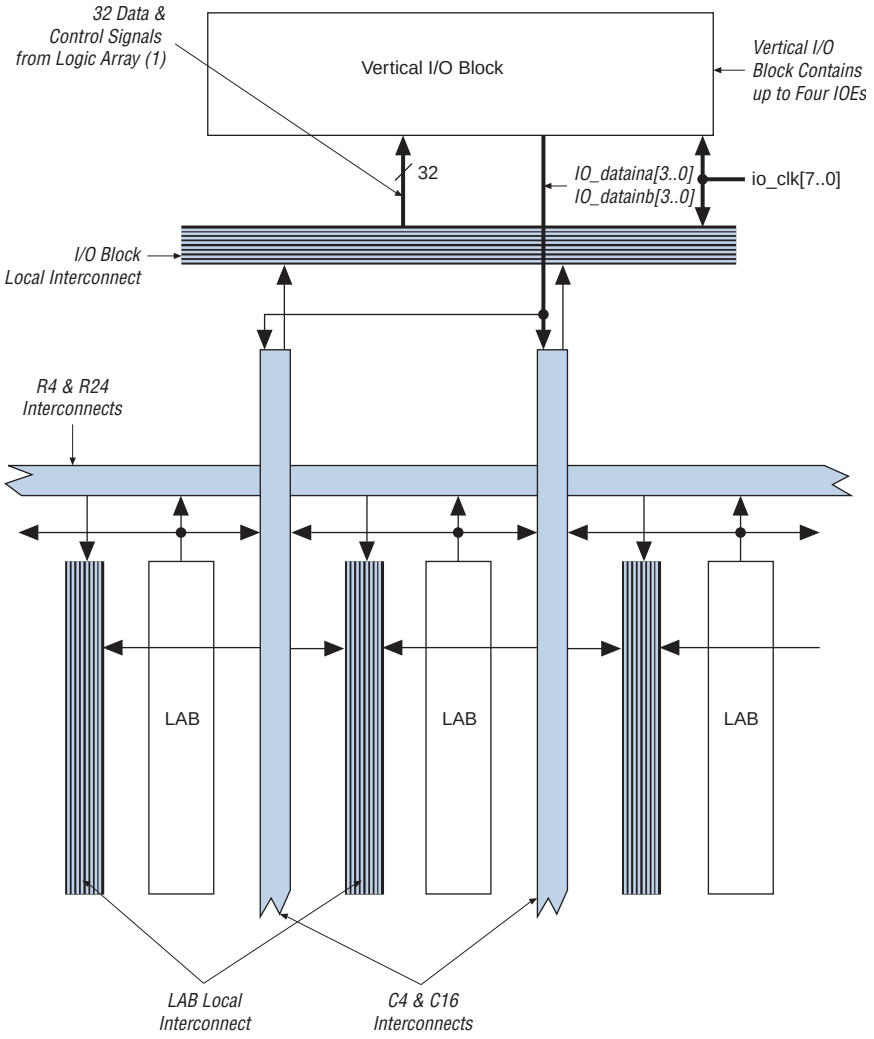


Regional Clock Network

There are eight regional clock networks (RCLK[7..0]) in each quadrant of the Stratix II GX device that are driven by the dedicated CLK[15..12] and CLK[7..0] input pins, by PLL outputs, or by internal logic. The regional clock networks provide the lowest clock delay and skew for logic contained in a single quadrant. The CLK pins symmetrically drive the RCLK networks in a particular quadrant, as shown in Figure 2–62.

Figure 2–78 shows how a column I/O block connects to the logic array.

Figure 2–78. Column I/O Block Connection to the Interconnect



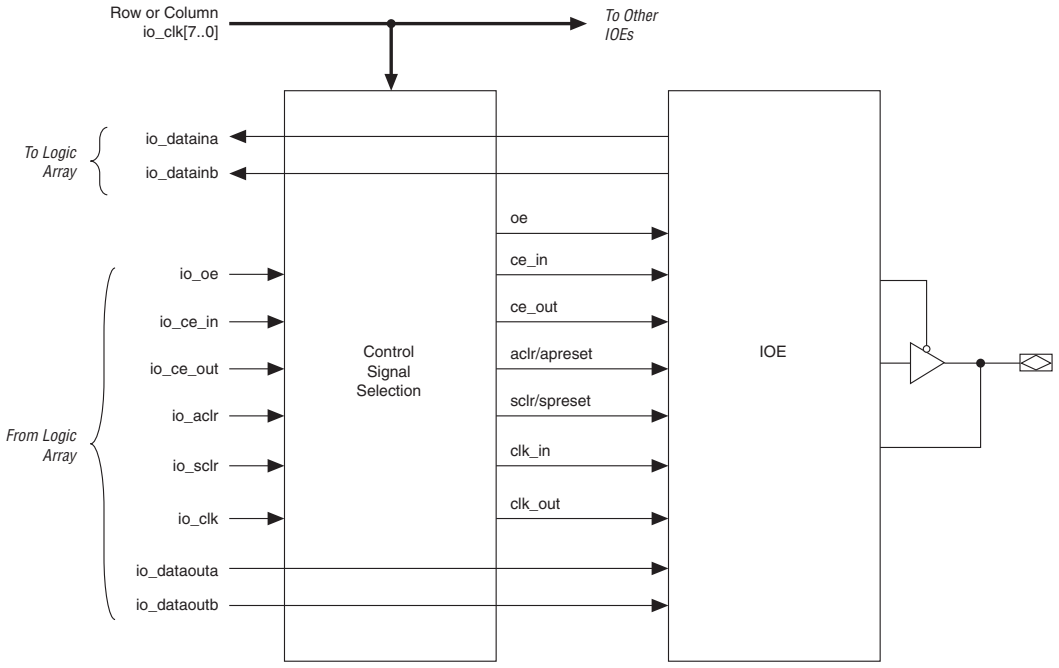
Note to Figure 2–78:

(1) The 32 data and control signals consist of eight data out lines: four lines each for DDR applications `io_dataouta[3..0]` and `io_dataoutb[3..0]`, four output enables `io_oe[3..0]`, four input clock enables `io_ce_in[3..0]`, four output clock enables `io_ce_out[3..0]`, four clocks `io_clk[3..0]`, four asynchronous clear and preset signals `io_aclr/apreset[3..0]`, and four synchronous clear and preset signals `io_sclr/spreset[3..0]`.

There are 32 control and data signals that feed each row or column I/O block. These control and data signals are driven from the logic array. The row or column IOE clocks, `io_clk[7..0]`, provide a dedicated routing resource for low-skew, high-speed clocks. I/O clocks are generated from global or regional clocks. Refer to "PLLs and Clock Networks" on page 2–89 for more information.

Figure 2–79 illustrates the signal paths through the I/O block.

Figure 2–79. Signal Path Through the I/O Block



Each IOE contains its own control signal selection for the following control signals: `oe`, `ce_in`, `ce_out`, `aclr/apreset`, `sclr/spreset`, `clk_in`, and `clk_out`. Figure 2–80 illustrates the control signal selection.

Table 2–34. On-Chip Termination Support by I/O Banks (Part 2 of 2)

On-Chip Termination Support	I/O Standard Support	Top and Bottom Banks (3, 4, 7, 8)	Left Bank (1, 2)
Series termination with calibration	3.3-V LVTTL	✓	—
	3.3-V LVCMOS	✓	—
	2.5-V LVTTL	✓	—
	2.5-V LVCMOS	✓	—
	1.8-V LVTTL	✓	—
	1.8-V LVCMOS	✓	—
	1.5-V LVTTL	✓	—
	1.5-V LVCMOS	✓	—
	SSTL-2 class I and II	✓	—
	SSTL-18 class I and II	✓	—
	1.8-V HSTL class I	✓	—
	1.8-V HSTL class II	✓	—
	1.5-V HSTL class I	✓	—
	1.2-V HSTL	✓	—
Differential termination *(1)*	LVDS	—	✓
	HyperTransport technology	—	✓

Note to Table 2–34:

(1) Clock pins `CLK1` and `CLK3`, and pins `FPLL[7..8]CLK` do not support differential on-chip termination. Clock pins `CLK0` and `CLK2`, do support differential on-chip termination. Clock pins in the top and bottom banks (`CLK[4..7, 12..15]`) do not support differential on-chip termination.

Differential On-Chip Termination

Stratix II GX devices support internal differential termination with a nominal resistance value of 100 for LVDS input receiver buffers. LVPECL input signals (supported on clock pins only) require an external termination resistor. Differential on-chip termination is supported across the full range of supported differential data rates, as shown in the *High-Speed I/O Specifications* section of the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II GX Device Handbook*.

For more information on differential on-chip termination, refer to the *High-Speed Differential I/O Interfaces with DPA in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook*.

Table 2–42. Document Revision History (Part 3 of 6)

Date and Document Version	Changes Made	Summary of Changes
	Moved the "Transmit State Machine" section to after the "8B/10B Encoder" section.	
	Moved the "PCI Express Receiver Detect" and "PCI Express Electric Idles (or Individual Transmitter Tri-State)" sections to after the "Transmit Buffer" section.	
	Moved the "Dynamic Reconfiguration" section to the "Other Transceiver Features" section.	
	Moved the "Calibration Block", "Receiver PLL & CRU", and "Deserializer (Serial-to-Parallel Converter)" sections to the "Receiver Path" section.	
	Moved the "8B/10B Decoder" and "Receiver State Machine" sections to after the "Rate Matcher" section.	
	Moved the "Byte Ordering Block" section to after the "Byte Deserializer" section.	
	Updated the Clocking diagrams.	
	Added the "Clock Resource for PLD-Transceiver Interface" section.	
	Added the "On-Chip Parallel Termination with Calibration" section to the "On-Chip Termination" section.	
	Updated: • Table 2–2. • Table 2–10 • Table 2–14. • Table 2–3. • Table 2–5. • Table 2–8. • Table 2–13 • Table 2–18 • Table 2–19 • Table 2–29.	
	Updated Figures 2–3, 2–9, 2–24, 2–25, 2–28, 2–29, 2–60, 2–62.	
	Change 622 Mbps to 600 Mbps throughout the chapter.	

Table 3–5 shows the specifications for bias voltage and current of the Stratix II GX temperature sensing diode.

Table 3–5. Temperature-Sensing Diode Electrical Characteristics

Parameter	Minimum	Typical	Maximum	Unit
IBIAS high	80	100	120	µA
IBIAS low	8	10	12	µA
VBP - VBN	0.3		0.9	V
VBN		0.7		V
Series resistance			3	Ω

The temperature-sensing diode works for the entire operating range shown in Figure 3–2.

Figure 3–2. Temperature Versus Temperature-Sensing Diode Voltage

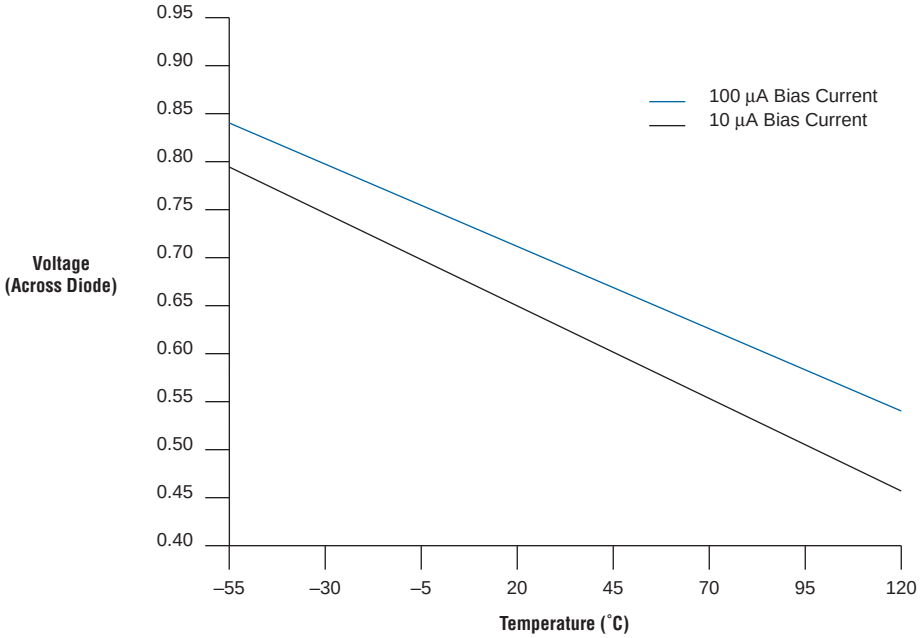


Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 9 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
HiGig Receiver Jitter Tolerance *(13)*											
Deterministic Jitter Tolerance (peak-to-peak)	Data Rate = 3.75 Gbps REFCLK = 187.5 MHz Pattern = CJPAT No Equalization DC Gain = 3 dB		> 0.37			-			-		UI
Combined Deterministic and Random Jitter Tolerance (peak-to-peak)	Data Rate = 3.75 Gbps REFCLK = 187.5 MHz Pattern = CJPAT No Equalization DC Gain = 3 dB		> 0.65			-			-		UI
	Jitter Frequency = 22.1 KHz Data Rate = 3.75 Gbps REFCLK = 187.5 MHz Pattern = CJPAT No Equalization DC Gain = 3 dB		> 8.5			-			-		UI

Table 4–22. PCS Latency (Part 2 of 3) Note (1)

Functional Mode	Configuration	Receiver PCS Latency									
		Word Aligner	Deskew FIFO	Rate Matcher (3)	8B/10B Decoder	Receiver State Machine	Byte De-serializer	Byte Order	Receiver Phase Comp FIFO	Receiver PIPE	Sum (2)
BASIC Single Width	8/10-bit channel width; with Rate Matcher	4-5	-	11-13	1	-	1	1	1-2	1	19-23
	8/10-bit channel width; without Rate Matcher	4-5	-	-	1	-	1	1	1-2	-	8-10
	16/20-bit channel width; with Rate Matcher	2-2.5	-	5.5-6.5	0.5	-	1	1	1-2	-	11-14
	16/20-bit channel width; without Rate Matcher	2-2.5	-	-	0.5	-	1	1	1-2	-	6-7

Table 4–55 shows the Stratix II GX performance for some common designs. All performance values were obtained with the Quartus II software compilation of LPM or MegaCore functions for FIR and FFT designs.

Table 4–55. Stratix II GX Performance Notes (Part 1 of 3) *Note (1)*

Applications		Resources Used			Performance				
		ALUTs	TriMatrix Memory Blocks	DSP Blocks	-3 Speed Grade (2)	-3 Speed Grade (3)	-4 Speed Grade	-5 Speed Grade	Units
LE	16-to-1 multiplexer (4)	21	0	0	657.03	620.73	589.62	477.09	MHz
	32-to-1 multiplexer (4)	38	0	0	534.75	517.33	472.81	369.27	MHz
	16-bit counter	16	0	0	568.18	539.66	507.61	422.47	MHz
	64-bit counter	64	0	0	242.54	231.0	217.77	180.31	MHz
TriMatrix Memory M512 block	Simple dual-port RAM 32 x 18bit	0	1	0	500.0	476.19	447.22	373.13	MHz
	FIFO 32 x 18 bit	22	1	0	500.00	476.19	460.82	373.13	MHz
TriMatrix Memory M4K block	Simple dual-port RAM 128 x 36bit	0	1	0	540.54	515.46	483.09	401.6	MHz
	True dual-port RAM 128 x 18bit	0	1	0	540.54	515.46	483.09	401.6	MHz
	FIFO 128 x 36 bit	22	1	0	524.10	500.25	466.41	381.38	MHz

Table 4–59. M512 Block Internal Timing Microparameters (Part 1 of 2)

Symbol	Parameter	-3 Speed Grade (2)		-3 Speed Grade (3)		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{M512RC}	Synchronous read cycle time	2089	2318	2089	2433	2089	2587	2089	3104	ps
$t_{M512WERESU}$	Write or read enable setup time before clock	22		23		24		29		ps
$t_{M512WEREH}$	Write or read enable hold time after clock	203		213		226		272		ps
$t_{M512DATASU}$	Data setup time before clock	22		23		24		29		ps
$t_{M512DATAH}$	Data hold time after clock	203		213		226		272		ps
$t_{M512WADDRSU}$	Write address setup time before clock	22		23		24		29		ps
$t_{M512WADDRH}$	Write address hold time after clock	203		213		226		272		ps
$t_{M512RADDRSU}$	Read address setup time before clock	22		23		24		29		ps
$t_{M512RADDRH}$	Read address hold time after clock	203		213		226		272		ps
$t_{M512DATACO1}$	Clock-to-output delay when using output registers	298	478	298	501	298	533	298	640	ps
$t_{M512DATACO2}$	Clock-to-output delay without output registers	2102	2345	2102	2461	2102	2616	2102	3141	ps
$t_{M512CLKL}$	Minimum clock low time	1315		1380		1468		1762		ps
$t_{M512CLKH}$	Minimum clock high time	1315		1380		1468		1762		ps

Table 4–68. EP2SGX60 Row Pins Global Clock Timing Parameters

Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.494	1.508	2.582	2.875	3.441	ns
t_{COUT}	1.499	1.513	2.578	2.871	3.436	ns
t_{PLLCIN}	-0.183	-0.168	0.116	0.122	0.135	ns
$t_{PLLCOUT}$	-0.178	-0.163	0.112	0.118	0.13	ns

Table 4–69. EP2SGX60 Column Pins Regional Clock Timing Parameters

Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.577	1.591	2.736	3.048	3.648	ns
t_{COUT}	1.412	1.426	2.740	3.052	3.653	ns
t_{PLLCIN}	0.065	0.08	0.334	0.361	0.423	ns
$t_{PLLCOUT}$	-0.1	-0.085	0.334	0.361	0.423	ns

Table 4–70. EP2SGX60 Row Pins Regional Clock Timing Parameters

Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.342	1.355	2.716	3.024	3.622	ns
t_{COUT}	1.347	1.360	2.716	3.024	3.622	ns
t_{PLLCIN}	-0.18	-0.166	0.326	0.352	0.412	ns
$t_{PLLCOUT}$	-0.175	-0.161	0.334	0.361	0.423	ns

Table 4–87. Stratix II GX I/O Output Delay for Row Pins (Part 4 of 4)								
I/O Standard	**Drive Strength**	**Parameter**	**Fast Corner Industrial/ Commercial**	**-3 Speed Grade** *(3)*	**-3 Speed Grade** *(4)*	**-4 Speed Grade**	**-5 Speed Grade**	**Unit**
Differential SSTL-18 Class I	4 mA	t_{OP}	1038	1709	1793	1906	2046	ps
		t_{DIP}	995	1654	1736	1846	1973	ps
	6 mA	t_{OP}	1042	1648	1729	1838	1975	ps
		t_{DIP}	999	1593	1672	1778	1902	ps
	8 mA	t_{OP}	1018	1633	1713	1821	1958	ps
		t_{DIP}	975	1578	1656	1761	1885	ps
	10 mA	t_{OP}	1021	1615	1694	1801	1937	ps
		t_{DIP}	978	1560	1637	1741	1864	ps
LVDS *(2)*	-	t_{OP}	1067	1723	1808	1922	2089	ps
		t_{DIP}	1024	1668	1751	1862	2016	ps
HyperTransport	-	t_{OP}	1053	1723	1808	1922	2089	ps
		t_{DIP}	1010	1668	1751	1862	2016	ps

(1) This is the default setting in the Quartus II software.
(2) The parameters are only available on the left side of the device.
(3) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
(4) This column refers to –3 speed grades for EP2SGX130 devices.

Maximum Input and Output Clock Toggle Rate

Maximum clock toggle rate is defined as the maximum frequency achievable for a clock type signal at an I/O pin. The I/O pin can be a regular I/O pin or a dedicated clock I/O pin.

The maximum clock toggle rate is different from the maximum data bit rate. If the maximum clock toggle rate on a regular I/O pin is 300 MHz, the maximum data bit rate for dual data rate (DDR) could be potentially as high as 600 Mbps on the same I/O pin.

Tables 4–88 through 4–90 specify the maximum input clock toggle rates. Tables 4–91 through 4–96 specify the maximum output clock toggle rates at 0 pF load. Table 4–97 specifies the derating factors for the output clock toggle rate for a non 0 pF load.

Table 4–91. Stratix II GX Maximum Output Clock Rate for Column Pins (Part 3 of 3)					
I/O Standard	**Drive Strength**	**-3 Speed Grade**	**-4 Speed Grade**	**-5 Speed Grade**	**Unit**
Differential SSTL-18 Class I	4 mA	200	150	150	MHz
	6 mA	350	250	200	MHz
	8 mA	450	300	300	MHz
	10 mA	500	400	400	MHz
	12 mA	700	550	400	MHz
Differential SSTL-18 Class II	8 mA	200	200	150	MHz
	16 mA	400	350	350	MHz
	18 mA	450	400	400	MHz
	20 mA	550	500	450	MHz
1.8-V HSTL differential Class I	4 mA	300	300	300	MHz
	6 mA	500	450	450	MHz
	8 mA	650	600	600	MHz
	10 mA	700	650	600	MHz
	12 mA	700	700	650	MHz
1.8-V HSTL differential Class II	16 mA	500	500	450	MHz
	18 mA	550	500	500	MHz
	20 mA	650	550	550	MHz
1.5-V HSTL differential Class I	4 mA	350	300	300	MHz
	6 mA	500	500	450	MHz
	8 mA	700	650	600	MHz
	10 mA	700	700	650	MHz
	12 mA	700	700	700	MHz
1.5-V HSTL differential Class II	16 mA	600	600	550	MHz
	18 mA	650	600	600	MHz
	20 mA	700	650	600	MHz

(1) This is the default setting in the Quartus II software.

Table 4–93. Stratix II GX Maximum Output Clock Rate for Dedicated Clock Pins (Part 4 of 4)					
I/O Standard	Drive Strength	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
1.8-V differential Class II	16 mA	500	500	450	MHz
	18 mA	550	500	500	MHz
	20 mA	550	550	550	MHz
1.5-V differential Class I	4 mA	350	300	300	MHz
	6 mA	500	500	450	MHz
	8 mA	700	650	600	MHz
	10 mA	700	700	650	MHz
	12 mA	700	700	700	MHz
1.5-V differential Class II	16 mA	600	600	550	MHz
	18 mA	650	600	600	MHz
	20 mA	700	650	600	MHz
HyperTransport	-	300	250	125	MHz
LVPECL	-	450	400	300	MHz

(1) This is the default setting in Quartus II software.

Table 4–94 shows the maximum output clock toggle rate for Stratix II GX device series-terminated column pins.

Table 4–94. Stratix II GX Maximum Output Clock Rate for Column Pins (Series Termination) (Part 1 of 2)					
I/O Standard	Drive Strength	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
LVTTL	OCT_25_OHMS	400	400	350	MHz
	OCT_50_OHMS	400	400	350	MHz
LVCMOS	OCT_25_OHMS	350	350	300	MHz
	OCT_50_OHMS	350	350	300	MHz
2.5 V	OCT_25_OHMS	350	350	300	MHz
	OCT_50_OHMS	350	350	300	MHz
1.8 V	OCT_25_OHMS	700	550	450	MHz
	OCT_50_OHMS	700	550	450	MHz
1.5 V	OCT_50_OHMS	550	450	400	MHz
SSTL-2 Class I	OCT_50_OHMS	600	500	500	MHz
SSTL-2 Class II	OCT_25_OHMS	600	550	500	MHz

Table 4–105. Maximum DCD for DDIO Output on Column I/O Pins With PLL in the Clock Path (Part 2 of 2)			
Maximum DCD (ps) for Column DDIO Output I/O Standard	Stratix II GX Devices (PLL Output Feeding DDIO)		Unit
	-3 Device	-4 and -5 Device	
1.2-V HSTL	155	155	ps
LVPECL	180	180	ps

High-Speed I/O Specifications

Table 4–106 provides high-speed timing specifications definitions.

Table 4–106. High-Speed Timing Specifications and Definitions	
High-Speed Timing Specifications	Definitions
t_C	High-speed receiver/transmitter input and output clock period.
f_{HSCLK}	High-speed receiver/transmitter input and output clock frequency.
J	Deserialization factor (width of parallel data bus).
W	PLL multiplication factor.
t_{RISE}	Low-to-high transmission time.
t_{FALL}	High-to-low transmission time.
Timing unit interval (TUI)	The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency × Multiplication Factor) = t_C/w).
f_{IN}	Fast PLL input clock frequency
f_{HSDR}	Maximum/minimum LVDS data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
$f_{HSDRDPA}$	Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.
Channel-to-channel skew (TCCS)	The timing difference between the fastest and the slowest output edges including t_{CO} variation and clock skew across channels driven by the same fast PLL. The clock is included in the TCCS measurement.
Sampling window (SW)	The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window.
Input jitter	Peak-to-peak input jitter on high-speed PLLs.
Output jitter	Peak-to-peak output jitter on high-speed PLLs.
t_{DUTY}	Duty cycle on high-speed transmitter output clock.
t_{LOCK}	Lock time for high-speed transmitter and receiver PLLs.