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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	4548
Number of Logic Elements/Cells	90960
Total RAM Bits	4520448
Number of I/O	650
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1508-BBGA, FCBGA
Supplier Device Package	1508-FBGA, FC (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2sgx90ff1508i4

- Support for multiple intellectual property megafunctions from Altera® MegaCore® functions and Altera Megafunction Partners Program (AMPP^{SM}) megafunctions
- Support for design security using configuration bitstream encryption
- Support for remote configuration updates

- Transceiver block features:
  - High-speed serial transceiver channels with clock data recovery (CDR) provide 600-megabits per second (Mbps) to 6.375-Gbps full-duplex transceiver operation per channel
  - Devices available with 4, 8, 12, 16, or 20 high-speed serial transceiver channels providing up to 255 Gbps of serial bandwidth (full duplex)
  - Dynamically programmable voltage output differential (V_{OD}) and pre-emphasis settings for improved signal integrity
  - Support for CDR-based serial protocols, including PCI Express, Gigabit Ethernet, SDI, Altera's SerialLite II, XAUI, CEI-6G, CPRI, Serial RapidIO, SONET/SDH
  - Dynamic reconfiguration of transceiver channels to switch between multiple protocols and data rates
  - Individual transmitter and receiver channel power-down capability for reduced power consumption during non-operation
  - Adaptive equalization (AEQ) capability at the receiver to compensate for changing link characteristics
  - Selectable on-chip termination resistors (100, 120, or 150 Ω) for improved signal integrity on a variety of transmission media
  - Programmable transceiver-to-FPGA interface with support for 8-, 10-, 16-, 20-, 32-, and 40-bit wide data transfer
  - 1.2- and 1.5-V pseudo current mode logic (PCML) for 600 Mbps to 6.375 Gbps (AC coupling)
  - Receiver indicator for loss of signal (available only in PIPE mode)
  - Built-in self test (BIST)
  - Hot socketing for hot plug-in or hot swap and power sequencing support without the use of external devices
  - Rate matcher, byte-reordering, bit-reordering, pattern detector, and word aligner support programmable patterns
  - Dedicated circuitry that is compliant with PIPE, XAUI, and GIGE
  - Built-in byte ordering so that a frame or packet always starts in a known byte lane
  - Transmitters with two PLL inputs for each transceiver block with independent clock dividers to provide varying clock rates on each of its transmitters

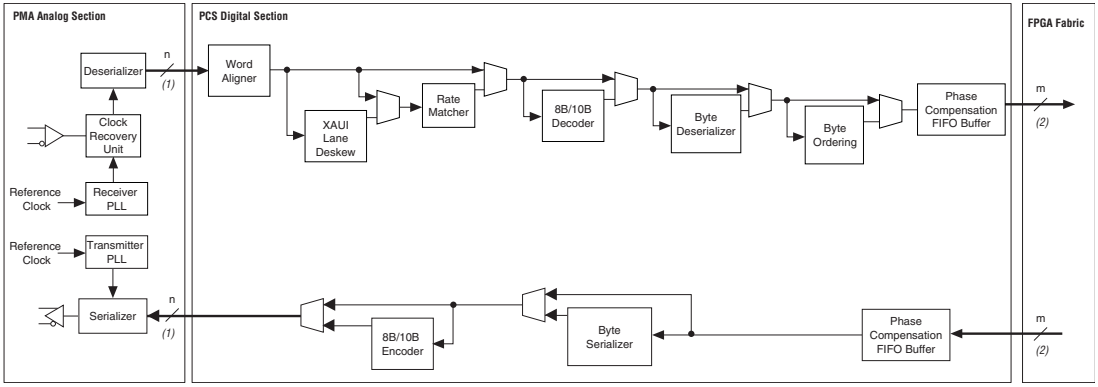
2. Stratix II GX Architecture

SIIGX51003-2.2

Transceivers

Stratix® II GX devices incorporate dedicated embedded circuitry on the right side of the device, which contains up to 20 high-speed 6.375-Gbps serial transceiver channels. Each Stratix II GX transceiver block contains four full-duplex channels and supporting logic to transmit and receive high-speed serial data streams. The transceivers deliver bidirectional point-to-point data transmissions, with up to 51 Gbps (6.375 Gbps per channel) of full-duplex data transmission per transceiver block. Figure 2–1 shows the function blocks that make up a transceiver channel within the Stratix II GX device.

Figure 2–1. Stratix II GX Transceiver Block Diagram



Notes to Figure 2–1:

(1) *n* represents the number of bits in each word that need to be serialized by the transmitter portion of the PMA or have been deserialized by the receiver portion of the PMA. *n* = 8, 10, 16, or 20.

(2) *m* represents the number of bits in the word that pass between the FPGA logic and the PCS portion of the transceiver. *m* = 8, 10, 16, 20, 32, or 40.

Transceivers within each block are independent and have their own set of dividers. Therefore, each transceiver can operate at different frequencies. Each block can select from two reference clocks to provide two clock domains that each transceiver can select from.

Table 2–13. Available Clocking Connections for Transceivers in 2SGX60E

Region	Clock Resource		Transceiver		
	Global Clock	Regional Clock	Bank 13 8 Clock I/O	Bank 14 8 Clock I/O	Bank 15 8 Clock I/O
Region0 8 LRIO clock	✓	RCLK 20-27	✓		
Region1 8 LRIO clock	✓	RCLK 20-27	✓	✓	
Region2 8 LRIO clock	✓	RCLK 12-19		✓	✓
Region3 8 LRIO clock	✓	RCLK 12-19			✓

Table 2–14. Available Clocking Connections for Transceivers in 2SGX90F

Region	Clock Resource		Transceiver			
	Global Clock	Regional Clock	Bank 13 8 Clock I/O	Bank 14 8 Clock I/O	Bank 15 8 clock I/O	Bank 16 8 Clock I/O
Region0 8 LRIO clock	✓	RCLK 20-27	✓			
Region1 8 LRIO clock	✓	RCLK 20-27		✓		
Region2 8 LRIO clock	✓	RCLK 12-19			✓	
Region3 8 LRIO clock	✓	RCLK 12-19				✓

M512 RAM blocks can have different clocks on its inputs and outputs. The wren, datain, and write address registers are all clocked together from one of the two clocks feeding the block. The read address, rden, and output registers can be clocked by either of the two clocks driving the block, allowing the RAM block to operate in read and write or input and output clock modes. Only the output register can be bypassed. The six labclk signals or local interconnect can drive the inclock, outclock, wren, rden, and outclr signals. Because of the advanced interconnect between the LAB and M512 RAM blocks, ALMs can also control the wren and rden signals and the RAM clock, clock enable, and asynchronous clear signals. Figure 2–49 shows the M512 RAM block control signal generation logic.

Figure 2–49. M512 RAM Block Control Signals

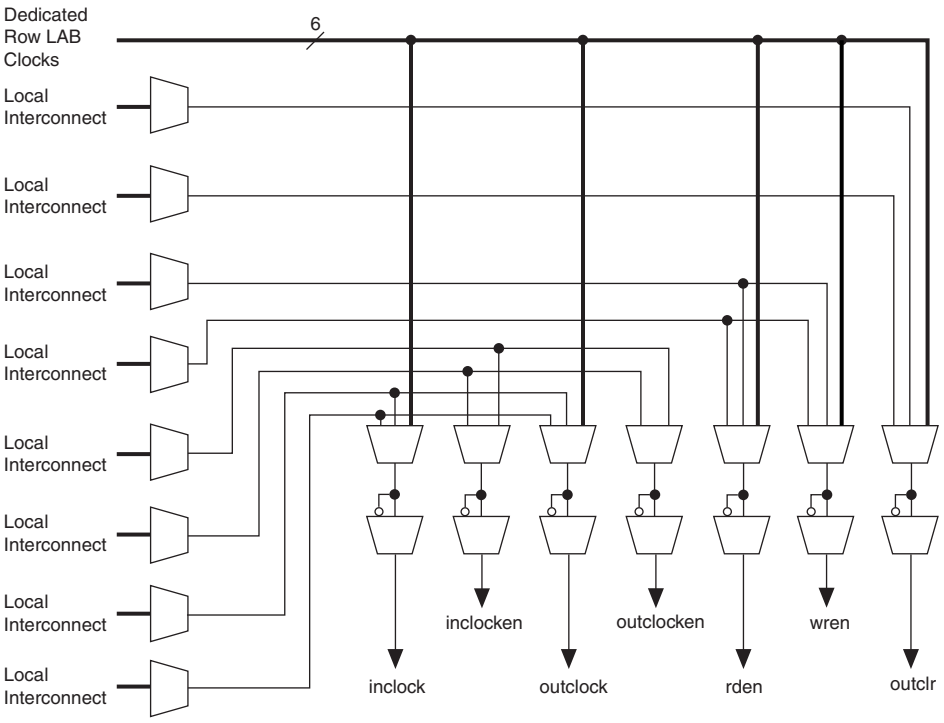
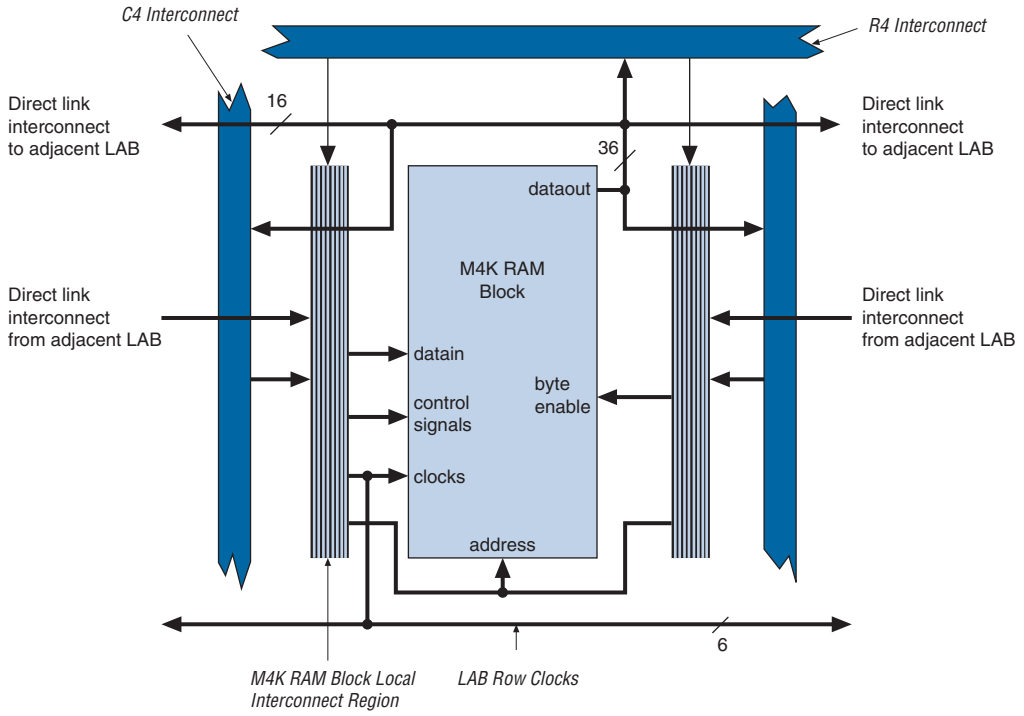


Figure 2–52. M4K RAM Block LAB Row Interface



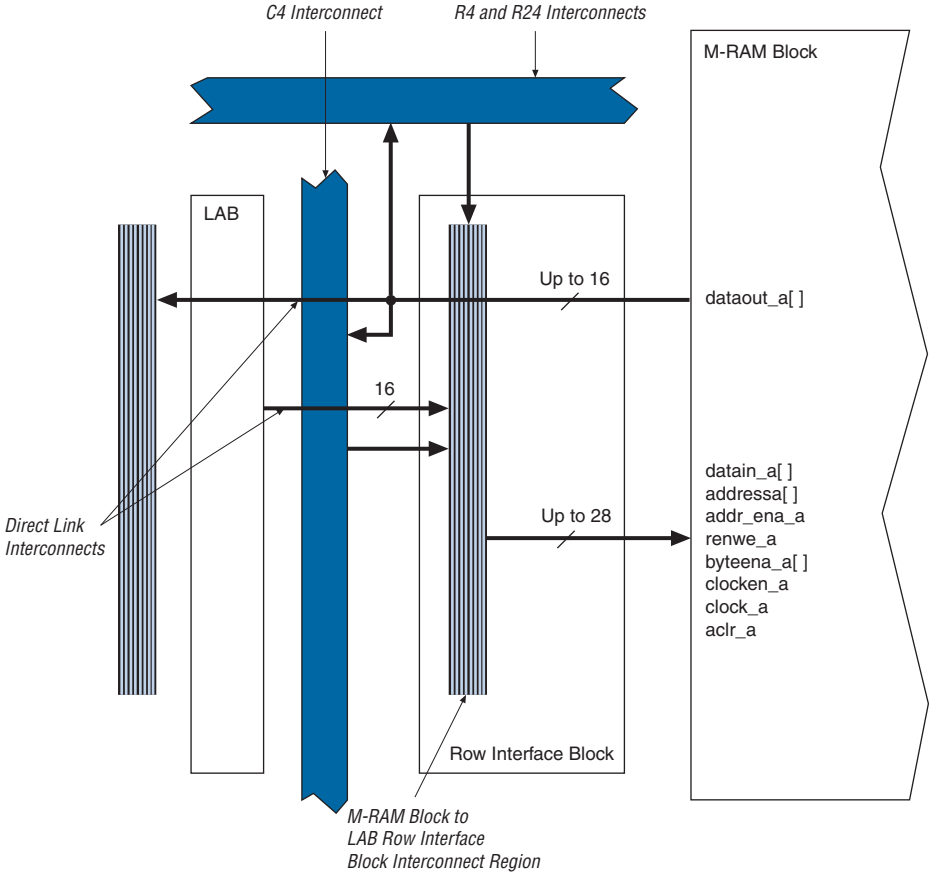
M-RAM Block

The largest TriMatrix memory block, the M-RAM block, is useful for applications where a large volume of data must be stored on-chip. Each block contains 589,824 RAM bits (including parity bits). The M-RAM block can be configured in the following modes:

- True dual-port RAM
- Simple dual-port RAM
- Single-port RAM
- FIFO

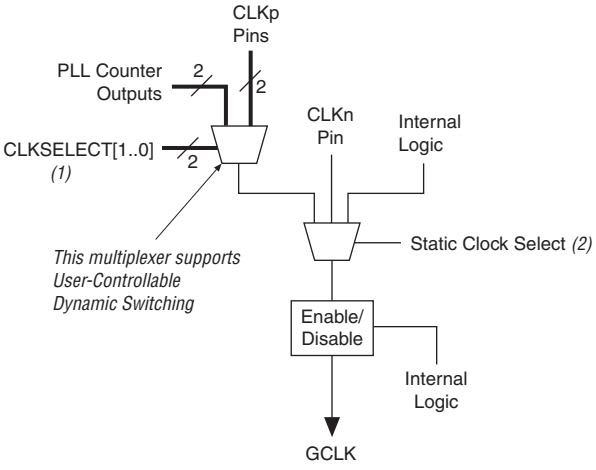
You cannot use an initialization file to initialize the contents of a M-RAM block. All M-RAM block contents power up to an undefined value. Only synchronous operation is supported in the M-RAM block, so all inputs are registered. Output registers can be bypassed.

Figure 2–56. M-RAM Row Unit Interface to Interconnect



Figures 2–67 through 2–69 show the clock control block for the global clock, regional clock, and PLL external clock output, respectively.

Figure 2–67. Global Clock Control Blocks

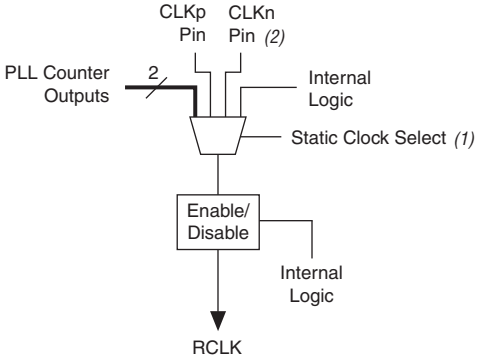


Notes to Figure 2–67:

(1) These clock select signals can be dynamically controlled through internal logic when the device is operating in user mode.

(2) These clock select signals can only be set through a configuration file (SRAM Object File [**.sof**] or Programmer Object File [**.pof**]) and cannot be dynamically controlled during user mode operation.

Figure 2–68. Regional Clock Control Blocks



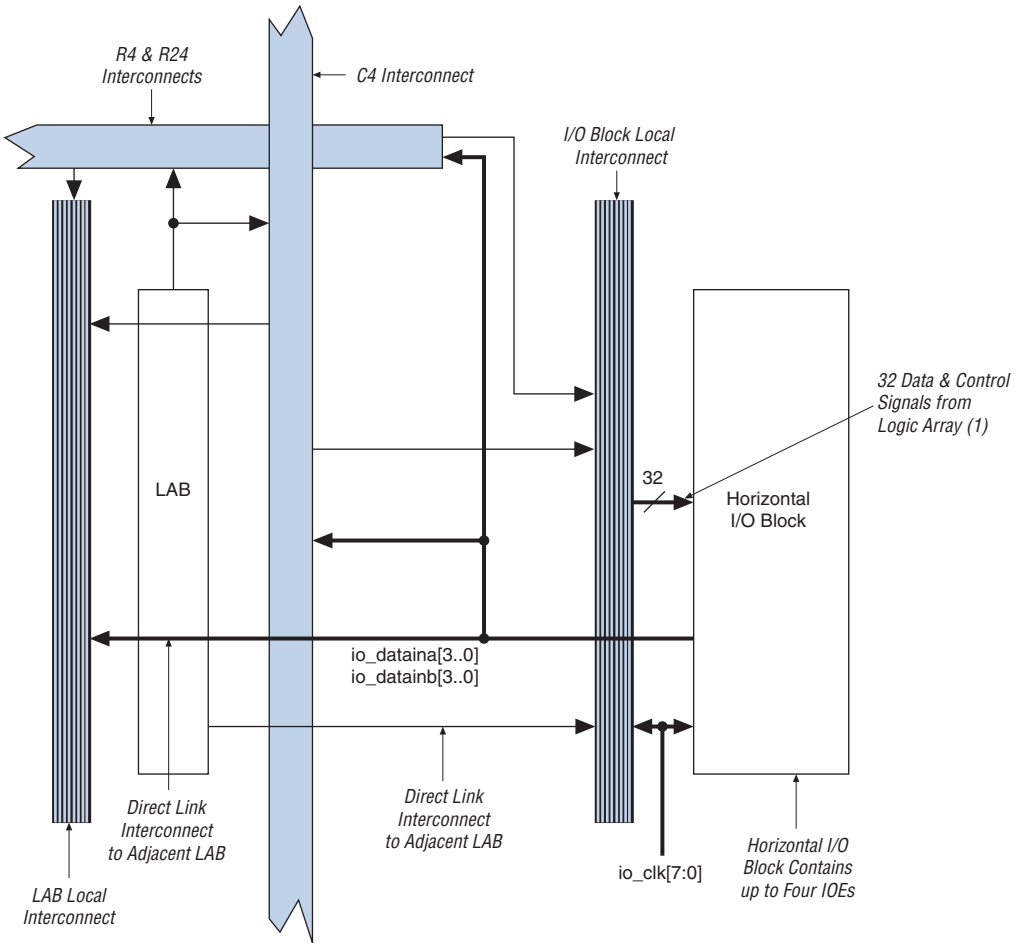
Notes to Figure 2–68:

(1) These clock select signals can only be set through a configuration file (**.sof** or **.pof**) and cannot be dynamically controlled during user mode operation.

(2) Only the `CLKn` pins on the top and bottom of the device feed to regional clock select.

Figure 2–77 shows how a row I/O block connects to the logic array.

Figure 2–77. Row I/O Block Connection to the Interconnect

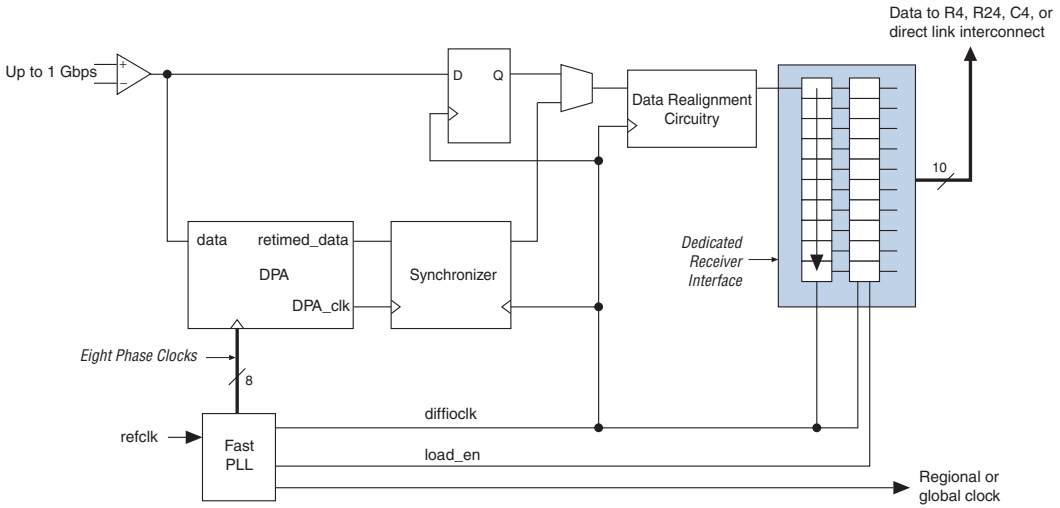


Note to Figure 2–77:

(1) The 32 data and control signals consist of eight data out lines: four lines each for DDR applications `io_dataouta[3..0]` and `io_dataoutb[3..0]`, four output enables `io_oe[3..0]`, four input clock enables `io_ce_in[3..0]`, four output clock enables `io_ce_out[3..0]`, four clocks `io_clk[3..0]`, four asynchronous clear and preset signals `io_aclr/apreset[3..0]`, and four synchronous clear and preset signals `io_sclr/spreset[3..0]`.

Figure 2–89 shows the block diagram of the Stratix II GX receiver channel.

Figure 2–89. Stratix II GX Receiver Channel



An external pin or global or regional clock can drive the fast PLLs, which can output up to three clocks: two multiplied high-speed clocks to drive the SERDES block and/or external pin, and a low-speed clock to drive the logic array. In addition, eight phase-shifted clocks from the VCO can feed to the DPA circuitry.

For more information on the fast PLL, see the *PLLs in Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Handbook*.

The eight phase-shifted clocks from the fast PLL feed to the DPA block. The DPA block selects the closest phase to the center of the serial data eye to sample the incoming data. This allows the source-synchronous circuitry to capture incoming data correctly regardless of the channel-to-channel or clock-to-channel skew. The DPA block locks to a phase closest to the serial data phase. The phase-aligned DPA clock is used to write the data into the synchronizer.

The synchronizer sits between the DPA block and the data realignment and SERDES circuitry. Since every channel utilizing the DPA block can have a different phase selected to sample the data, the synchronizer is needed to synchronize the data to the high-speed clock domain of the data realignment and the SERDES circuitry.

- *Stratix II Performance and Logic Efficiency Analysis White Paper*
- *TriMatrix Embedded Memory Blocks in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook*

Document Revision History

Table 2–42 shows the revision history for this chapter.

Table 2–42. Document Revision History (Part 1 of 6)

Date and Document Version	Changes Made	Summary of Changes
October 2007, v2.2	Updated: • "Programmable Pull-Up Resistor" • "Reverse Serial Pre-CDR Loopback" • "Receiver Input Buffer" • "Pattern Detection" • "Control and Status Signals" • "Individual Power Down and Reset for the Transmitter and Receiver"	
	Updated: • Figure 2–14 • Figure 2–26 • Figure 2–27 • Figure 2–86 (notes only) • Figure 2–87	
	Updated: • Table 2–4 • Table 2–7	
	Removed note from Table 2–31.	
	Removed Tables 2-2, 2-7, and 2-8.	
	Minor text edits.	
August 2007, v2.1	Added "Reverse Serial Pre-CDR Loopback" section.	
	Updated Table 2–2.	
	Added "Referenced Documents" section.	

3. Configuration & Testing

SIIGX51005-1.4

IEEE Std. 1149.1 JTAG Boundary-Scan Support

All Stratix® II GX devices provide Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry that complies with the IEEE Std. 1149.1. You can perform JTAG boundary-scan testing either before or after, but not during configuration. Stratix II GX devices can also use the JTAG port for configuration with the Quartus® II software or hardware using either Jam Files (**.jam**) or Jam Byte-Code Files (**.jbc**).

Stratix II GX devices support IOE I/O standard setting reconfiguration through the JTAG BST chain. The JTAG chain can update the I/O standard for all input and output pins any time before or during user mode through the `CONFIG_IO` instruction. You can use this capability for JTAG testing before configuration when some of the Stratix II GX pins drive or receive from other devices on the board using voltage-referenced standards. Since the Stratix II GX device may not be configured before JTAG testing, the I/O pins may not be configured for appropriate electrical standards for chip-to-chip communication. Programming these I/O standards via JTAG allows you to fully test I/O connections to other devices.

A device operating in JTAG mode uses four required pins, `TDI`, `TDO`, `TMS`, and `TCK`, and one optional pin, `TRST`. The `TCK` pin has an internal weak pull-down resistor, while the `TDI`, `TMS`, and `TRST` pins have weak internal pull-up resistors. The JTAG input pins are powered by the 3.3-V `VCCPD` pins. The `TDO` output pin is powered by the `VCCIO` power supply in I/O bank 4.

Stratix II GX devices also use the JTAG port to monitor the logic operation of the device with the SignalTap® II embedded logic analyzer. Stratix II GX devices support the JTAG instructions shown in Table 3–1.

Stratix II GX devices must be within the first eight devices in a JTAG chain. All of these devices have the same JTAG controller. If any of the Stratix II GX devices appear after the eighth device in the JTAG chain, they will fail configuration. This does not affect SignalTap II embedded logic analysis.

Table 4–2. Maximum Duty Cycles in Voltage Transitions			
Symbol	**Parameter**	**Condition**	**Maximum Duty Cycles (%)** *(1)*
V_I	Maximum duty cycles in voltage transitions	V_I = 4.0 V	100
		V_I = 4.1 V	90
		V_I = 4.2 V	50
		V_I = 4.3 V	30
		V_I = 4.4 V	17
		V_I = 4.5 V	10

Note to Table 4–2:

(1) During transition, the inputs may overshoot to the voltages shown based on the input duty cycle. The duty cycle case is equivalent to 100% duty cycle.

Recommended Operating Conditions

Table 4–3 contains the Stratix II GX device family recommended operating conditions.

Table 4–3. Stratix II GX Device Recommended Operating Conditions (Part 1 of 2) Note (1)					
Symbol	**Parameter**	**Conditions**	**Minimum**	**Maximum**	**Unit**
V_{CCINT}	Supply voltage for internal logic and input buffers	100 µs ≤rise time ≤100 ms *(3)*	1.15	1.25	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	100 µs ≤rise time ≤100 ms *(3)*, *(6)*	3.135 (3.00)	3.465 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	100 µs ≤rise time ≤100 ms *(3)*	2.375	2.625	V
	Supply voltage for output buffers, 1.8-V operation	100 µs ≤rise time ≤100 ms *(3)*	1.71	1.89	V
	Supply voltage for output buffers, 1.5-V operation	100 µs ≤rise time ≤100 ms *(3)*	1.425	1.575	V
	Supply voltage for output buffers, 1.2-V operation	100 µs ≤rise time ≤100 ms *(3)*	1.15	1.25	V
V_{CCPD}	Supply voltage for pre-drivers as well as configuration and JTAG I/O buffers.	100 µs ≤rise time ≤100 ms *(4)*	3.135	3.465	V
V_I	Input voltage (see Table 4–2)	*(2)*, *(5)*	–0.5	4.0	V
V_O	Output voltage		0	V_{CCIO}	V

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 3 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Fibre Channel Transmit Jitter Generation *(8), (17)*											
Total jitter FC-1	REFCLK = 106.25 MHz Pattern = CRPAT V_{OD} = 800 mV No Pre-emphasis	-	-	0.23	-	-	0.23	-	-	0.23	UI
Deterministic jitter FC-1	REFCLK = 106.25 MHz Pattern = CRPAT V_{OD} = 800 mV No Pre-emphasis	-	-	0.11	-	-	0.11	-	-	0.11	UI
Total jitter FC-2	REFCLK = 106.25 MHz Pattern = CRPAT V_{OD} = 800 mV No Pre-emphasis	-	-	0.33	-	-	0.33	-	-	0.33	UI
Deterministic jitter FC-2	REFCLK = 106.25 MHz Pattern = CRPAT V_{OD} = 800 mV No Pre-emphasis	-	-	0.2	-	-	0.2	-	-	0.2	UI
Total jitter FC-4	REFCLK = 106.25 MHz Pattern = CRPAT V_{OD} = 800 mV No Pre-emphasis	-	-	0.52	-	-	0.52	-	-	0.52	UI
Deterministic jitter FC-4	REFCLK = 106.25 MHz Pattern = CRPAT V_{OD} = 800 mV No Pre-emphasis	-	-	0.33	-	-	0.33	-	-	0.33	UI
Fibre Channel Receiver Jitter Tolerance *(8), (18)*											
Deterministic jitter FC-1	Pattern = CJTPAT No Equalization DC Gain = 0 dB	> 0.37			> 0.37			> 0.37			UI
Random jitter FC-1	Pattern = CJTPAT No Equalization DC Gain = 0 dB	> 0.31			> 0.31			> 0.31			UI

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 9 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
HiGig Receiver Jitter Tolerance *(13)*											
Deterministic Jitter Tolerance (peak-to-peak)	Data Rate = 3.75 Gbps REFCLK = 187.5 MHz Pattern = CJPAT No Equalization DC Gain = 3 dB		> 0.37			-			-		UI
Combined Deterministic and Random Jitter Tolerance (peak-to-peak)	Data Rate = 3.75 Gbps REFCLK = 187.5 MHz Pattern = CJPAT No Equalization DC Gain = 3 dB		> 0.65			-			-		UI
	Jitter Frequency = 22.1 KHz Data Rate = 3.75 Gbps REFCLK = 187.5 MHz Pattern = CJPAT No Equalization DC Gain = 3 dB		> 8.5			-			-		UI

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 10 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Sinusoidal Jitter Tolerance (peak-to-peak)	Jitter Frequency = 1.875 MHz Data Rate = 3.75 Gbps REFCLK = 187.5 MHz Pattern = CJPAT No Equalization DC Gain = 3 dB	> 0.1			-			-			UI
	Jitter Frequency = 20 MHz Data Rate = 3.75 Gbps REFCLK = 187.5 MHz Pattern = CJPAT No Equalization DC Gain = 3 dB	> 0.1			-			-			UI
(OIF) CEI Transmitter Jitter Generation *(14)*											
Total Jitter (peak-to-peak)	Data Rate = 6.375 Gbps REFCLK = 318.75 MHz Pattern = PRBS15 Vod=1000 mV *(5)* No Pre-emphasis BER = 10^{-12}			0.3			N/A			N/A	UI
(OIF) CEI Receiver Jitter Tolerance *(14)*											
Deterministic Jitter Tolerance (peak-to-peak)	Data Rate = 6.375 Gbps Pattern = PRBS31 Equalizer Setting = 15 DC Gain = 0 dB BER = 10^{-12}	> 0.675			N/A			N/A			UI

Table 4–59. M512 Block Internal Timing Microparameters (Part 2 of 2)

Symbol	Parameter	-3 Speed Grade (2)		-3 Speed Grade (3)		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{M512CLR}$	Minimum clear pulse width	144		151		160		192		ps

(1) The M512 block f_{MAX} obtained using the Quartus II software does not necessarily equal to 1/TM512RC.
(2) This column refers to –3 speed grades for EP2SGX30, EP2SGX60, and EP2SGX90 devices.
(3) This column refers to –3 speed grades for EP2SGX130 devices.

Table 4–60. M4K Block Internal Timing Microparameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	-3 Speed Grade (2)		-3 Speed Grade (3)		-4 Speed Grade		-5 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{M4KRC}	Synchronous read cycle time	1462	2240	1462	2351	1462	2500	1462	3000	ps
$t_{M4KWERESU}$	Write or read enable setup time before clock	22		23		24		29		ps
$t_{M4KWEREH}$	Write or read enable hold time after clock	203		213		226		272		ps
$t_{M4KBESU}$	Byte enable setup time before clock	22		23		24		29		ps
t_{M4KBEH}	Byte enable hold time after clock	203		213		226		272		ps
$t_{M4KDATAASU}$	A port data setup time before clock	22		23		24		29		ps
$t_{M4KDATAAH}$	A port data hold time after clock	203		213		226		272		ps
$t_{M4KADDRASU}$	A port address setup time before clock	22		23		24		29		ps
$t_{M4KADDRAH}$	A port address hold time after clock	203		213		226		272		ps
$t_{M4KDATABSU}$	B port data setup time before clock	22		23		24		29		ps

Therefore, the DCD percentage for the output clock is from 48.4% to 51.6%.

Table 4–101. Maximum DCD for DDIO Output on Row I/O Pins Without PLL in the Clock Path for -4 and -5 Devices *Note (1)*

Maximum DCD (ps) for Row DDIO Output I/O Standard	Input I/O Standard (No PLL in the Clock Path)					Unit
	TTL/CMOS		SSTL-2	SSTL/HSTL	LVDS	
	3.3/2.5V	1.8/1.5V	2.5V	1.8/1.5V	3.3V	
3.3-V LVTTL	440	495	170	160	105	ps
3.3-V LVCMOS	390	450	120	110	75	ps
2.5 V	375	430	105	95	90	ps
1.8 V	325	385	90	100	135	ps
1.5-V LVCMOS	430	490	160	155	100	ps
SSTL-2 Class I	355	410	85	75	85	ps
SSTL-2 Class II	350	405	80	70	90	ps
SSTL-18 Class I	335	390	65	65	105	ps
1.8-V HSTL Class I	330	385	60	70	110	ps
1.5-V HSTL Class I	330	390	60	70	105	ps
LVDS	180	180	180	180	180	ps

(1) Table 4–101 assumes the input clock has zero DCD.

Table 4–102. Maximum DCD for DDIO Output on Column I/O Pins Without PLL in the Clock Path for -3 Devices (Part 1 of 2) *Note (1)*

Maximum DCD (ps) for DDIO Column Output I/O Standard	Input IO Standard (No PLL in the Clock Path)					Unit
	TTL/CMOS		SSTL-2	SSTL/HSTL	HSTL12	
	3.3/2.5V	1.8/1.5V	2.5V	1.8/1.5V	1.2V	
3.3-V LVTTL	260	380	145	145	145	ps
3.3-V LVCMOS	210	330	100	100	100	ps
2.5 V	195	315	85	85	85	ps
1.8 V	150	265	85	85	85	ps
1.5-V LVCMOS	255	370	140	140	140	ps
SSTL-2 Class I	175	295	65	65	65	ps
SSTL-2 Class II	170	290	60	60	60	ps
SSTL-18 Class I	155	275	55	50	50	ps

Table 4–102. Maximum DCD for DDIO Output on Column I/O Pins Without PLL in the Clock Path for -3 Devices (Part 2 of 2) *Note (1)*

Maximum DCD (ps) for DDIO Column Output I/O Standard	Input IO Standard (No PLL in the Clock Path)					Unit
	TTL/CMOS		SSTL-2	SSTL/HSTL	HSTL12	
	3.3/2.5V	1.8/1.5V	2.5V	1.8/1.5V	1.2V	
SSTL-18 Class II	140	260	70	70	70	ps
1.8-V HSTL Class I	150	270	60	60	60	ps
1.8-V HSTL Class II	150	270	60	60	60	ps
1.5-V HSTL Class I	150	270	55	55	55	ps
1.5-V HSTL Class II	125	240	85	85	85	ps
1.2-V HSTL	240	360	155	155	155	ps
LVPECL	180	180	180	180	180	ps

(1) Table 4–102 assumes the input clock has zero DCD.

Table 4–103. Maximum DCD for DDIO Output on Column I/O Pins Without PLL in the Clock Path for -4 and -5 Devices *Note (1)*

Maximum DCD (ps) for DDIO Column Output I/O Standard	Input IO Standard (No PLL in the Clock Path)				Unit
	TTL/CMOS		SSTL-2	SSTL/HSTL	
	3.3/2.5V	1.8/1.5V	2.5V	1.8/1.5V	
3.3-V LVTTL	440	495	170	160	ps
3.3-V LVCMOS	390	450	120	110	ps
2.5 V	375	430	105	95	ps
1.8 V	325	385	90	100	ps
1.5-V LVCMOS	430	490	160	155	ps
SSTL-2 Class I	355	410	85	75	ps
SSTL-2 Class II	350	405	80	70	ps
SSTL-18 Class I	335	390	65	65	ps
SSTL-18 Class II	320	375	70	80	ps
1.8-V HSTL Class I	330	385	60	70	ps
1.8-V HSTL Class II	330	385	60	70	ps
1.5-V HSTL Class I	330	390	60	70	ps
1.5-V HSTL Class II	330	360	90	100	ps
LVPECL	180	180	180	180	ps

(1) Table 4–103 assumes the input clock has zero DCD.

Table 4–108 shows the high-speed I/O timing specifications for -4 speed grade Stratix II GX devices.

Table 4–108. High-Speed I/O Specifications for -4 Speed Grade *Notes (1), (2)*

Symbol	Conditions			-4 Speed Grade			Unit
				Min	Typ	Max	
$f_{IN} = f_{HSDR} / W$	W = 2 to 32 (LVDS, HyperTransport technology) *(3)*			16		520	MHz
	W = 1 (SERDES bypass, LVDS only)			16		500	MHz
	W = 1 (SERDES used, LVDS only)			150		717	MHz
f_{HSDR} (data rate)	J = 4 to 10 (LVDS, HyperTransport technology)			150		1,040	Mbps
	J = 2 (LVDS, HyperTransport technology)			*(4)*		760	Mbps
	J = 1 (LVDS only)			*(4)*		500	Mbps
$f_{HSDRDPA}$ (DPA data rate)	J = 4 to 10 (LVDS, HyperTransport technology)			150		1,040	Mbps
TCCS	All differential standards			-		200	ps
SW	All differential standards			330		-	ps
Output jitter						190	ps
Output t_{RISE}	All differential I/O standards					160	ps
Output t_{FALL}	All differential I/O standards					180	ps
t_{DUTY}				45	50	55	%
DPA run length						6,400	UI
DPA jitter tolerance	Data channel peak-to-peak jitter			0.44			UI
DPA lock time							Number of repetitions
	SPI-4	0000000000 1111111111	10%	256			
	Parallel Rapid I/O	00001111	25%	256			
		10010000	50%	256			
	Miscellaneous	10101010	100%	256			
		01010101		256			

(1) When J = 4 to 10, the SERDES block is used.
(2) When J = 1 or 2, the SERDES block is bypassed.
(3) The input clock frequency and the W factor must satisfy the following fast PLL VCO specification: 150 ≤nput clock frequency × W ≤1,040.
(4) The minimum specification is dependent on the clock source (fast PLL, enhanced PLL, clock pin, and so on) and the clock routing resource (global, regional, or local) utilized. The I/O differential buffer and input register do not have a minimum toggle rate.