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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	4548
Number of Logic Elements/Cells	90960
Total RAM Bits	4520448
Number of I/O	650
Number of Gates	-
Voltage - Supply	1.15V ~ 1.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1508-BBGA, FCBGA
Supplier Device Package	1508-FBGA, FC (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/ep2sgx90ff1508i4n

There are up to 20 transceiver channels available on a single Stratix II GX device. Table 2–1 shows the number of transceiver channels and their serial bandwidth for each Stratix II GX device.

Table 2–1. Stratix II GX Transceiver Channels

Device	Number of Transceiver Channels	Serial Bandwidth (Full Duplex)
EP2SGX30C	4	51 Gbps
EP2SGX60C	4	51 Gbps
EP2SGX30D	8	102 Gbps
EP2SGX60D	8	102 Gbps
EP2SGX60E	12	153 Gbps
EP2SGX90E	12	153 Gbps
EP2SGX90F	16	204 Gbps
EP2SGX130G	20	255 Gbps

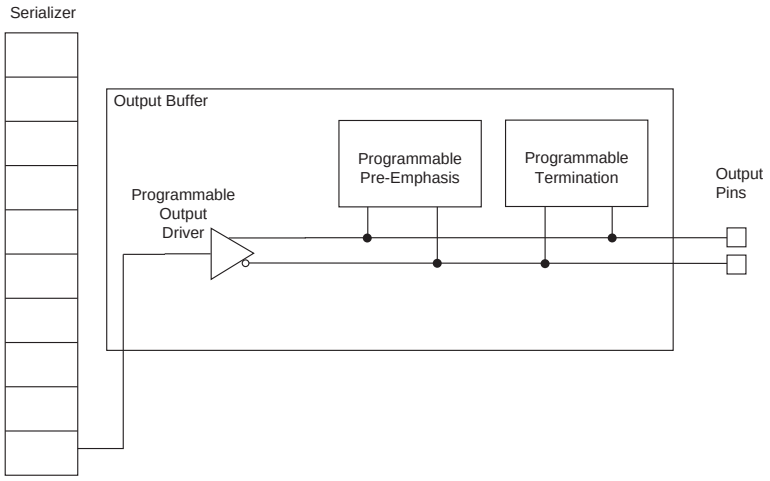
Figure 2–2 shows the elements of the transceiver block, including the four transceiver channels, supporting logic, and I/O buffers. Each transceiver channel consists of a receiver and transmitter. The supporting logic contains two transmitter PLLs to generate the high-speed clock(s) used by the four transmitters within that block. Each of the four transmitter channels has its own individual clock divider. The four receiver PLLs within each transceiver block generate four recovered clocks. The transceiver channels can be configured in one of the following functional modes:

- PCI Express (PIPE)
- OIF CEI PHY Interface
- SONET/SDH
- Gigabit Ethernet (GIGE)
- XAUI
- Basic (600 Mbps to 3.125 Gbps single-width mode and 1 Gbps to 6.375 Gbps double-width mode)
- SDI (HD, 3G)
- CPRI (614 Mbps, 1228 Mbps, 2456 Mbps)
- Serial RapidIO (1.25 Gbps, 2.5 Gbps, 3.125 Gbps)

Refer to the *Stratix II GX Transceiver Architecture Overview* chapter in volume 2 of the *Stratix II GX Handbook*.

The output buffer, as shown in Figure 2–8, is directly driven by the high-speed data serializer and consists of a programmable output driver, a programmable pre-emphasis circuit, a programmable termination, and a programmable V_{CM}.

Figure 2–8. Output Buffer



Programmable Output Driver

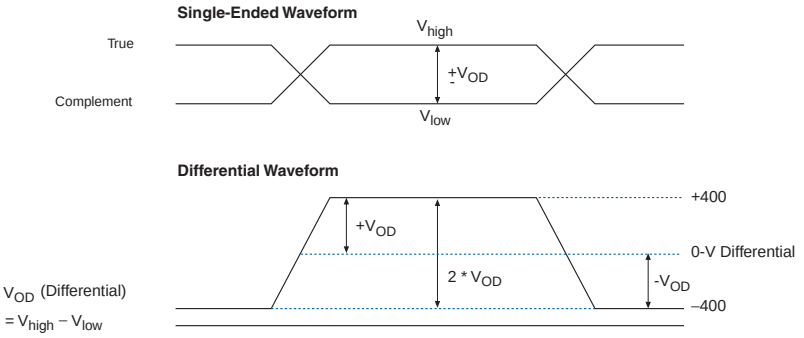
The programmable output driver can be set to drive out differentially 200 to 1,400 mV. The differential output voltage (V_{OD}) can be changed dynamically, or statically set by using the ALT2GXB megafunction or through I/O pins.

The output driver may be programmed with four different differential termination values:

- 100 Ω
- 120 Ω
- 150 Ω
- External termination

Differential signaling conventions are shown in Figure 2–9. The differential amplitude represents the value of the voltage between the true and complement signals. Peak-to-peak differential voltage is defined as $2 \times (V_{HIGH} - V_{LOW}) = 2 \times$ single-ended voltage swing. The common mode voltage is the average of V_{high} and V_{low}.

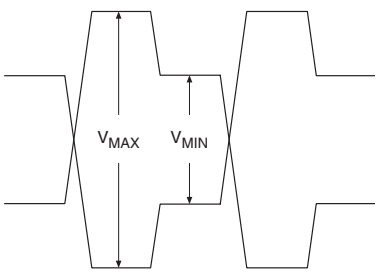
Figure 2–9. Differential Signaling



Programmable Pre-Emphasis

The programmable pre-emphasis module controls the output driver to boost the high frequency components, and compensate for losses in the transmission medium, as shown in Figure 2–10. The pre-emphasis is set statically using the ALT2GXB megafunction or dynamically through the dynamic reconfiguration controller.

Figure 2–10. Pre-Emphasis Signaling



$$\text{Pre-Emphasis \%} = \left(\frac{V_{MAX}}{V_{MIN}} - 1 \right) \times 100$$

When the FIFO pointers initialize, the receiver domain clock must remain phase locked to receiver FPGA clock.

After resetting the receiver FIFO buffer, writing to the receiver FIFO buffer begins and continues on each parallel clock. The phase compensation FIFO buffer is eight words deep for PIPE mode and four words deep for all other modes.

Loopback Modes

The Stratix II GX transceiver has built-in loopback modes for debugging and testing. The loopback modes are configured in the Stratix II GX ALT2GXB megafunction in the Quartus II software. The available loopback modes are:

- Serial loopback
- Parallel loopback
- Reverse serial loopback
- Reverse serial loopback (pre-CDR)
- PCI Express PIPE reverse parallel loopback (available only in PIPE mode)

Serial Loopback

The serial loopback mode exercises all the transceiver logic, except for the input buffer. Serial loopback is available for all non-PIPE modes. The loopback function is dynamically enabled through the `rx_seriallpbken` port on a channel-by-channel basis.

In serial loopback mode, the data on the transmit side is sent by the PLD. A separate mode is available in the ALT2GXB megafunction under Basic protocol mode, in which PRBS data is generated and verified internally in the transceiver. The PRBS patterns available in this mode are shown in Table 2–10.

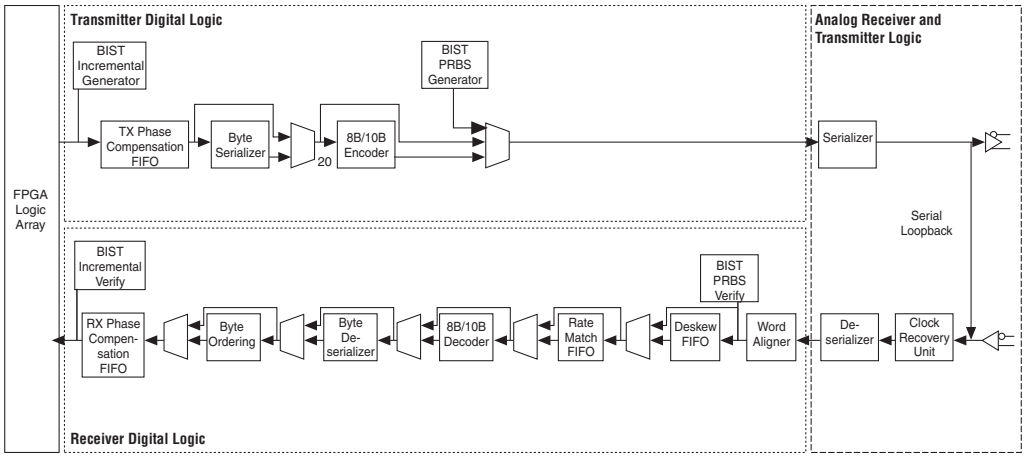
Table 2–10 shows the BIST data output and verifier alignment pattern.

Table 2–10. BIST Data Output and Verifier Alignment Pattern

Pattern	Polynomial	Parallel Data Width			
		8-Bit	10-Bit	16-Bit	20-Bit
PRBS-7	×7 + ×6 + 1				✓
PRBS-10	×10 + ×7 + 1		✓		

Figure 2–24 shows the data path in serial loopback mode.

Figure 2–24. Stratix II GX Block in Serial Loopback Mode with BIST and PRBS



Parallel Loopback

The parallel loopback mode exercises the digital logic portion of the transceiver data path. The analog portions are not used in this loopback path, and the received high-speed serial data is not retimed. This protocol is available as one of the sub-protocols under Basic mode and can be used only for Basic double-width mode.

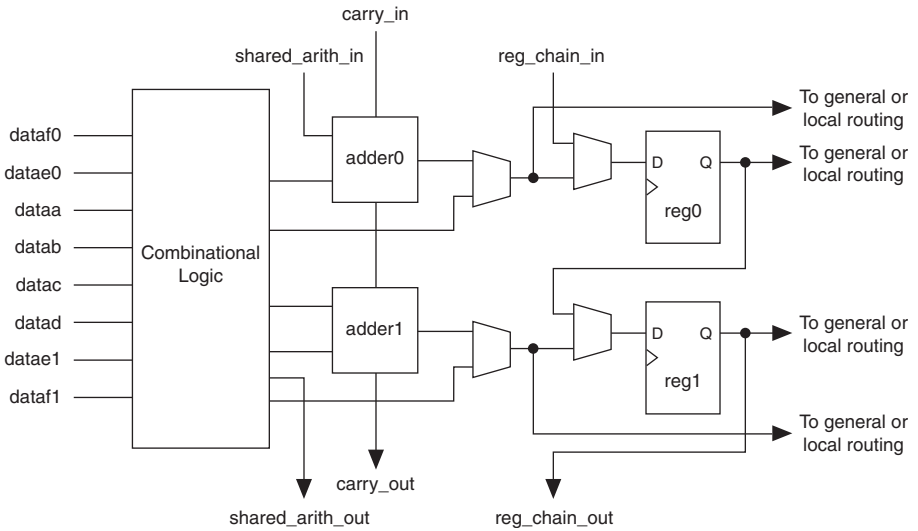
In this loopback mode, the data from the internally available BIST generator is transmitted. The data is looped back after the end of PCS and before the PMA. On the receive side, an internal BIST verifier checks for errors. This loopback enables you to verify the PCS block.

Adaptive Logic Modules

The basic building block of logic in the Stratix II GX architecture is the ALM. The ALM provides advanced features with efficient logic utilization. Each ALM contains a variety of look-up table (LUT)-based resources that can be divided between two adaptive LUTs (ALUTs). With up to eight inputs to the two ALUTs, one ALM can implement various combinations of two functions. This adaptability allows the ALM to be completely backward-compatible with four-input LUT architectures. One ALM can also implement any function of up to six inputs and certain seven-input functions.

In addition to the adaptive LUT-based resources, each ALM contains two programmable registers, two dedicated full adders, a carry chain, a shared arithmetic chain, and a register chain. Through these dedicated resources, the ALM can efficiently implement various arithmetic functions and shift registers. Each ALM drives all types of interconnects: local, row, column, carry chain, shared arithmetic chain, register chain, and direct link interconnects. Figure 2–35 shows a high-level block diagram of the Stratix II GX ALM while Figure 2–36 shows a detailed view of all the connections in the ALM.

Figure 2–35. High-Level Block Diagram of the Stratix II GX ALM



Figures 2–57 shows one of the columns with surrounding LAB rows.

Figure 2–57. DSP Blocks Arranged in Columns

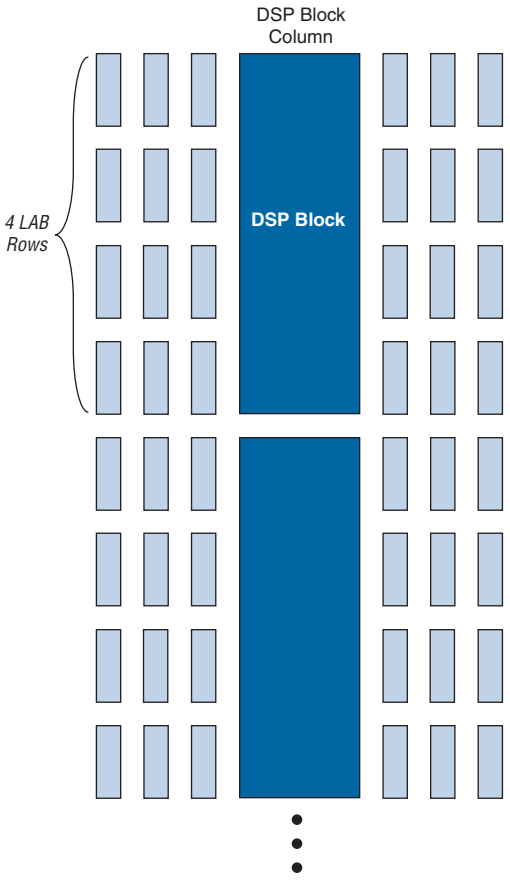
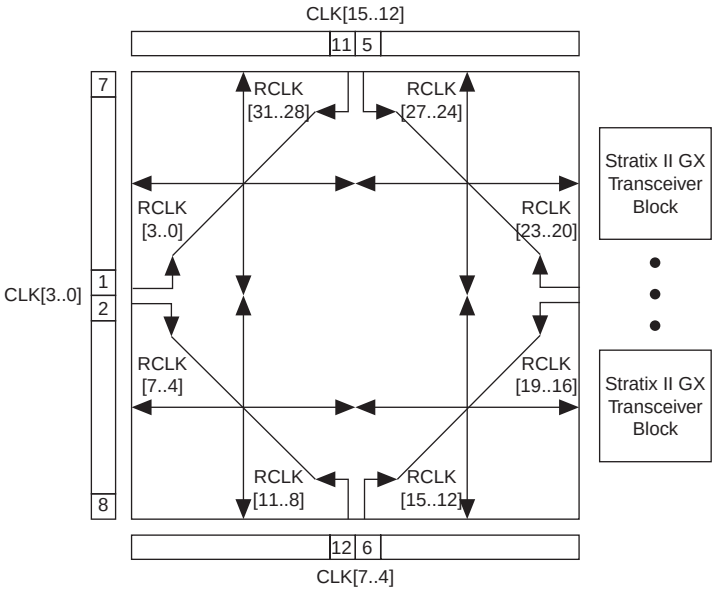


Figure 2–62. Regional Clocks



Dual-Regional Clock Network

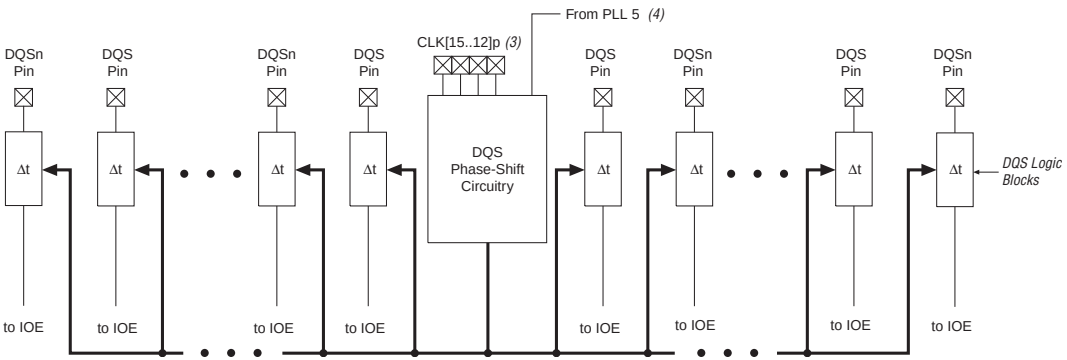
A single source (CLK pin or PLL output) can generate a dual-regional clock by driving two regional clock network lines in adjacent quadrants (one from each quadrant), which allows logic that spans multiple quadrants to utilize the same low skew clock. The routing of this clock signal on an entire side has approximately the same speed but slightly higher clock skew when compared with a clock signal that drives a single quadrant. Internal logic-array routing can also drive a dual-regional clock. Clock pins and enhanced PLL outputs on the top and bottom can drive horizontal dual-regional clocks. Clock pins and fast PLL outputs on the left and right can drive vertical dual-regional clocks, as shown in Figure 2–63. Corner PLLs cannot drive dual-regional clocks.

A compensated delay element on each DQS pin automatically aligns input DQS synchronization signals with the data window of their corresponding DQ data signals. The DQS signals drive a local DQS bus in the top and bottom I/O banks. This DQS bus is an additional resource to the I/O clocks and is used to clock DQ input registers with the DQS signal.

The Stratix II GX device has two phase-shifting reference circuits, one on the top and one on the bottom of the device. The circuit on the top controls the compensated delay elements for all DQS pins on the top. The circuit on the bottom controls the compensated delay elements for all DQS pins on the bottom.

Each phase-shifting reference circuit is driven by a system reference clock, which must have the same frequency as the DQS signal. Clock pins `CLK[15..12]p` feed the phase circuitry on the top of the device and clock pins `CLK[7..4]p` feed the phase circuitry on the bottom of the device. In addition, PLL clock outputs can also feed the phase-shifting reference circuits. Figure 2–86 shows the phase-shift reference circuit control of each DQS delay shift on the top of the device. This same circuit is duplicated on the bottom of the device.

Figure 2–86. DQS Phase-Shift Circuitry *Notes (1), (2)*



Notes to Figure 2–86:

(1) There are up to 18 pairs of DQS and DQSn pins available on the top or the bottom of the Stratix II GX device. There are up to 10 pairs on the right side and 8 pairs on the left side of the DQS phase-shift circuitry.

(2) The "t" module represents the DQS logic block.

(3) Clock pins `CLK[15..12]p` feed the phase-shift circuitry on the top of the device and clock pins `CLK[7..4]p` feed the phase circuitry on the bottom of the device. You can also use a PLL clock output as a reference clock to the phaseshift circuitry.

(4) You can only use PLL 5 to feed the DQS phase-shift circuitry on the top of the device and PLL 6 to feed the DQS phase-shift circuitry on the bottom of the device.

memory, and transmit this compressed bitstream to Stratix II GX FPGAs. During configuration, the Stratix II GX FPGA decompresses the bitstream in real time and programs its SRAM cells. Stratix II GX FPGAs support decompression in the FPP (when using a MAX II device or microprocessor and flash memory), AS, and PS configuration schemes. Decompression is not supported in the PPA configuration scheme nor in JTAG-based configuration.

Remote System Upgrades

Shortened design cycles, evolving standards, and system deployments in remote locations are difficult challenges faced by system designers. Stratix II GX devices can help effectively deal with these challenges with their inherent re programmability and dedicated circuitry to perform remote system updates. Remote system updates help deliver feature enhancements and bug fixes without costly recalls, reducing time to market, and extending product life.

Stratix II GX FPGAs feature dedicated remote system upgrade circuitry to facilitate remote system updates. Soft logic (Nios processor or user logic) implemented in the Stratix II GX device can download a new configuration image from a remote location, store it in configuration memory, and direct the dedicated remote system upgrade circuitry to initiate a reconfiguration cycle. The dedicated circuitry performs error detection during and after the configuration process, recovers from any error condition by reverting back to a safe configuration image, and provides error status information. This dedicated remote system upgrade circuitry avoids system downtime and is the critical component for successful remote system upgrades.

Remote system configuration is supported in the following Stratix II GX configuration schemes: FPP, AS, PS, and PPA. Remote system configuration can also be implemented in conjunction with Stratix II GX features such as real-time decompression of configuration data and design security using AES for secure and efficient field upgrades.

Refer to the *Remote System Upgrades with Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Device Handbook* for more information about remote configuration in Stratix II GX devices.

Configuring Stratix II GX FPGAs with JRunner

The JRunner™ software driver configures Altera FPGAs, including Stratix II GX FPGAs, through the ByteBlaster II or ByteBlasterMV cables in JTAG mode. The programming input file supported is in Raw Binary File (**.rbf**) format. JRunner also requires a Chain Description File (**.cdf**)

Table 4–6. Stratix II GX Transceiver Block AC Specification (Part 3 of 6)

Symbol / Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
reconfig_clk clock frequency		2.5	-	50	2.5	-	50	2.5	-	50	MHz
Transceiver block minimum power-down pulse width		100	-	-	100	-	-	100	-	-	ns
Receiver											
Data rate		600	-	6375	600	-	5000	600	-	4250	Mbps
Absolute V_{MAX} for a receiver pin *(1)*		-	-	2.0	-	-	2.0	-	-	2.0	V
Absolute V_{MIN} for a receiver pin		-0.4	-	-	-0.4	-	-	-0.4	-	-	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p)	V_{CM} = 0.85 V	-	-	3.3	-	-	3.3	-	-	3.3	V
Minimum peak-to-peak differential input voltage V_{ID} (diff p-p)	V_{CM} = 0.85 V DC Gain = ≥ 3 dB	160	-	-	160	-	-	160	-	-	mV
V_{ICM}	V_{ICM} = 0.85 V setting	850±10%			850±10%			850±10%			mV
	V_{ICM} = 1.2 V setting *(11)*	1200±10%			1200±10%			1200±10%			mV
On-chip termination resistors	100 Ω setting	100±15%			100±15%			100±15%			Ω
	120 Ω setting	120±15%			120±15%			120±15%			Ω
	150 Ω setting	150±15%			150±15%			150±15%			Ω
Bandwidth at 6.375 Gbps	BW = Low	-	20	-	-	-	-	-	-	-	MHz
	BW = Med	-	35	-	-	-	-	-	-	-	MHz
	BW = High	-	45	-	-	-	-	-	-	-	MHz

Table 4–19 shows the Stratix II GX transceiver block AC specifications.

Table 4–19. Stratix II GX Transceiver Block AC Specification Notes (1), (2), (3) (Part 1 of 19)

Symbol/ Description	Conditions	-3 Speed Commercial Speed Grade			-4 Speed Commercial and Industrial Speed Grade			-5 Speed Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SONET/SDH Transmit Jitter Generation *(7)*											
Peak-to-peak jitter at 622.08 Mbps	REFCLK = 77.76 MHz Pattern = PRBS23 V_{OD} = 800 mV No Pre-emphasis	-	-	0.1	-	-	0.1	-	-	0.1	UI
RMS jitter at 622.08 Mbps	REFCLK = 77.76 MHz Pattern = PRBS23 V_{OD} = 800 mV No Pre-emphasis	-	-	0.01	-	-	0.01	-	-	0.01	UI
Peak-to-peak jitter at 2488.32 Mbps	REFCLK = 155.52 MHz Pattern = PRBS23 V_{OD} = 800 mV No Pre-emphasis	-	-	0.1	-	-	0.1	-	-	0.1	UI
RMS jitter at 2488.32 Mbps	REFCLK = 155.52 MHz Pattern = PRBS23 V_{OD} = 800 mV No Pre-emphasis	-	-	0.01	-	-	0.01	-	-	0.01	UI

Table 4–20. Recommended Input Clock Jitter (Part 2 of 2)

Mode	Reference Clock (MHz)	Vectron LVPECL XO Type/Model	Frequency Range (MHz)	RMS Jitter (12 kHz to 20 MHz) (ps)	Period Jitter (Peak to Peak) (ps)	Phase Noise at 1 MHz (dB c/Hz)
SONET/SDH OC-48	77.76	VCC6-Q/R	10 to 270	0.3	23	-149.5476
	155.52	VCC6-Q/R	10 to 270	0.3	23	-149.1903
	311.04	VCC6-Q	270 to 800	2	30	Not available
	622.08	VCC6-Q	270 to 800	2	30	Not available
SONET/SDH OC-12	62.2	VCC6-Q/R	10 to 270	0.3	23	-149.6289
	311	VCC6-Q	270 to 800	2	30	Not available
	77.76	VCC6-Q/R	10 to 270	0.3	23	-149.5476
	155.52	VCC6-Q/R	10 to 270	0.3	23	-149.1903
	622.08	VCC6-Q	270 to 800	2	30	Not available

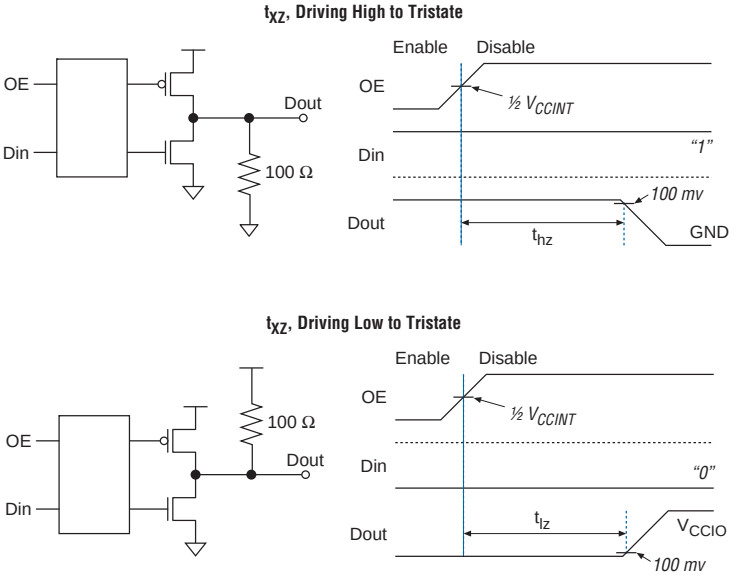
Tables 4–21 and 4–22 show the transmitter and receiver PCS latency for each mode, respectively.

Table 4–21. PCS Latency (Part 1 of 2) *Note (1)*

Functional Mode	Configuration	Transmitter PCS Latency					
		TX PIPE	TX Phase Comp FIFO	Byte Serializer	TX State Machine	8B/10B Encoder	Sum *(2)*
XAUI		-	2-3	1	0.5	0.5	4-5
PIPE	×1, ×4, ×8 8-bit channel width	1	3-4	1	-	1	6-7
	×1, ×4, ×8 16-bit channel width	1	3-4	1	-	0.5	6-7
GIGE		-	2-3	1	-	1	4-5
SONET/SDH	OC-12	-	2-3	1	-	1	4-5
	OC-48	-	2-3	1	-	0.5	4-5
	OC-96	-	2-3	1	-	0.5	4-5
(OIF) CEI PHY		-	2-3	1	-	0.5	4-5
CPRI *(3)*	614 Mbps, 1.228 Gbps	-	2	1	-	1	4
	2.456 Gbps	-	2-3	1	-	1	4-5

Figures 4–9 and 4–10 show the measurement setup for output disable and output enable timing.

Figure 4–9. Measurement Setup for t_{xz} *Note (1)*



Note to Figure 4–9:

(1) V_{CCINT} is 1.12 V for this measurement.

Table 4–65. EP2SGX30 Column Pins Regional Clock Timing Parameters

Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.493	1.507	2.522	2.806	3.364	ns
t_{COUT}	1.353	1.372	2.525	2.809	3.364	ns
t_{PLLCIN}	0.087	0.104	0.237	0.253	0.292	ns
$t_{PLLCOUT}$	-0.078	-0.061	0.237	0.253	0.29	ns

Table 4–66. EP2SGX30 Row Pins Regional Clock Timing Parameters

Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.246	1.262	2.437	2.712	3.246	ns
t_{COUT}	1.251	1.267	2.437	2.712	3.246	ns
t_{PLLCIN}	-0.18	-0.167	0.215	0.229	0.263	ns
$t_{PLLCOUT}$	-0.175	-0.162	0.215	0.229	0.263	ns

EP2SGX60 Clock Timing Parameters

Tables 4–67 through 4–70 show the maximum clock timing parameters for EP2SGX60 devices.

Table 4–67. EP2SGX60 Column Pins Global Clock Timing Parameters

Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.722	1.736	2.940	3.275	3.919	ns
t_{COUT}	1.557	1.571	2.698	3.005	3.595	ns
t_{PLLCIN}	0.037	0.051	0.474	0.521	0.613	ns
$t_{PLLCOUT}$	-0.128	-0.114	0.232	0.251	0.289	ns

Table 4–74. EP2SGX90 Row Pins Regional Clock Timing Parameters						
Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.444	1.461	2.792	3.108	3.716	ns
t_{COUT}	1.449	1.466	2.792	3.108	3.716	ns
t_{PLLCIN}	-0.348	-0.333	0.204	0.217	0.243	ns
$t_{PLLCOUT}$	-0.343	-0.328	0.212	0.217	0.254	ns

EP2SGX130 Clock Timing Parameters

Tables 4–75 through 4–78 show the maximum clock timing parameters for EP2SGX130 devices.

Table 4–75. EP2SGX130 Column Pins Global Clock Timing Parameters						
Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.980	1.998	3.491	3.706	4.434	ns
t_{COUT}	1.815	1.833	3.237	3.436	4.110	ns
t_{PLLCIN}	-0.027	-0.009	0.307	0.322	0.376	ns
$t_{PLLCOUT}$	-0.192	-0.174	0.053	0.052	0.052	ns

Table 4–76. EP2SGX130 Row Pins Global Clock Timing Parameters						
Parameter	Fast Corner		-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Units
	Industrial	Commercial				
t_{CIN}	1.741	1.759	3.112	3.303	3.950	ns
t_{COUT}	1.746	1.764	3.108	3.299	3.945	ns
t_{PLLCIN}	-0.261	-0.243	-0.089	-0.099	-0.129	ns
$t_{PLLCOUT}$	-0.256	-0.238	-0.093	-0.103	-0.134	ns

Table 4–91. Stratix II GX Maximum Output Clock Rate for Column Pins (Part 3 of 3)					
I/O Standard	**Drive Strength**	**-3 Speed Grade**	**-4 Speed Grade**	**-5 Speed Grade**	**Unit**
Differential SSTL-18 Class I	4 mA	200	150	150	MHz
	6 mA	350	250	200	MHz
	8 mA	450	300	300	MHz
	10 mA	500	400	400	MHz
	12 mA	700	550	400	MHz
Differential SSTL-18 Class II	8 mA	200	200	150	MHz
	16 mA	400	350	350	MHz
	18 mA	450	400	400	MHz
	20 mA	550	500	450	MHz
1.8-V HSTL differential Class I	4 mA	300	300	300	MHz
	6 mA	500	450	450	MHz
	8 mA	650	600	600	MHz
	10 mA	700	650	600	MHz
	12 mA	700	700	650	MHz
1.8-V HSTL differential Class II	16 mA	500	500	450	MHz
	18 mA	550	500	500	MHz
	20 mA	650	550	550	MHz
1.5-V HSTL differential Class I	4 mA	350	300	300	MHz
	6 mA	500	500	450	MHz
	8 mA	700	650	600	MHz
	10 mA	700	700	650	MHz
	12 mA	700	700	700	MHz
1.5-V HSTL differential Class II	16 mA	600	600	550	MHz
	18 mA	650	600	600	MHz
	20 mA	700	650	600	MHz

(1) This is the default setting in the Quartus II software.

Table 4–94. Stratix II GX Maximum Output Clock Rate for Column Pins (Series Termination) (Part 2 of 2)

I/O Standard	Drive Strength	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
SSTL-18 Class I	OCT_50_OHMS	560	400	350	MHz
SSTL-18 Class II	OCT_25_OHMS	550	500	450	MHz
1.5-V HSTL Class I	OCT_50_OHMS	600	550	500	MHz
1.8-V HSTL Class I	OCT_50_OHMS	650	600	600	MHz
1.8-V HSTL Class II	OCT_25_OHMS	500	500	450	MHz
Differential SSTL-2 Class I	OCT_50_OHMS	600	500	500	MHz
Differential SSTL-2 Class II	OCT_25_OHMS	600	550	500	MHz
Differential SSTL-18 Class I	OCT_50_OHMS	560	400	350	MHz
Differential SSTL-18 Class II	OCT_25_OHMS	550	500	450	MHz
1.8-V differential HSTL Class I	OCT_50_OHMS	650	600	600	MHz
1.8-V differential HSTL Class II	OCT_25_OHMS	500	500	450	MHz
1.5-V differential HSTL Class I	OCT_50_OHMS	600	550	500	MHz

Table 4–95 shows the maximum output clock toggle rate for Stratix II GX device series-terminated row pins.

Table 4–95. Stratix II GX Maximum Output Clock Rate for Row Pins (Series Termination) (Part 1 of 2)

I/O Standard	Drive Strength	-3 Speed Grade	-4 Speed Grade	-5 Speed Grade	Unit
LVTTL	OCT_25_OHMS	400	400	350	MHz
	OCT_50_OHMS	400	400	350	MHz
LVCMOS	OCT_25_OHMS	350	350	300	MHz
	OCT_50_OHMS	350	350	300	MHz
2.5 V	OCT_25_OHMS	350	350	300	MHz
	OCT_50_OHMS	350	350	300	MHz
1.8 V	OCT_50_OHMS	700	550	450	MHz
1.5 V	OCT_50_OHMS	550	450	400	MHz

Table 4–105. Maximum DCD for DDIO Output on Column I/O Pins With PLL in the Clock Path (Part 2 of 2)			
Maximum DCD (ps) for Column DDIO Output I/O Standard	Stratix II GX Devices (PLL Output Feeding DDIO)		Unit
	-3 Device	-4 and -5 Device	
1.2-V HSTL	155	155	ps
LVPECL	180	180	ps

High-Speed I/O Specifications

Table 4–106 provides high-speed timing specifications definitions.

Table 4–106. High-Speed Timing Specifications and Definitions	
High-Speed Timing Specifications	Definitions
t_C	High-speed receiver/transmitter input and output clock period.
f_{HSCLK}	High-speed receiver/transmitter input and output clock frequency.
J	Deserialization factor (width of parallel data bus).
W	PLL multiplication factor.
t_{RISE}	Low-to-high transmission time.
t_{FALL}	High-to-low transmission time.
Timing unit interval (TUI)	The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency × Multiplication Factor) = t_C/w).
f_{IN}	Fast PLL input clock frequency
f_{HSDR}	Maximum/minimum LVDS data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
$f_{HSDRDPA}$	Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.
Channel-to-channel skew (TCCS)	The timing difference between the fastest and the slowest output edges including t_{CO} variation and clock skew across channels driven by the same fast PLL. The clock is included in the TCCS measurement.
Sampling window (SW)	The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window.
Input jitter	Peak-to-peak input jitter on high-speed PLLs.
Output jitter	Peak-to-peak output jitter on high-speed PLLs.
t_{DUTY}	Duty cycle on high-speed transmitter output clock.
t_{LOCK}	Lock time for high-speed transmitter and receiver PLLs.

Table 4–118. Document Revision History (Part 2 of 5)		
Date and Document Version	**Changes Made**	**Summary of Changes**
August 2007 v4.4	Removed note “The data in this table is preliminary. Altera will provide a report upon completion of characterization of the Stratix II GX devices. Conditions for testing the silicon have not been determined.” from each table.	
	Removed note “The data in Tables xxx through xxx is preliminary. Altera will provide a report upon completion of characterization of the Stratix II GX devices. Conditions for testing the silicon have not been determined.” in the clock timing parameters sections.	
	Updated clock timing parameter Tables 4–63 through 4–78 (Table 4–75 was unchanged).	
	Updated Table 4–21 and added new Table 4–22.	
	Updated: ● Table 4–6 ● Table 4–16 ● Table 4–19 ● Table 4–49 ● Table 4–52 ● Table 4–107	
	Added note to Table 4–50.	
	Added: ● Figure 4–3 ● Figure 4–4 ● Figure 4–5	
	Added the “Referenced Documents” section.	
May 2007 v4.3	Changed 1.875 KHz to 1.875 MHz in Table 4–19, XAUI Receiver Jitter Tolerance section.	