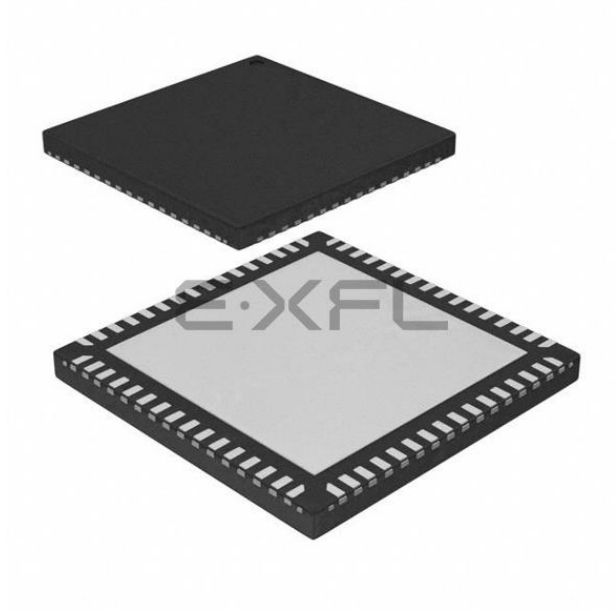

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	I²C, IrDA, Memory Card, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	47
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 10x10/12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam3s8ba-mu

Figure 2-2. SAM3S8/SD8 64-pin version Block Diagram

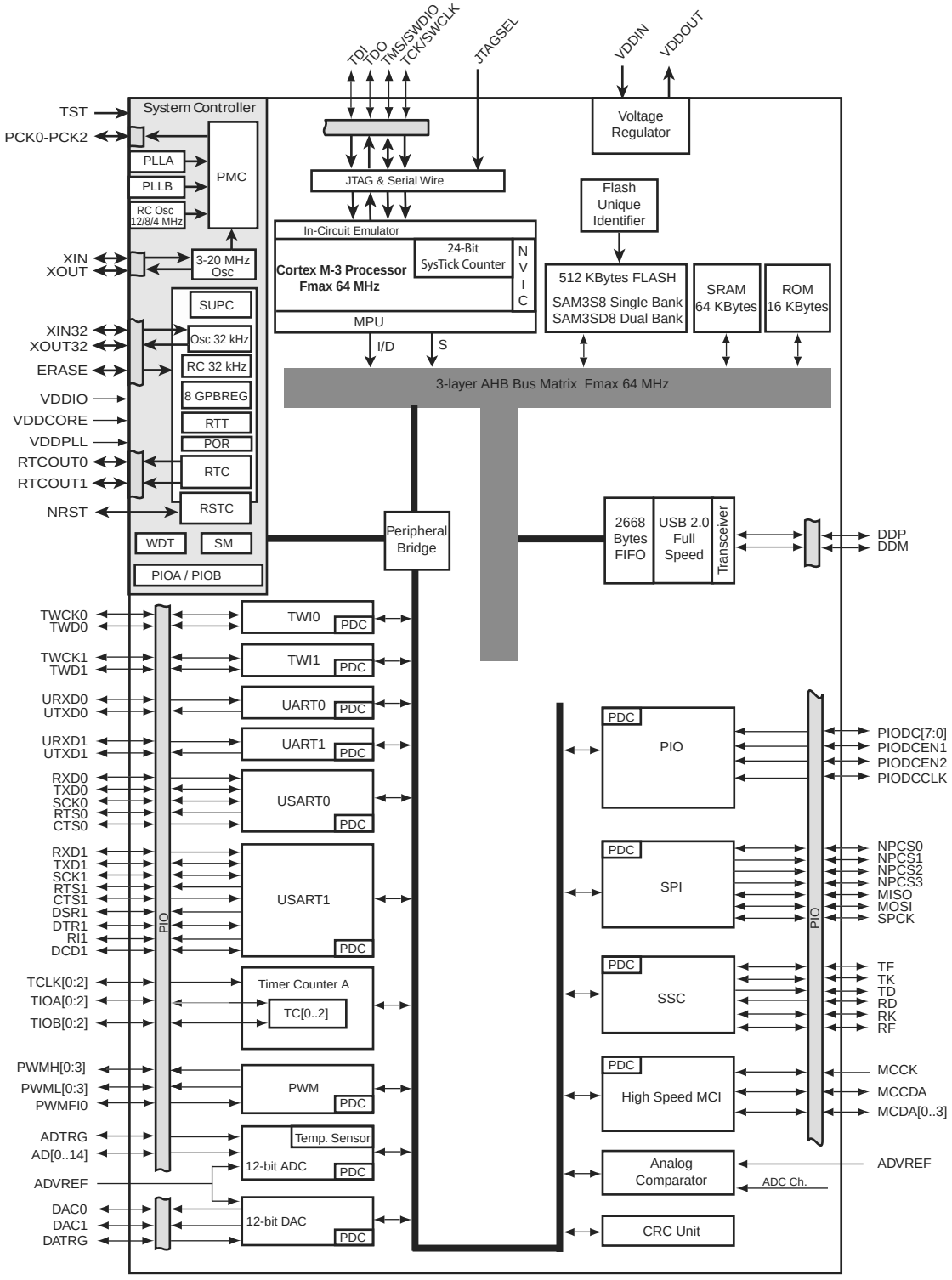


Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage reference	Comments
Universal Synchronous Asynchronous Receiver Transmitter USARTx					
SCKx	USARTx Serial Clock	I/O			
TXDx	USARTx Transmit Data	I/O			
RXDx	USARTx Receive Data	Input			
RTSx	USARTx Request To Send	Output			
CTSx	USARTx Clear To Send	Input			
DTR1	USART1 Data Terminal Ready	I/O			
DSR1	USART1 Data Set Ready	Input			
DCD1	USART1 Data Carrier Detect	Output			
RI1	USART1 Ring Indicator	Input			
Synchronous Serial Controller - SSC					
TD	SSC Transmit Data	Output			
RD	SSC Receive Data	Input			
TK	SSC Transmit Clock	I/O			
RK	SSC Receive Clock	I/O			
TF	SSC Transmit Frame Sync	I/O			
RF	SSC Receive Frame Sync	I/O			
Timer/Counter - TC					
TCLKx	TC Channel x External Clock Input	Input			
TIOAx	TC Channel x I/O Line A	I/O			
TIOBx	TC Channel x I/O Line B	I/O			
Pulse Width Modulation Controller- PWMC					
PWMHx	PWM Waveform Output High for channel x	Output			
PWMLx	PWM Waveform Output Low for channel x	Output			only output in complementary mode when dead time insertion is enabled.
PWMFI0	**PWM Fault Input**	Input			
Serial Peripheral Interface - SPI					
MISO	Master In Slave Out	I/O			
MOSI	Master Out Slave In	I/O			
SPCK	SPI Serial Clock	I/O			
SPI_NPCS0	SPI Peripheral Chip Select 0	I/O	Low		
SPI_NPCS1 - SPI_NPCS3	SPI Peripheral Chip Select	Output	Low		

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage reference	Comments
Two-Wire Interface- TWI					
TWDx	TWIx Two-wire Serial Data	I/O			
TWCKx	TWIx Two-wire Serial Clock	I/O			
Analog					
ADVREF	ADC, DAC and Analog Comparator Reference	Analog			
12-bit Analog-to-Digital Converter - ADC					
AD0-AD14	Analog Inputs	Analog, Digital			
ADTRG	ADC Trigger	Input		VDDIO	
12-bit Digital-to-Analog Converter - DAC					
DAC0 - DAC1	Analog output	Analog, Digital			
DACTRG	DAC Trigger	Input		VDDIO	
Fast Flash Programming Interface - FFPI					
PGMEN0-PGMEN2	Programming Enabling	Input		VDDIO	
PGMM0-PGMM3	Programming Mode	Input		VDDIO	
PGMD0-PGMD15	Programming Data	I/O			
PGMRDY	Programming Ready	Output	High		
PGMNVALID	Data Direction	Output	Low		
PGMNOE	Programming Read	Input	Low		
PGMCK	Programming Clock	Input			
PGMNCMD	Programming Command	Input	Low		
USB Full Speed Device					
DDM	USB Full Speed Data -	Analog, Digital		VDDIO	Reset State: - USB Mode - Internal Pull-down(3)
DDP	USB Full Speed Data +				

Note:
1. Schmitt Triggers can be disabled through PIO registers.
2. Some PIO lines are shared with System I/Os.
3. Refer to USB Section of the product Electrical Characteristics for information on Pull-down value in USB Mode.
4. See “Typical Powering Schematics” Section for restrictions on voltage range of Analog Cells.
5. TDO pin is set in input mode when the Cortex-M3 Core is not in debug mode. Thus the internal pull-up corresponding to this PIO line must be enabled to avoid current consumption due to floating input.

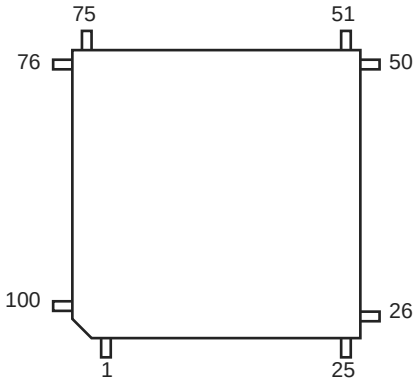
4. Package and Pinout

SAM3S8/SD8 devices are pin-to-pin compatible with AT91SAM7S legacy products for 64-pin version. Furthermore, SAM3S8/SD8 products have new functionalities referenced in italic in Table 4-1, Table 4-3.

4.1 SAM3S8C/8DC Package and Pinout

4.1.1 100-Lead LQFP Package Outline

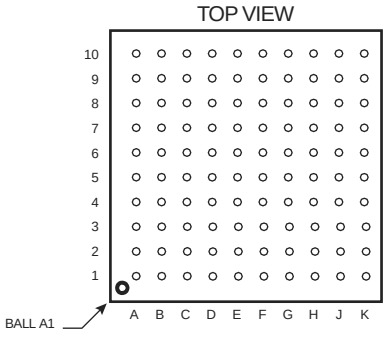
Figure 4-1. Orientation of the 100-lead LQFP Package



4.1.2 100-ball TFBGA Package Outline

The 100-Ball TFBGA package has a 0.8 mm ball pitch and respects Green Standards. Its dimensions are 9 x 9 x 1.1 mm. Figure 4-2 shows the orientation of the 100-ball TFBGA Package.

Figure 4-2. Orientation of the 100-ball TFBGA Package



4.2 SAM3S8B/D8B Package and Pinout

4.2.1 64-Lead LQFP Package Outline

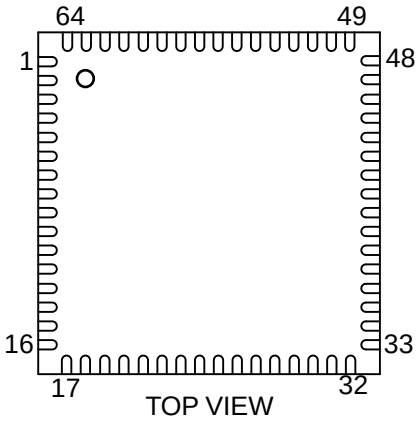
Figure 4-3. Orientation of the 64-lead LQFP Package

64

1

4.2.2 64-lead QFN Package Outline

Figure 4-4. Orientation of the 64-lead QFN Package



5. Power Considerations

5.1 Power Supplies

The SAM3S8/SD8 has several types of power supply pins:

- VDDCORE pins: Power the core, the embedded memories and the peripherals. Voltage ranges from 1.62V to 1.95V.
- VDDIO pins: Power the Peripherals I/O lines (Input/Output Buffers), USB transceiver, Backup part, 32 kHz crystal oscillator and oscillator pads. Voltage ranges from 1.62V to 3.6V.
- VDDIN pin: Voltage Regulator Input, ADC, DAC and Analog Comparator Power Supply. Voltage ranges from 1.8V to 3.6V.
- VDDPLL pin: Powers the PLLA, PLLB, the Fast RC and the 3 to 20 MHz oscillator. Voltage ranges from 1.62V to 1.95V.

5.2 Voltage Regulator

The SAM3S8/SD8 embeds a voltage regulator that is managed by the Supply Controller.

This internal regulator is designed to supply the internal core of SAM3S8/SD8. It features two operating modes:

- In Normal mode, the voltage regulator consumes less than 700 µA static current and draws 80 mA of output current. Internal adaptive biasing adjusts the regulator quiescent current depending on the required load current. In Wait Mode quiescent current is only 7 µA.
- In Backup mode, the voltage regulator consumes less than 1 µA while its output (VDDOUT) is driven internally to GND. The default output voltage is 1.80V and the start-up time to reach Normal mode is less than 100 µs.

For adequate input and output power supply decoupling/bypassing, refer to the “Voltage Regulator” section in the “Electrical Characteristics” section of the datasheet.

5.3 Typical Powering Schematics

The SAM3S8/SD8 supports a 1.62V-3.6V single supply mode. The internal regulator input connected to the source and its output feeds VDDCORE. Figure 5-1 below shows the power schematics.

As VDDIN powers the voltage regulator, the ADC, DAC and the analog comparator, when the user does not want to use the embedded voltage regulator, it can be disabled by software via the SUPC (note that this is different from Backup mode).

- Supply Monitor alarm
- RTC alarm
- RTT alarm

5.5.2 Wait Mode

The purpose of the wait mode is to achieve very low power consumption while maintaining the whole device in a powered state for a startup time of less than 10 µs. Current Consumption in Wait mode is typically 15 µA (total current consumption) if the internal voltage regulator is used or 8 µA if an external regulator is used.

In this mode, the clocks of the core, peripherals and memories are stopped. However, the core, peripherals and memories power supplies are still powered. From this mode, a fast start up is available.

This mode is entered via Wait for Event (WFE) instructions with LPM = 1 (Low Power Mode bit in PMC_FSMR). The Cortex-M3 is able to handle external events or internal events in order to wake-up the core (WFE). This is done by configuring the external lines WUP0-15 as fast startup wake-up pins (refer to Section 5.7 “Fast Startup”). RTC or RTT Alarm and USB wake-up events can be used to wake up the CPU (exit from WFE).

Entering Wait Mode:

- Select the 4/8/12 MHz fast RC oscillator as Main Clock
- Set the LPM bit in the PMC Fast Startup Mode Register (PMC_FSMR)
- Execute the Wait-For-Event (WFE) instruction of the processor

Note: Internal Main clock resynchronization cycles are necessary between the writing of MOSCRCEN bit and the effective entry in Wait mode. Depending on the user application, waiting for MOSCRCEN bit to be cleared is recommended to ensure that the core will not execute undesired instructions.

5.5.3 Sleep Mode

The purpose of sleep mode is to optimize power consumption of the device versus response time. In this mode, only the core clock is stopped. The peripheral clocks can be enabled. The current consumption in this mode is application dependent.

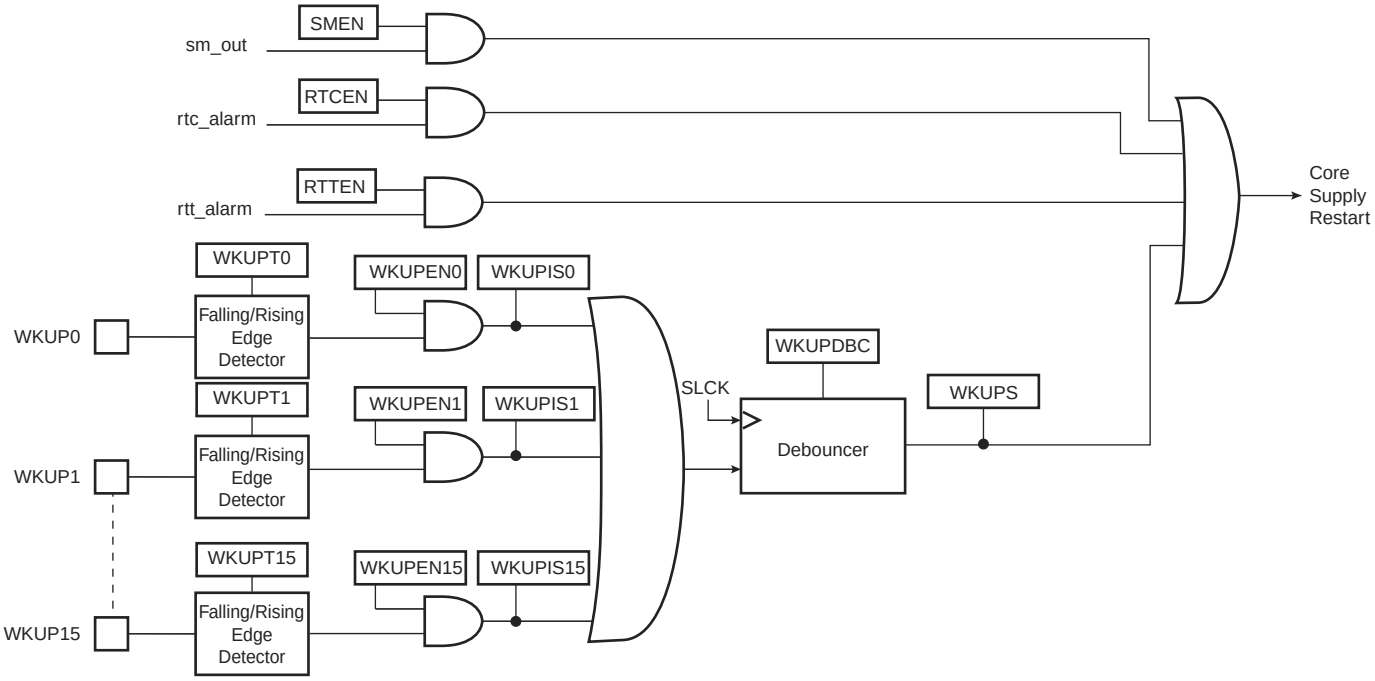
This mode is entered via Wait for Interrupt (WFI) or Wait for Event (WFE) instructions with LPM = 0 in PMC_FSMR.

The processor can be awakened from an interrupt if WFI instruction of the Cortex M3 is used, or from an event if the WFE instruction is used to enter this mode.

5.6 Wake-up Sources

The wake-up events allow the device to exit the backup mode. When a wake-up event is detected, the Supply Controller performs a sequence which automatically reenables the core power supply and the SRAM power supply, if they are not already enabled.

Figure 5-4. Wake-up Source



6.3 Test Pin

The TST pin is used for JTAG Boundary Scan Manufacturing Test or Fast Flash programming mode of the SAM3S8/SD8 series. The TST pin integrates a permanent pull-down resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations. To enter fast programming mode, see the Fast Flash Programming Interface (FFPI) section. For more on the manufacturing and test mode, refer to the “Debug and Test” section of the product datasheet.

6.4 NRST Pin

The NRST pin is bidirectional. It is handled by the on-chip reset controller and can be driven low to provide a reset signal to the external components or asserted low externally to reset the microcontroller. It will reset the Core and the peripherals except the Backup region (RTC, RTT and Supply Controller). There is no constraint on the length of the reset pulse and the reset controller can guarantee a minimum pulse length. The NRST pin integrates a permanent pull-up resistor to VDDIO of about 100 kΩ. By default, the NRST pin is configured as an input.

6.5 ERASE Pin

The ERASE pin is used to reinitialize the Flash content (and some of its NVM bits) to an erased state (all bits read as logic level 1). It integrates a pull-down resistor of about 100 kΩ to GND, so that it can be left unconnected for normal operations.

This pin is debounced by SCLK to improve the glitch tolerance. When the ERASE pin is tied high during less than 100 ms, it is not taken into account. The pin must be tied high during more than 220 ms to perform a Flash erase operation.

The ERASE pin is a system I/O pin and can be used as a standard I/O. At startup, the ERASE pin is not configured as a PIO pin. If the ERASE pin is used as a standard I/O, startup level of this pin must be low to prevent unwanted erasing. Refer to Section 10.17 “Peripheral Signal Multiplexing on I/O Lines” on page 40. Also, if the ERASE pin is used as a standard I/O output, asserting the pin to low does not erase the Flash.

7. Processor and Architecture

7.1 ARM Cortex-M3 Processor

- Version 2.0
- Thumb-2 (ISA) subset consisting of all base Thumb-2 instructions, 16-bit and 32-bit.
- Harvard processor architecture enabling simultaneous instruction fetch with data load/store.
- Three-stage pipeline.
- Single cycle 32-bit multiply.
- Hardware divide.
- Thumb and Debug states.
- Handler and Thread modes.
- Low latency ISR entry and exit.

7.2 APB/AHB bridge

The SAM3S8/SD8 embeds One Peripheral bridge:

The peripherals of the bridge are clocked by MCK.

7.3 Matrix Masters

The Bus Matrix of the SAM3S8/SD8 manages 4 masters, which means that each master can perform an access concurrently with others, to an available slave.

Each master has its own decoder, which is defined specifically for each master. In order to simplify the addressing, all the masters have the same decodings.

Table 7-1. List of Bus Matrix Masters

Master 0	Cortex-M3 Instruction/Data
Master 1	Cortex-M3 System
Master 2	Peripheral DMA Controller (PDC)
Master 3	CRC Calculation Unit

7.4 Matrix Slaves

The Bus Matrix of the SAM3S8/SD8 manages 5 slaves. Each slave has its own arbiter, allowing a different arbitration per slave.

Table 7-2. List of Bus Matrix Slaves

Slave 0	Internal SRAM
Slave 1	Internal ROM
Slave 2	Internal Flash
Slave 3	External Bus Interface
Slave 4	Peripheral Bridge

7.5 Master to Slave Access

All the Masters can normally access all the Slaves. However, some paths do not make sense, for example allowing access from the Cortex-M3 S Bus to the Internal ROM. Thus, these paths are forbidden or simply not wired, and shown as “-” in the following table.

Table 7-3. SAM3S8_SD8 Master to Slave Access

Slaves	Masters	0	1	2	3
		Cortex-M3 I/D Bus	Cortex-M3 S Bus	PDC	CRCCU
0	Internal SRAM	-	X	X	X
1	Internal ROM	X	-	X	X
2	Internal Flash	X	-	-	X
3	External Bus Interface	-	X	X	X
4	Peripheral Bridge	-	X	X	-

7.6 Peripheral DMA Controller

- Handles data transfer between peripherals and memories
- Low bus arbitration overhead
  - One Master Clock cycle needed for a transfer from memory to peripheral
  - Two Master Clock cycles needed for a transfer from peripheral to memory
- Next Pointer management for reducing interrupt latency requirement

The Peripheral DMA Controller handles transfer requests from the channel according to the following priorities (Low to High priorities):

Table 7-4. Peripheral DMA Controller

Instance name	Channel T/R
USART2	Transmit
USART2	Receive
PWM	Transmit
TWI1	Transmit
TWI0	Transmit
UART1	Transmit
UART0	Transmit
USART1	Transmit
USART0	Transmit
DACC	Transmit
SPI	Transmit

The reset circuitry is based on a zero-power power-on reset cell and a brownout detector cell. The zero-power power-on reset allows the Supply Controller to start properly, while the software-programmable brownout detector allows detection of either a battery discharge or main voltage loss.

The Slow Clock generator is based on a 32 kHz crystal oscillator and an embedded 32 kHz RC oscillator. The Slow Clock defaults to the RC oscillator, but the software can enable the crystal oscillator and select it as the Slow Clock source.

The Supply Controller starts up the device by sequentially enabling the internal power switches and the Voltage Regulator, then it generates the proper reset signals to the core power supply.

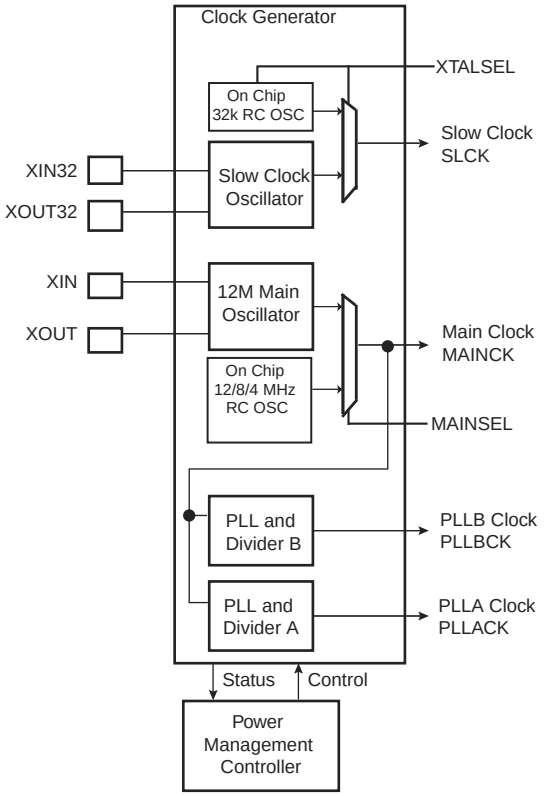
It also enables to set the system in different low-power modes and to wake it up from a wide range of events.

10.5 Clock Generator

The Clock Generator is made up of:

- One Low-power 32768Hz Slow Clock Oscillator with bypass mode
- One Low-power RC Oscillator
- One 3-20 MHz Crystal Oscillator, which can be bypassed
- One Fast RC Oscillator, factory programmed. Three output frequencies can be selected: 4, 8 or 12 MHz. By default 4 MHz is selected.
- One 60 to 130 MHz PLL (PLLB) providing a clock for the USB Full Speed Controller
- One 60 to 130 MHz programmable PLL (PLLA), provides the clock, MCK to the processor and peripherals. The PLLA input frequency is from 3.5 MHz to 20 MHz.

Figure 10-2. Clock Generator Block Diagram



10.6 Power Management Controller

The Power Management Controller provides all the clock signals to the system. It provides:

- the Processor Clock, HCLK
- the Free running processor clock, FCLK
- the Cortex SysTick external clock
- the Master Clock, MCK, in particular to the Matrix and the memory interfaces
- the USB Clock, UDPCK
- independent peripheral clocks, typically at the frequency of MCK
- three programmable clock outputs: PCK0, PCK1 and PCK2

The Supply Controller selects between the 32 kHz RC oscillator or the crystal oscillator. The unused oscillator is disabled automatically so that power consumption is optimized.

By default, at startup the chip runs out of the Master Clock using the fast RC oscillator running at 4 MHz.

The user can trim the 8 and 12 MHz RC Oscillator frequency by software.

10.13 Chip Identification

- Chip Identifier (CHIPID) registers permit recognition of the device and its revision.

Table 10-1. SAM3S8/SD8 Hip IDs Register

Chip Name	Flash Size (KBytes)	Pin Count	CHIPID_CIDR	CHIPID_EXID
SAM3S8B (Rev A)	512	64	0x289B0A60	0x0
SAM3S8C (Rev A)	512	100	0x28AB0A60	0x0
SAM3SD8B (Rev A)	512	64	0x299B0A60	0x0
SAM3SD8C (Rev A)	512	100	0x29AB0A60	0x0

- JTAG ID: 0x05B2D03F

10.14 UART

- Two-pin UART
  - Implemented features are 100% compatible with the standard Atmel USART
  - Independent receiver and transmitter with a common programmable Baud Rate Generator
  - Even, Odd, Mark or Space Parity Generation
  - Parity, Framing and Overrun Error Detection
  - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
  - Support for two PDC channels with connection to receiver and transmitter

10.15 PIO Controllers

- 3 PIO Controllers, PIOA, PIOB and PIOC (100-pin version only) controlling a maximum of 79 I/O Lines
- Each PIO Controller controls up to 32 programmable I/O Lines
- Fully programmable through Set/Clear Registers

Table 10-2. PIO available according to pin count

Version	64 pin	100 pin
PIOA	32	32
PIOB	15	15
PIOC	-	32

- Multiplexing of four peripheral functions per I/O Line
- For each I/O Line (whether assigned to a peripheral or used as general purpose I/O)
  - Input change interrupt
  - Programmable Glitch filter
  - Programmable debouncing filter
  - Multi-drive option enables driving in open drain
  - Programmable pull-up on each I/O line
  - Pin data status register, supplies visibility of the level on the pin at any time
  - Additional interrupt modes on a programmable event: rising edge, falling edge, low level or high level

10.17.1 PIO Controller A Multiplexing

Table 10-4. Multiplexing on PIO Controller A (PIOA)

I/O Line	Peripheral A	Peripheral B	Peripheral C	Peripheral D	Extra Function	System Function	Comments
PA0	PWMH0	TIOA0	A17		WKUP0		
PA1	PWMH1	TIOB0	A18		WKUP1		
PA2	PWMH2	SCK0	DATRG		WKUP2		
PA3	TWD0	NPCS3					
PA4	TWCK0	TCLK0			WKUP3		
PA5	RXD0	NPCS3			WKUP4		
PA6	TXD0	PCK0					
PA7	RTS0	PWMH3				XIN32	
PA8	CTS0	ADTRG			WKUP5	XOUT32	
PA9	URXD0	NPCS1	PWMFI0		WKUP6		
PA10	UTXD0	NPCS2					
PA11	NPCS0	PWMH0			WKUP7		
PA12	MISO	PWMH1					
PA13	MOSI	PWMH2					
PA14	SPCK	PWMH3			WKUP8		
PA15	TF	TIOA1	PWML3	PIODCEN1	WKUP14		
PA16	TK	TIOB1	PWML2	PIODCEN2	WKUP15		
PA17	TD	PCK1	PWMH3		AD0		
PA18	RD	PCK2	A14		AD1		
PA19	RK	PWML0	A15		AD2/WKUP9		
PA20	RF	PWML1	A16		AD3/WKUP10		
PA21	RXD1	PCK1			AD8		64/100 pins versions
PA22	TXD1	NPCS3	NCS2		AD9		64/100 pins versions
PA23	SCK1	PWMH0	*A19*	PIODCCLK			64/100 pins versions
PA24	RTS1	PWMH1	*A20*	PIODC0			64/100 pins versions
PA25	CTS1	PWMH2	A23	PIODC1			64/100 pins versions
PA26	DCD1	TIOA2	MCDA2	PIODC2			64/100 pins versions
PA27	DTR1	TIOB2	MCDA3	PIODC3			64/100 pins versions
PA28	DSR1	TCLK1	MCCDA	PIODC4			64/100 pins versions
PA29	RI1	TCLK2	MCCK	PIODC5			64/100 pins versions
PA30	PWML2	NPCS2	MCDA0	PIODC6	WKUP11		64/100 pins versions
PA31	NPCS1	PCK2	MCDA1	PIODC7			64/100 pins versions

10.17.2 PIO Controller B Multiplexing

Table 10-5. Multiplexing on PIO Controller B (PIOB)

I/O Line	Peripheral A	Peripheral B	Peripheral C	Extra Function	System Function	Comments
PB0	PWMH0			AD4/RTCOUT0		
PB1	PWMH1			AD5/RTCOUT1		
PB2	URXD1	NPCS2		AD6/WKUP12		
PB3	UTXD1	PCK2		AD7		
PB4	TWD1	PWMH2			TDI	
PB5	TWCK1	PWML0		WKUP13	TDO/TRACESWO	
PB6					TMS/SWDIO	
PB7					TCK/SWCLK	
PB8					XOUT	
PB9					XIN	
PB10					DDM	
PB11					DDP	
PB12	PWML1				ERASE	
PB13	PWML2	PCK0		DAC0		64/00 pins versions
PB14	NPCS1	PWMH3		DAC1		64/100 pins versions

10.17.3 PIO Controller C Multiplexing

Table 10-6. Multiplexing on PIO Controller C (PIOC)

I/O Line	Peripheral A	Peripheral B	Peripheral C	Extra Function	System Function	Comments
PC0	D0	PWML0				100 pin version
PC1	D1	PWML1				100 pin version
PC2	D2	PWML2				100 pin version
PC3	D3	PWML3				100 pin version
PC4	D4	NPCS1				100 pin version
PC5	D5					100 pin version
PC6	D6					100 pin version
PC7	D7					100 pin version
PC8	NWE					100 pin version
PC9	NANDOE	RXD2(1)				100 pin version
PC10	NANDWE	TXD2(1)				100 pin version
PC11	NRD					100 pin version
PC12	NCS3			AD12		100 pin version
PC13	NWAIT	PWML0		AD10		100 pin version
PC14	NCS0	SCK2(1)				100 pin version
PC15	NCS1	PWML1		AD11		100 pin version
PC16	A21/NANDALE	RTS2(1)				100 pin version
PC17	A22/NANDCLE	CTS2(1)				100 pin version
PC18	A0	PWMH0				100 pin version
PC19	A1	PWMH1				100 pin version
PC20	A2	PWMH2				100 pin version
PC21	A3	PWMH3				100 pin version
PC22	A4	PWML3				100 pin version
PC23	A5	TIOA3				100 pin version
PC24	A6	TIOB3				100 pin version
PC25	A7	TCLK3				100 pin version
PC26	A8	TIOA4				100 pin version
PC27	A9	TIOB4				100 pin version
PC28	A10	TCLK4				100 pin version
PC29	A11	TIOA5		AD13		100 pin version
PC30	A12	TIOB5		AD14		100 pin version
PC31	A13	TCLK5				100 pin version

Note: 1. USART2 only on SAM3SD8 in 100 pin package.

11. Embedded Peripherals Overview

11.1 Serial Peripheral Interface (SPI)

- Supports communication with serial external devices
  - Four chip selects with external decoder support allow communication with up to 15 peripherals
  - Serial memories, such as DataFlash® and 3-wire EEPROMs
  - Serial peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
  - External co-processors
- Master or slave serial peripheral bus interface
  - 8- to 16-bit programmable data length per chip select
  - Programmable phase and polarity per chip select
  - Programmable transfer delays between consecutive transfers and between clock and data per chip select
  - Programmable delay between consecutive transfers
  - Selectable mode fault detection
- Connection to PDC channel capabilities optimizes data transfers
  - One channel for the receiver, one channel for the transmitter
  - Next buffer support

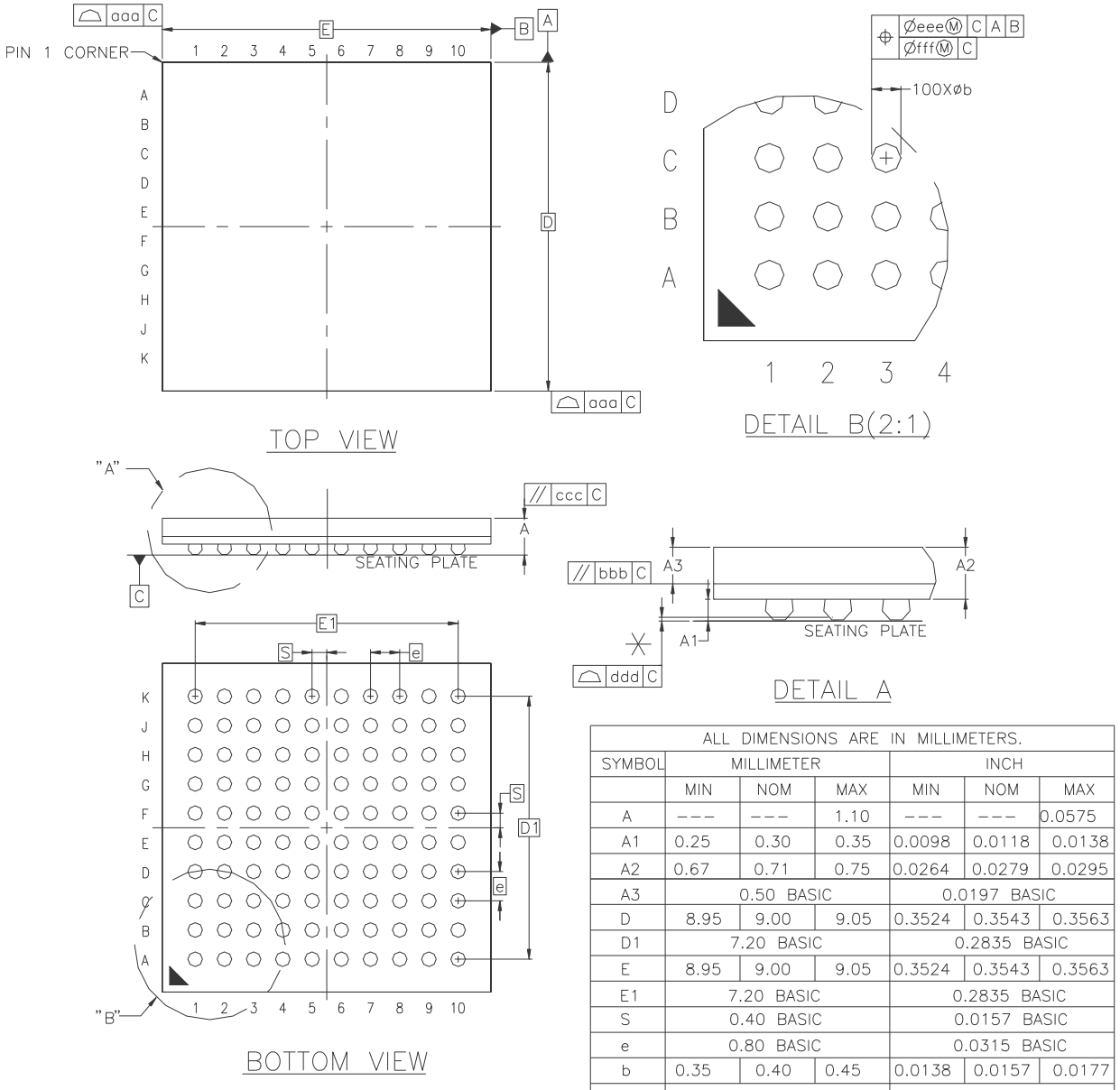
11.2 Two Wire Interface (TWI)

- Master, Multi-Master and Slave Mode Operation
- Compatibility with Atmel two-wire interface, serial memory and I^2C compatible devices
- One, two or three bytes for slave address
- Sequential read/write operations
- Bit Rate: Up to 400 kbit/s
- General Call Supported in Slave Mode
- Connecting to PDC channel capabilities optimizes data transfers in Master Mode only
  - One channel for the receiver, one channel for the transmitter
  - Next buffer support

11.3 Universal Asynchronous Receiver Transceiver (UART)

- Two-pin UART
  - Independent receiver and transmitter with a common programmable Baud Rate Generator
  - Even, Odd, Mark or Space Parity Generation
  - Parity, Framing and Overrun Error Detection
  - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
  - Support for two PDC channels with connection to receiver and transmitter

Figure 12-2. 100-ball TFBGA Package Mechanical Drawing



ALL DIMENSIONS ARE IN MILLIMETERS.						
SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	0.0575
A1	0.25	0.30	0.35	0.0098	0.0118	0.0138
A2	0.67	0.71	0.75	0.0264	0.0279	0.0295
A3	0.50 BASIC			0.0197 BASIC		
D	8.95	9.00	9.05	0.3524	0.3543	0.3563
D1	7.20 BASIC			0.2835 BASIC		
E	8.95	9.00	9.05	0.3524	0.3543	0.3563
E1	7.20 BASIC			0.2835 BASIC		
S	0.40 BASIC			0.0157 BASIC		
e	0.80 BASIC			0.0315 BASIC		
b	0.35	0.40	0.45	0.0138	0.0157	0.0177
aaa	0.15			0.0059		
bbb	0.20			0.0079		
ccc	0.20			0.0079		
ddd	0.12			0.0047		
eee	0.15			0.0059		
fff	0.08			0.0031		

Figure 12-3. 64-lead LQFP Package Mechanical Drawing

Table 12-1. 64-lead LQFP Package Dimensions (in mm)

Symbol	Millimeter			Inch		
	Min	**Nom**	**Max**	**Min**	**Nom**	**Max**
A	–	–	1.60	–	–	0.063
A1	0.05	–	0.15	0.002	–	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	12.00 BSC			0.472 BSC		
D1	10.00 BSC			0.383 BSC		
E	12.00 BSC			0.472 BSC		
E1	10.00 BSC			0.383 BSC		
R2	0.08	–	0.20	0.003	–	0.008
R1	0.08	–	–	0.003	–	–
q	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	–	–	0°	–	–
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°
c	0.09	–	0.20	0.004	–	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		