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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	EBI/EMI, I²C, IrDA, Memory Card, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	79
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 15x10/12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam3s8ca-au

1. Description

The Atmel SAM3S8/SD8 series is a member of a family of Flash microcontrollers based on the high performance 32-bit ARM Cortex-M3 RISC processor. It operates at a maximum speed of 64 MHz and features up to 512 Kbytes of Flash (dual plane on SAM3SD8) and up to 64 Kbytes of SRAM. The peripheral set includes a Full Speed USB Device port with embedded transceiver, a High Speed MCI for SDIO/SD/MMC, an External Bus Interface featuring a Static Memory Controller providing connection to SRAM, PSRAM, NOR Flash, LCD Module and NAND Flash, 2(3)x USARTs, (3 on SAM3SD8C) 2x UARTs, 2x TWIs, 3x SPI, an I2S, as well as 1 PWM timer, 6x general-purpose 16-bit timers (with stepper motor and quadrature decoder logic support), an RTC, a 12-bit ADC, a 12-bit DAC and an analog comparator.

The SAM3S8/SD8 series is ready for capacitive touch thanks to the QTouch® library, offering an easy way to implement buttons, wheels and sliders.

The SAM3S8/SD8 device is a medium range general purpose microcontroller with the best ratio in terms of reduced power consumption, processing power and peripheral set. This enables the SAM3S8/SD8 to sustain a wide range of applications including consumer, industrial control, and PC peripherals.

It operates from 1.62V to 3.6V and is available in 64- and 100-pin QFP, 64-pin QFN, and 100-pin BGA packages.

The SAM3S8/SD8 series is the ideal migration path from the SAM7S series for applications that require more performance. The SAM3S8/SD8 series is pin-to-pin compatible with the SAM7S series.

1.1 Configuration Summary

The SAM3S8/SD8 series devices differ in memory size, package and features. Table 1-1 summarizes the configurations of the device family.

Table 1-1. Configuration Summary

Feature	SAM3S8B	SAM3S8C	SAM3SD8B	SAM3SD8C
Flash	512 Kbytes	512 Kbytes	512 Kbytes	512 Kbytes
SRAM	64 Kbytes	64 Kbytes	64 Kbytes	64 Kbytes
Package	LQFP64 QFN64	LQFP100 BGA100	LQFP64 QFN64	LQFP100 BGA100
Number of PIOs	47	79	47	79
12-bit ADC	11 channels(2)	16 channels(2)	11 channels(2)	16 channels(2)
12-bit DAC	2 channels	2 channels	2 channels	2 channels
Timer Counter Channels	6	6	6	6
PDC Channels	22	22	24	24
USART/UART	2/2(1)	2/2(1)	2/2(1)	3/2(1)
HSMCI	1 port/4 bits	1 port/4 bits	1 port/4 bits	1 port/4 bits
External Bus Interface	-	8-bit data, 4 chip selects, 24-bit address	-	8-bit data, 4 chip selects, 24-bit address

Notes: 1. Full Modem support on USART1.
2. One channel is reserved for internal temperature sensor.

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage reference	Comments
Universal Synchronous Asynchronous Receiver Transmitter USARTx					
SCKx	USARTx Serial Clock	I/O			
TXDx	USARTx Transmit Data	I/O			
RXDx	USARTx Receive Data	Input			
RTSx	USARTx Request To Send	Output			
CTSx	USARTx Clear To Send	Input			
DTR1	USART1 Data Terminal Ready	I/O			
DSR1	USART1 Data Set Ready	Input			
DCD1	USART1 Data Carrier Detect	Output			
RI1	USART1 Ring Indicator	Input			
Synchronous Serial Controller - SSC					
TD	SSC Transmit Data	Output			
RD	SSC Receive Data	Input			
TK	SSC Transmit Clock	I/O			
RK	SSC Receive Clock	I/O			
TF	SSC Transmit Frame Sync	I/O			
RF	SSC Receive Frame Sync	I/O			
Timer/Counter - TC					
TCLKx	TC Channel x External Clock Input	Input			
TIOAx	TC Channel x I/O Line A	I/O			
TIOBx	TC Channel x I/O Line B	I/O			
Pulse Width Modulation Controller- PWMC					
PWMHx	PWM Waveform Output High for channel x	Output			
PWMLx	PWM Waveform Output Low for channel x	Output			only output in complementary mode when dead time insertion is enabled.
PWMFI0	**PWM Fault Input**	Input			
Serial Peripheral Interface - SPI					
MISO	Master In Slave Out	I/O			
MOSI	Master Out Slave In	I/O			
SPCK	SPI Serial Clock	I/O			
SPI_NPCS0	SPI Peripheral Chip Select 0	I/O	Low		
SPI_NPCS1 - SPI_NPCS3	SPI Peripheral Chip Select	Output	Low		

4.1.3 100-Lead LQFP Pinout

Table 4-1. SAM3S8C/SD8C 100-lead LQFP pinout

1	ADVREF	26	GND	51	TDI/PB4	76	TDO/TRACESWO/ PB5
2	GND	27	VDDIO	52	PA6/PGMNOE	77	JTAGSEL
3	PB0/AD4	28	PA16/PGMD4	53	PA5/PGMRDY	78	PC18
4	PC29/AD13	29	PC7	54	PC28	79	TMS/SWDIO/PB6
5	PB1/AD5	30	PA15/PGMD3	55	PA4/PGMNCMD	80	PC19
6	PC30/AD14	31	PA14/PGMD2	56	VDDCORE	81	PA31
7	PB2/AD6	32	PC6	57	PA27/PGMD15	82	PC20
8	PC31	33	PA13/PGMD1	58	PC8	83	TCK/SWCLK/PB7
9	PB3/AD7	34	PA24/PGMD12	59	PA28	84	PC21
10	VDDIN	35	PC5	60	NRST	85	VDDCORE
11	VDDOUT	36	VDDCORE	61	TST	86	PC22
12	PA17/PGMD5/AD0	37	PC4	62	PC9	87	ERASE/PB12
13	PC26	38	PA25/PGMD13	63	PA29	88	DDM/PB10
14	PA18/PGMD6/AD1	39	PA26/PGMD14	64	PA30	89	DDP/PB11
15	PA21/PGMD9/AD8	40	PC3	65	PC10	90	PC23
16	VDDCORE	41	PA12/PGMD0	66	PA3	91	VDDIO
17	PC27	42	PA11/PGMM3	67	PA2/PGMEN2	92	PC24
18	PA19/PGMD7/AD2	43	PC2	68	PC11	93	PB13/DAC0
19	PC15/AD11	44	PA10/PGMM2	69	VDDIO	94	PC25
20	PA22/PGMD10/AD 9	45	GND	70	GND	95	GND
21	PC13/AD10	46	PA9/PGMM1	71	PC14	96	PB8/XOUT
22	PA23/PGMD11	47	PC1	72	PA1/PGMEN1	97	PB9/*PGMCK/XIN*
23	PC12/AD12	48	PA8/XOUT32/ PGMM0	73	PC16	98	VDDIO
24	PA20/PGMD8/AD3	49	PA7/XIN32/ PGMNVALID	74	PA0/PGMEN0	99	PB14/DAC1
25	PC0	50	VDDIO	75	PC17	100	VDDPLL

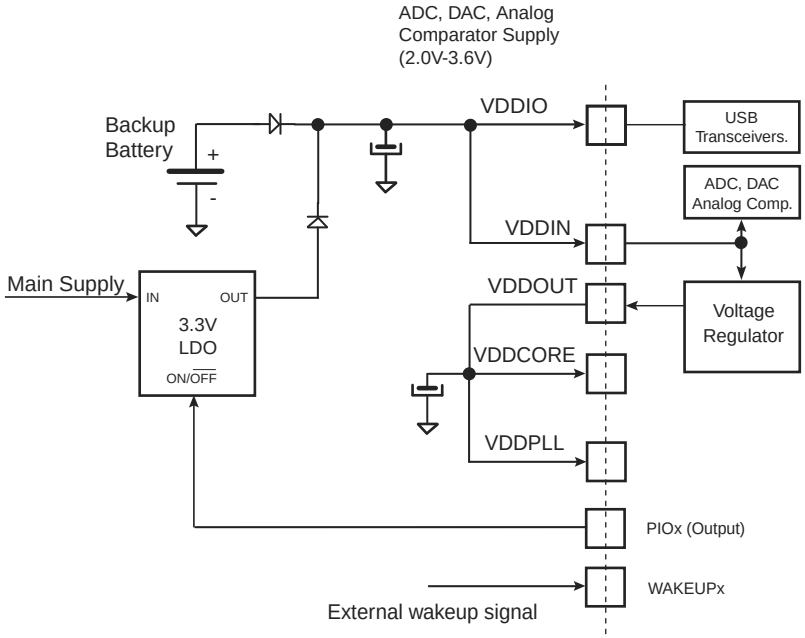
4.2.3 64-Lead LQFP and QFN Pinout

Table 4-3. 64-pin SAM3S8B/D8B pinout

1	ADVREF	17	GND	33	TDI/PB4	49	TDO/TRACESWO/ PB5
2	GND	18	VDDIO	34	PA6/PGMNOE	50	JTAGSEL
3	PB0/AD4	19	PA16/PGMD4	35	PA5/PGMRDY	51	TMS/SWDIO/PB6
4	PB1/AD5	20	PA15/PGMD3	36	PA4/PGMNCMD	52	PA31
5	PB2/AD6	21	PA14/PGMD2	37	PA27/PGMD15	53	TCK/SWCLK/PB7
6	PB3/AD7	22	PA13/PGMD1	38	PA28	54	VDDCORE
7	VDDIN	23	PA24/PGMD12	39	NRST	55	ERASE/PB12
8	VDDOUT	24	VDDCORE	40	TST	56	DDM/PB10
9	PA17/PGMD5/ AD*0*	25	PA25/PGMD13	41	PA29	57	DDP/PB11
10	PA18/PGMD6/ AD1	26	PA26/PGMD14	42	PA30	58	VDDIO
11	PA21/PGMD9/ AD8	27	PA12/PGMD0	43	PA3	59	PB13/DAC0
12	VDDCORE	28	PA11/PGMM3	44	PA2/PGMEN2	60	GND
13	PA19/PGMD7/ AD2	29	PA10/PGMM2	45	VDDIO	61	XOUT/PB8
14	PA22/PGMD10/ AD9	30	PA9/PGMM1	46	GND	62	XIN/PGMCK/PB9
15	PA23/PGMD11	31	PA8/*XOUT32*/ PGMM0	47	PA1/PGMEN1	63	PB14/DAC1
16	PA20/PGMD8/ AD3	32	PA7/*XIN32*/ PGMNVALID	48	PA0/PGMEN0	64	VDDPLL

Note: The bottom pad of the QFN package must be connected to ground.

Figure 5-3. Backup Battery



Note: The two diodes provide a "switchover circuit" (for illustration purpose) between the backup battery and the main supply when the system is put in backup mode.

5.4 Active Mode

Active mode is the normal running mode with the core clock running from the fast RC oscillator, the main crystal oscillator or the PLLA. The power management controller can be used to adapt the frequency and to disable the peripheral clocks.

5.5 Low-power Modes

The various low-power modes of the SAM3S8/SD8 are described below:

5.5.1 Backup Mode

The purpose of backup mode is to achieve the lowest power consumption possible in a system which is performing periodic wake-ups to perform tasks but not requiring fast startup time (<0.1ms). Total current consumption is 1.5 µA typical.

The Supply Controller, zero-power power-on reset, RTT, RTC, Backup registers and 32 kHz oscillator (RC or crystal oscillator selected by software in the Supply Controller) are running. The regulator and the core supply are off.

Backup mode is based on the Cortex-M3 deep sleep mode with the voltage regulator disabled.

The SAM3S8/SD8 can be awakened from this mode through WUP0-15 pins, the supply monitor (SM), the RTT or RTC wake-up event.

Backup mode is entered by using WFE instructions with the SLEEPDEEP bit in the Cortex-M3 System Control Register set to 1. (See the Power management description in The ARM Cortex-M3 Processor section of the product datasheet).

Exit from Backup mode happens if one of the following enable wake up events occurs:

- WKUPEN0-15 pins (level transition, configurable debouncing)

- Supply Monitor alarm
- RTC alarm
- RTT alarm

5.5.2 Wait Mode

The purpose of the wait mode is to achieve very low power consumption while maintaining the whole device in a powered state for a startup time of less than 10 µs. Current Consumption in Wait mode is typically 15 µA (total current consumption) if the internal voltage regulator is used or 8 µA if an external regulator is used.

In this mode, the clocks of the core, peripherals and memories are stopped. However, the core, peripherals and memories power supplies are still powered. From this mode, a fast start up is available.

This mode is entered via Wait for Event (WFE) instructions with LPM = 1 (Low Power Mode bit in PMC_FSMR). The Cortex-M3 is able to handle external events or internal events in order to wake-up the core (WFE). This is done by configuring the external lines WUP0-15 as fast startup wake-up pins (refer to Section 5.7 “Fast Startup”). RTC or RTT Alarm and USB wake-up events can be used to wake up the CPU (exit from WFE).

Entering Wait Mode:

- Select the 4/8/12 MHz fast RC oscillator as Main Clock
- Set the LPM bit in the PMC Fast Startup Mode Register (PMC_FSMR)
- Execute the Wait-For-Event (WFE) instruction of the processor

Note: Internal Main clock resynchronization cycles are necessary between the writing of MOSCRCEN bit and the effective entry in Wait mode. Depending on the user application, waiting for MOSCRCEN bit to be cleared is recommended to ensure that the core will not execute undesired instructions.

5.5.3 Sleep Mode

The purpose of sleep mode is to optimize power consumption of the device versus response time. In this mode, only the core clock is stopped. The peripheral clocks can be enabled. The current consumption in this mode is application dependent.

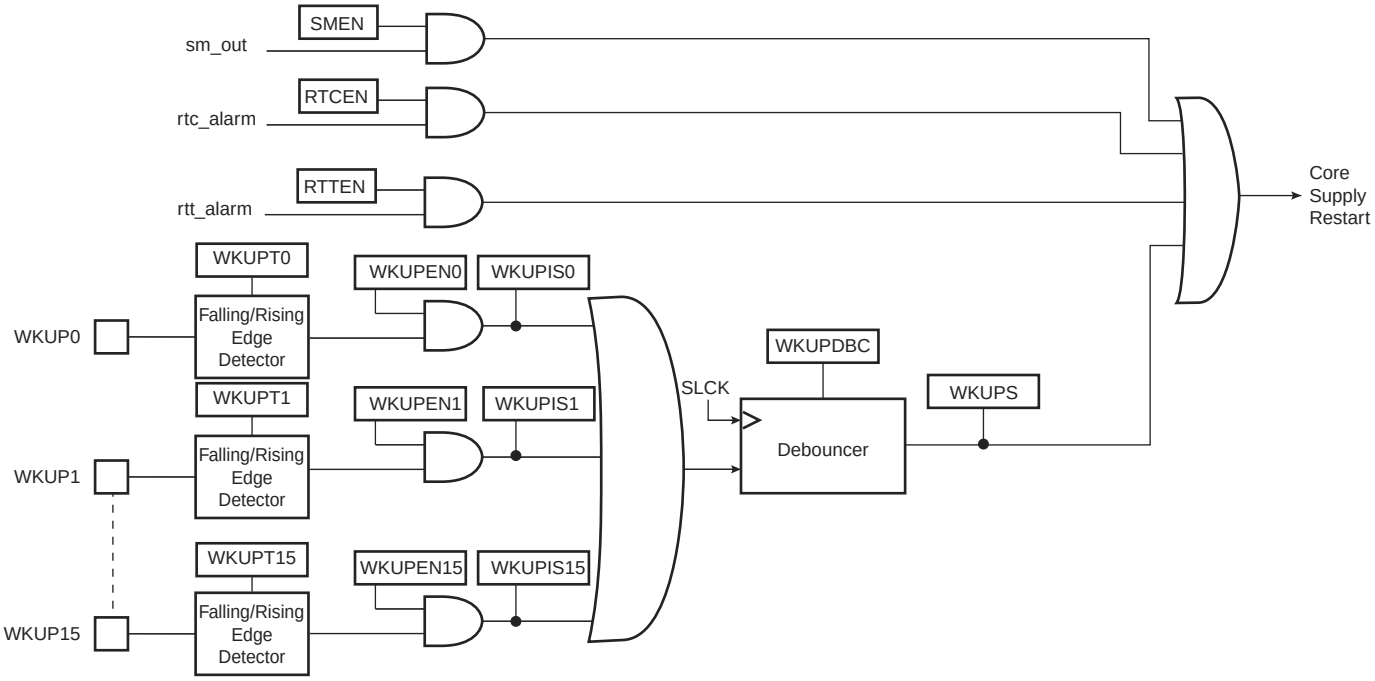
This mode is entered via Wait for Interrupt (WFI) or Wait for Event (WFE) instructions with LPM = 0 in PMC_FSMR.

The processor can be awakened from an interrupt if WFI instruction of the Cortex M3 is used, or from an event if the WFE instruction is used to enter this mode.

5.6 Wake-up Sources

The wake-up events allow the device to exit the backup mode. When a wake-up event is detected, the Supply Controller performs a sequence which automatically reenables the core power supply and the SRAM power supply, if they are not already enabled.

Figure 5-4. Wake-up Source

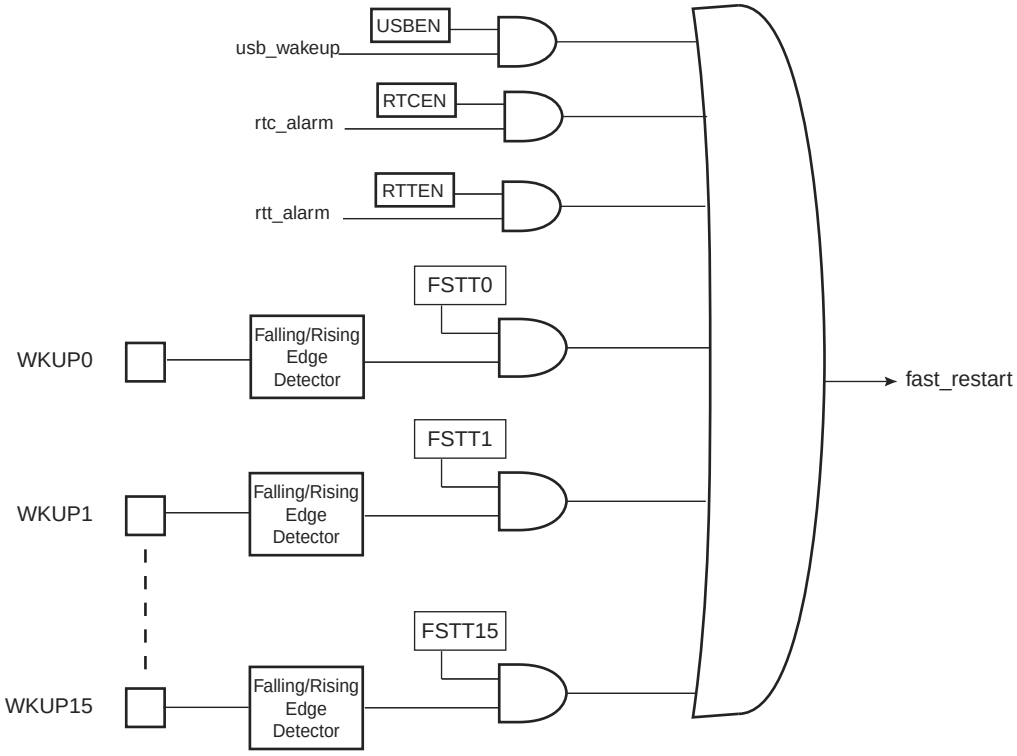


5.7 Fast Startup

The SAM3S8/SD8 allows the processor to restart in a few microseconds while the processor is in wait mode or in sleep mode. A fast start up can occur upon detection of a low level on one of the 19 wake-up inputs (WKUP0 to 15 + SM + RTC + RTT).

The fast restart circuitry, as shown in Figure 5-5, is fully asynchronous and provides a fast start-up signal to the Power Management Controller. As soon as the fast start-up signal is asserted, the PMC automatically restarts the embedded 4 MHz Fast RC oscillator, switches the master clock on this 4MHz clock and reenables the processor clock.

Figure 5-5. Fast Start-Up Sources



6.3 Test Pin

The TST pin is used for JTAG Boundary Scan Manufacturing Test or Fast Flash programming mode of the SAM3S8/SD8 series. The TST pin integrates a permanent pull-down resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations. To enter fast programming mode, see the Fast Flash Programming Interface (FFPI) section. For more on the manufacturing and test mode, refer to the “Debug and Test” section of the product datasheet.

6.4 NRST Pin

The NRST pin is bidirectional. It is handled by the on-chip reset controller and can be driven low to provide a reset signal to the external components or asserted low externally to reset the microcontroller. It will reset the Core and the peripherals except the Backup region (RTC, RTT and Supply Controller). There is no constraint on the length of the reset pulse and the reset controller can guarantee a minimum pulse length. The NRST pin integrates a permanent pull-up resistor to VDDIO of about 100 kΩ. By default, the NRST pin is configured as an input.

6.5 ERASE Pin

The ERASE pin is used to reinitialize the Flash content (and some of its NVM bits) to an erased state (all bits read as logic level 1). It integrates a pull-down resistor of about 100 kΩ to GND, so that it can be left unconnected for normal operations.

This pin is debounced by SCLK to improve the glitch tolerance. When the ERASE pin is tied high during less than 100 ms, it is not taken into account. The pin must be tied high during more than 220 ms to perform a Flash erase operation.

The ERASE pin is a system I/O pin and can be used as a standard I/O. At startup, the ERASE pin is not configured as a PIO pin. If the ERASE pin is used as a standard I/O, startup level of this pin must be low to prevent unwanted erasing. Refer to Section 10.17 “Peripheral Signal Multiplexing on I/O Lines” on page 40. Also, if the ERASE pin is used as a standard I/O output, asserting the pin to low does not erase the Flash.

7. Processor and Architecture

7.1 ARM Cortex-M3 Processor

- Version 2.0
- Thumb-2 (ISA) subset consisting of all base Thumb-2 instructions, 16-bit and 32-bit.
- Harvard processor architecture enabling simultaneous instruction fetch with data load/store.
- Three-stage pipeline.
- Single cycle 32-bit multiply.
- Hardware divide.
- Thumb and Debug states.
- Handler and Thread modes.
- Low latency ISR entry and exit.

7.2 APB/AHB bridge

The SAM3S8/SD8 embeds One Peripheral bridge:

The peripherals of the bridge are clocked by MCK.

7.3 Matrix Masters

The Bus Matrix of the SAM3S8/SD8 manages 4 masters, which means that each master can perform an access concurrently with others, to an available slave.

Each master has its own decoder, which is defined specifically for each master. In order to simplify the addressing, all the masters have the same decodings.

Table 7-1. List of Bus Matrix Masters

Master 0	Cortex-M3 Instruction/Data
Master 1	Cortex-M3 System
Master 2	Peripheral DMA Controller (PDC)
Master 3	CRC Calculation Unit

7.4 Matrix Slaves

The Bus Matrix of the SAM3S8/SD8 manages 5 slaves. Each slave has its own arbiter, allowing a different arbitration per slave.

Table 7-2. List of Bus Matrix Slaves

Slave 0	Internal SRAM
Slave 1	Internal ROM
Slave 2	Internal Flash
Slave 3	External Bus Interface
Slave 4	Peripheral Bridge

9.1.3.4 Flash Speed

The user needs to set the number of wait states depending on the frequency used:

For more details, refer to the “AC Characteristics” sub-section of the product “Electrical Characteristics”.

9.1.3.5 Lock Regions

Several lock bits are used to protect write and erase operations on lock regions. A lock region is composed of several consecutive pages, and each lock region has its associated lock bit.

Table 9-1. Lock bit number

Product	Number of lock bits	Lock region size
SAM3S8/SD8	16	32 kbytes (128 pages)

If a locked-region’s erase or program command occurs, the command is aborted and the EEFC triggers an interrupt.

The lock bits are software programmable through the EEFC User Interface. The command “Set Lock Bit” enables the protection. The command “Clear Lock Bit” unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

9.1.3.6 Security Bit Feature

The SAM3S8/SD8 features a security bit, based on a specific General Purpose NVM bit (GPNVM bit 0). When the security is enabled, any access to the Flash, SRAM, Core Registers and Internal Peripherals either through the ICE interface or through the Fast Flash Programming Interface, is forbidden. This ensures the confidentiality of the code programmed in the Flash.

This security bit can only be enabled, through the command “Set General Purpose NVM Bit 0” of the EEFC User Interface. Disabling the security bit can only be achieved by asserting the ERASE pin at 1, and after a full Flash erase is performed. When the security bit is deactivated, all accesses to the Flash, SRAM, Core registers, Internal Peripherals are permitted.

It is important to note that the assertion of the ERASE pin should always be longer than 200 ms.

As the ERASE pin integrates a permanent pull-down, it can be left unconnected during normal operation. However, it is safer to connect it directly to GND for the final application.

9.1.3.7 Calibration Bits

NVM bits are used to calibrate the brownout detector and the voltage regulator. These bits are factory configured and cannot be changed by the user. The ERASE pin has no effect on the calibration bits.

9.1.3.8 Unique Identifier

Each device integrates its own 128-bit unique identifier. These bits are factory configured and cannot be changed by the user. The ERASE pin has no effect on the unique identifier.

9.1.3.9 Fast Flash Programming Interface

The Fast Flash Programming Interface allows programming the device through either a serial JTAG interface or through a multiplexed fully-handshaked parallel port. It allows gang programming with market-standard industrial programmers.

The reset circuitry is based on a zero-power power-on reset cell and a brownout detector cell. The zero-power power-on reset allows the Supply Controller to start properly, while the software-programmable brownout detector allows detection of either a battery discharge or main voltage loss.

The Slow Clock generator is based on a 32 kHz crystal oscillator and an embedded 32 kHz RC oscillator. The Slow Clock defaults to the RC oscillator, but the software can enable the crystal oscillator and select it as the Slow Clock source.

The Supply Controller starts up the device by sequentially enabling the internal power switches and the Voltage Regulator, then it generates the proper reset signals to the core power supply.

It also enables to set the system in different low-power modes and to wake it up from a wide range of events.

10.5 Clock Generator

The Clock Generator is made up of:

- One Low-power 32768Hz Slow Clock Oscillator with bypass mode
- One Low-power RC Oscillator
- One 3-20 MHz Crystal Oscillator, which can be bypassed
- One Fast RC Oscillator, factory programmed. Three output frequencies can be selected: 4, 8 or 12 MHz. By default 4 MHz is selected.
- One 60 to 130 MHz PLL (PLLB) providing a clock for the USB Full Speed Controller
- One 60 to 130 MHz programmable PLL (PLLA), provides the clock, MCK to the processor and peripherals. The PLLA input frequency is from 3.5 MHz to 20 MHz.

10.9 Real-Time Timer

- Real-Time Timer, allowing backup of time with different accuracies
  - 32-bit Free-running backup Counter
  - Integrates a 16-bit programmable prescaler running on slow clock
  - Alarm Register capable to generate a wake-up of the system through the Shut Down Controller

10.10 Real Time Clock

- Low power consumption
- Full asynchronous design
- Two hundred year Gregorian and Persian calendar
- Programmable Periodic Interrupt
- Trimmable 32.7682 kHz crystal oscillator clock source
- Alarm and update parallel load
- Control of alarm and update Time/Calendar Data In
- Waveform output capability on GPIO pins in low power modes

10.11 General-Purpose Backed-up Registers

- Eight 32-bit backup general-purpose registers

10.12 Nested Vectored Interrupt Controller

- Thirty maskable external interrupts
- Sixteen priority levels
- Processor state automatically saved on interrupt entry, and restored on
- Dynamic reprioritizing of interrupts
- Priority grouping.
  - selection of pre-empting interrupt levels and non pre-empting interrupt levels.
- Support for tail-chaining and late arrival of interrupts.
  - back-to-back interrupt processing without the overhead of state saving and restoration between interrupts.
- Processor state automatically saved on interrupt entry, and restored on interrupt exit, with no instruction overhead.

Table 10-3. Peripheral Identifiers (Continued)

Instance ID	Instance Name	NVIC Interrupt	PMC Clock Control	Instance Description
22	**SSC**	**X**	**X**	Synchronous Serial Controller
23	**TC0**	**X**	**X**	Timer/Counter 0
24	**TC1**	**X**	**X**	Timer/Counter 1
25	**TC2**	**X**	**X**	Timer/Counter 2
26	**TC3**	**X**	**X**	Timer/Counter 3
27	**TC4**	**X**	**X**	Timer/Counter 4
28	**TC5**	**X**	**X**	Timer/Counter 5
29	**ADC**	**X**	**X**	Analog To Digital Converter
30	**DACC**	**X**	**X**	Digital To Analog Converter
31	**PWM**	**X**	**X**	Pulse Width Modulation
32	**CRCCU**	**X**	**X**	CRC Calculation Unit
33	**ACC**	**X**	**X**	Analog Comparator
34	**UDP**	**X**	**X**	USB Device Port

10.17 Peripheral Signal Multiplexing on I/O Lines

The SAM3S8/SD8 features 2 PIO controllers on 64-pin versions (PIOA and PIOB) or 3 PIO controllers on the 100-pin version (PIOA, PIOB and PIOC), that multiplex the I/O lines of the peripheral set.

The SAM3S8/SD8 64-pin and 100-pin PIO Controllers control up to 32 lines. Each line can be assigned to one of three peripheral functions: A, B or C. The multiplexing tables in the following paragraphs define how the I/O lines of the peripherals A, B and C are multiplexed on the PIO Controllers. The column “Comments” has been inserted in this table for the user’s own comments; it may be used to track how pins are defined in an application.

Note that some peripheral functions which are output only, might be duplicated within the tables.

10.17.3 PIO Controller C Multiplexing

Table 10-6. Multiplexing on PIO Controller C (PIOC)

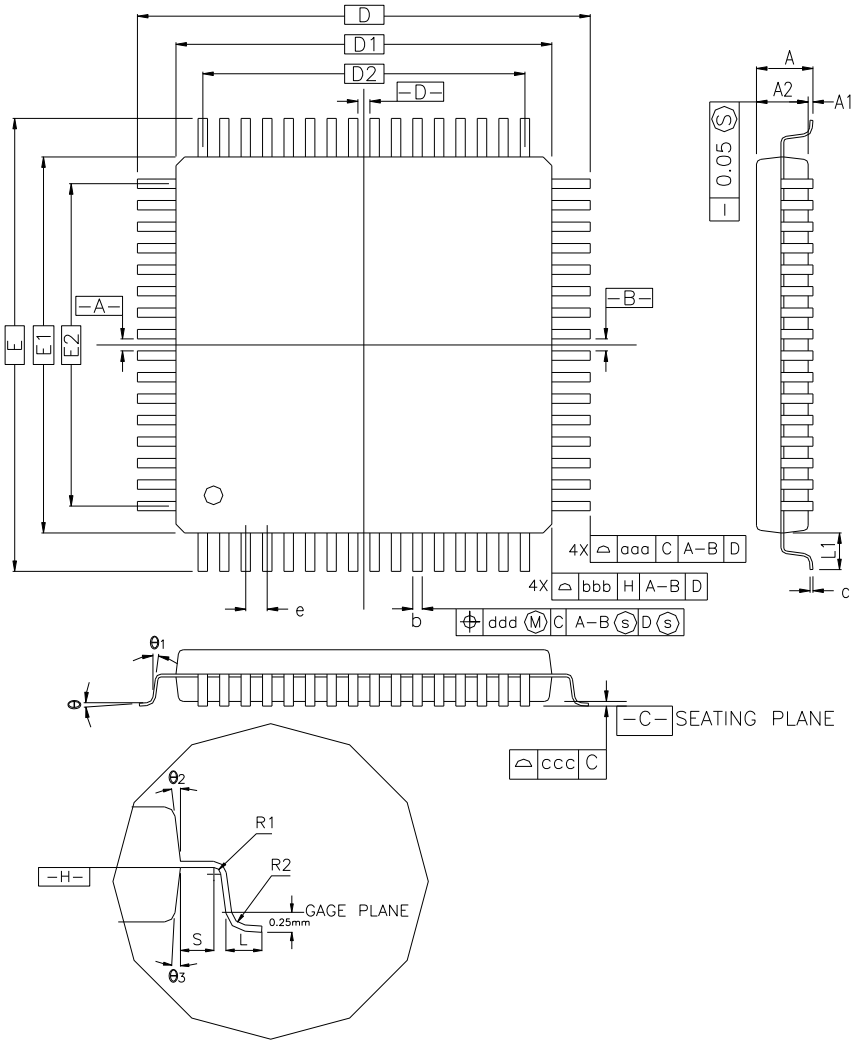
I/O Line	Peripheral A	Peripheral B	Peripheral C	Extra Function	System Function	Comments
PC0	D0	PWML0				100 pin version
PC1	D1	PWML1				100 pin version
PC2	D2	PWML2				100 pin version
PC3	D3	PWML3				100 pin version
PC4	D4	NPCS1				100 pin version
PC5	D5					100 pin version
PC6	D6					100 pin version
PC7	D7					100 pin version
PC8	NWE					100 pin version
PC9	NANDOE	RXD2(1)				100 pin version
PC10	NANDWE	TXD2(1)				100 pin version
PC11	NRD					100 pin version
PC12	NCS3			AD12		100 pin version
PC13	NWAIT	PWML0		AD10		100 pin version
PC14	NCS0	SCK2(1)				100 pin version
PC15	NCS1	PWML1		AD11		100 pin version
PC16	A21/NANDALE	RTS2(1)				100 pin version
PC17	A22/NANDCLE	CTS2(1)				100 pin version
PC18	A0	PWMH0				100 pin version
PC19	A1	PWMH1				100 pin version
PC20	A2	PWMH2				100 pin version
PC21	A3	PWMH3				100 pin version
PC22	A4	PWML3				100 pin version
PC23	A5	TIOA3				100 pin version
PC24	A6	TIOB3				100 pin version
PC25	A7	TCLK3				100 pin version
PC26	A8	TIOA4				100 pin version
PC27	A9	TIOB4				100 pin version
PC28	A10	TCLK4				100 pin version
PC29	A11	TIOA5		AD13		100 pin version
PC30	A12	TIOB5		AD14		100 pin version
PC31	A13	TCLK5				100 pin version

Note: 1. USART2 only on SAM3SD8 in 100 pin package.

12. Package Drawings

The SAM3S8/SD8 series devices are available in LQFP, QFN and TFBGA packages.

Figure 12-1. 100-lead LQFP Package Mechanical Drawing

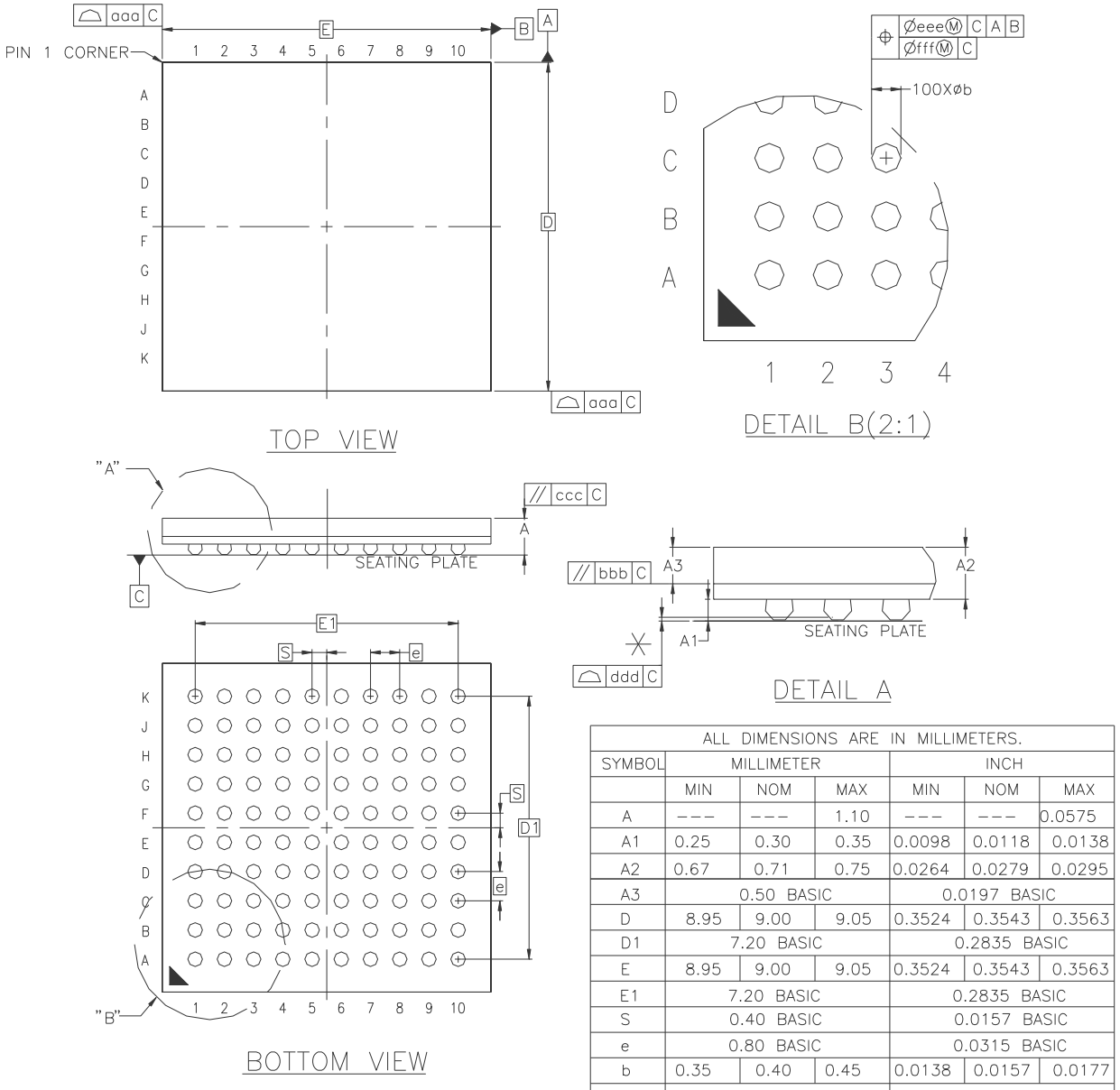


COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BSC.			0.630 BSC.		
D_1	14.00 BSC.			0.551 BSC.		
E	16.00 BSC.			0.630 BSC.		
E_1	14.00 BSC.			0.551 BSC.		
R_2	0.08	—	0.20	0.003	—	0.008
R_1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	0°	—	—	0°	—	—
$θ_2$	11°	12°	13°	11°	12°	13°
$θ_3$	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	12.00			0.472		
E2	12.00			0.472		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

Note : 1. This drawing is for general information only. Refer to JEDEC Drawing MS-026 for additional information.

Figure 12-2. 100-ball TFBGA Package Mechanical Drawing



ALL DIMENSIONS ARE IN MILLIMETERS.						
SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	0.0575
A1	0.25	0.30	0.35	0.0098	0.0118	0.0138
A2	0.67	0.71	0.75	0.0264	0.0279	0.0295
A3	0.50 BASIC			0.0197 BASIC		
D	8.95	9.00	9.05	0.3524	0.3543	0.3563
D1	7.20 BASIC			0.2835 BASIC		
E	8.95	9.00	9.05	0.3524	0.3543	0.3563
E1	7.20 BASIC			0.2835 BASIC		
S	0.40 BASIC			0.0157 BASIC		
e	0.80 BASIC			0.0315 BASIC		
b	0.35	0.40	0.45	0.0138	0.0157	0.0177
aaa	0.15			0.0059		
bbb	0.20			0.0079		
ccc	0.20			0.0079		
ddd	0.12			0.0047		
eee	0.15			0.0059		
fff	0.08			0.0031		

Table 12-1. 64-lead LQFP Package Dimensions (in mm) (Continued)

Symbol	Millimeter			Inch		
	Min	**Nom**	**Max**	**Min**	**Nom**	**Max**
S	0.20	–	–	0.008	–	–
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	7.50			0.285		
E2	7.50			0.285		
Tolerances of Form and Position						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

Revision History

In the information that follows, the most recent version of the document is referenced first.

Doc. Rev	Comments	Change Request Ref.
11090BS	Corrected Figure 12-3 “64-lead LQFP Package Mechanical Drawing” and inserted Table 12-1 “64-lead LQFP Package Dimensions (in mm)”.	9389

Doc. Rev	Comments	Change Request Ref.
11090AS	First issue	

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