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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	I²C, IrDA, Memory Card, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	47
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 10x10/12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam3sd8ba-au

2. Block Diagram

Figure 2-1. SAM3S8/SD8 100-pin version Block Diagram

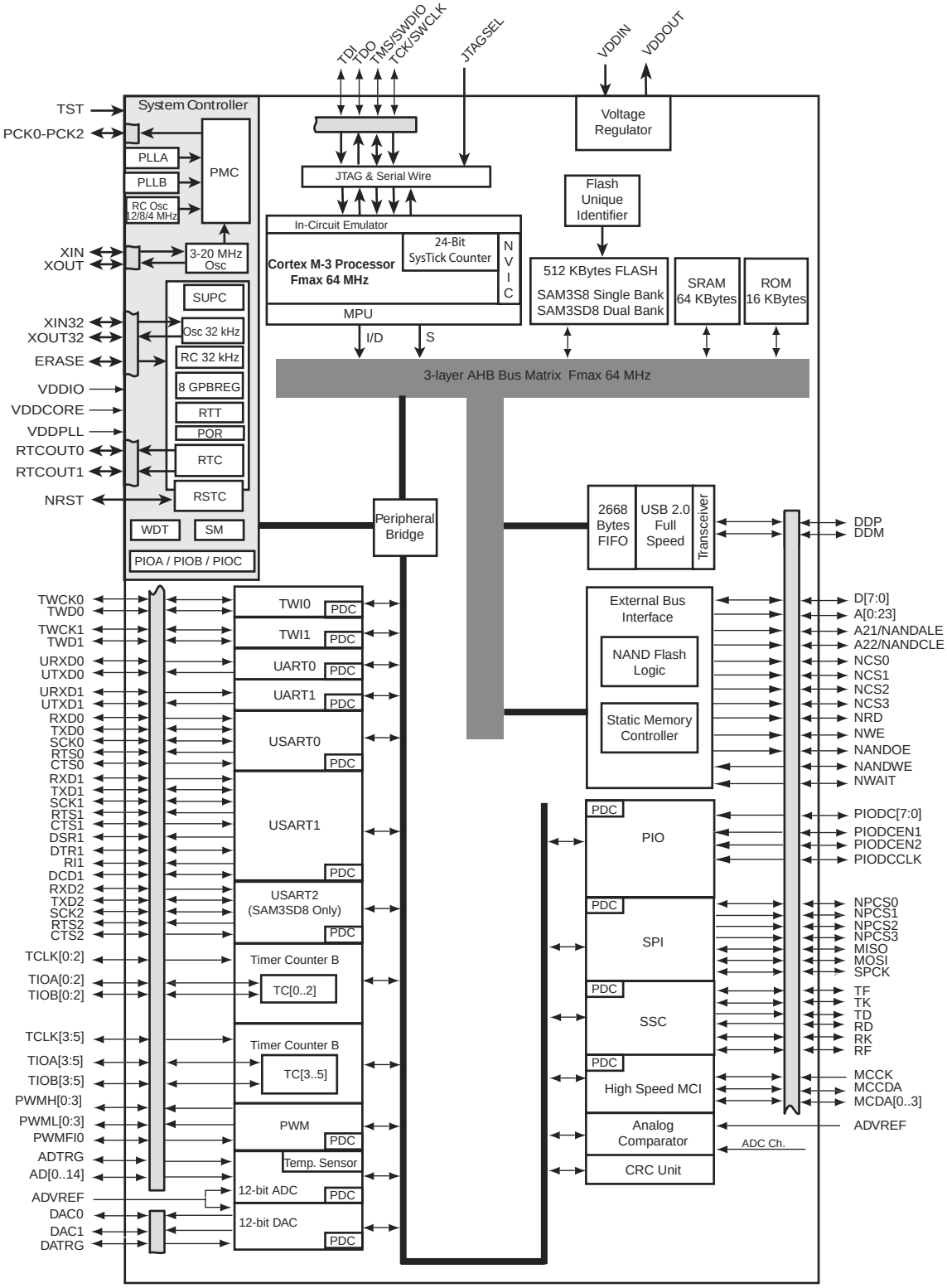


Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage reference	Comments
Flash Memory					
ERASE	Flash and NVM Configuration Bits Erase Command	Input	High	VDDIO	Reset State: - Erase Input - Internal pull-down enabled - Schmitt Trigger enabled(1)
Reset/Test					
NRST	Synchronous Microcontroller Reset	I/O	Low	VDDIO	Permanent Internal pull-up
TST	Test Select	Input			Permanent Internal pull-down
Universal Asynchronous Receiver Transceiver - UARTx					
URXDx	UART Receive Data	Input			
UTXDx	UART Transmit Data	Output			
PIO Controller - PIOA - PIOB - PIOC					
PA0 - PA31	Parallel IO Controller A	I/O		VDDIO	Reset State: - PIO or System IOs(2) - Internal pull-up enabled - Schmitt Trigger enabled(1)
PB0 - PB14	Parallel IO Controller B	I/O			
PC0 - PC31	Parallel IO Controller C	I/O			
PIO Controller - Parallel Capture Mode					
PIODC0-PIODC7	Parallel Capture Mode Data	Input		VDDIO	
PIODCCLK	Parallel Capture Mode Clock	Input			
PIODCEN1-2	Parallel Capture Mode Enable	Input			
External Bus Interface					
D0 - D7	Data Bus	I/O			
A0 - A23	Address Bus	Output			
NWAIT	External Wait Signal	Input	Low		
Static Memory Controller - SMC					
NCS0 - NCS3	Chip Select Lines	Output	Low		
NRD	Read Signal	Output	Low		
NWE	Write Enable	Output	Low		
NAND Flash Logic					
NANDOE	NAND Flash Output Enable	Output	Low		
NANDWE	NAND Flash Write Enable	Output	Low		
High Speed Multimedia Card Interface - HSMCI					
MCCK	Multimedia Card Clock	I/O			
MCCDA	Multimedia Card Slot A Command	I/O			
MCDA0 - MCDA3	Multimedia Card Slot A Data	I/O			

4.1.3 100-Lead LQFP Pinout

Table 4-1. SAM3S8C/SD8C 100-lead LQFP pinout

1	ADVREF	26	GND	51	TDI/PB4	76	TDO/TRACESWO/ PB5
2	GND	27	VDDIO	52	PA6/PGMNOE	77	JTAGSEL
3	PB0/AD4	28	PA16/PGMD4	53	PA5/PGMRDY	78	PC18
4	PC29/AD13	29	PC7	54	PC28	79	TMS/SWDIO/PB6
5	PB1/AD5	30	PA15/PGMD3	55	PA4/PGMNCMD	80	PC19
6	PC30/AD14	31	PA14/PGMD2	56	VDDCORE	81	PA31
7	PB2/AD6	32	PC6	57	PA27/PGMD15	82	PC20
8	PC31	33	PA13/PGMD1	58	PC8	83	TCK/SWCLK/PB7
9	PB3/AD7	34	PA24/PGMD12	59	PA28	84	PC21
10	VDDIN	35	PC5	60	NRST	85	VDDCORE
11	VDDOUT	36	VDDCORE	61	TST	86	PC22
12	PA17/PGMD5/AD0	37	PC4	62	PC9	87	ERASE/PB12
13	PC26	38	PA25/PGMD13	63	PA29	88	DDM/PB10
14	PA18/PGMD6/AD1	39	PA26/PGMD14	64	PA30	89	DDP/PB11
15	PA21/PGMD9/AD8	40	PC3	65	PC10	90	PC23
16	VDDCORE	41	PA12/PGMD0	66	PA3	91	VDDIO
17	PC27	42	PA11/PGMM3	67	PA2/PGMEN2	92	PC24
18	PA19/PGMD7/AD2	43	PC2	68	PC11	93	PB13/DAC0
19	PC15/AD11	44	PA10/PGMM2	69	VDDIO	94	PC25
20	PA22/PGMD10/AD 9	45	GND	70	GND	95	GND
21	PC13/AD10	46	PA9/PGMM1	71	PC14	96	PB8/XOUT
22	PA23/PGMD11	47	PC1	72	PA1/PGMEN1	97	PB9/*PGMCK/XIN*
23	PC12/AD12	48	PA8/XOUT32/ PGMM0	73	PC16	98	VDDIO
24	PA20/PGMD8/AD3	49	PA7/XIN32/ PGMNVALID	74	PA0/PGMEN0	99	PB14/DAC1
25	PC0	50	VDDIO	75	PC17	100	VDDPLL

4.1.4 100-Ball TFBGA Pinout

Table 4-2. SAM3S8C/SD8C 100-ball TFBGA pinout

A1	PB1/AD5	C6	TCK/SWCLK/PB7	F1	PA18/PGMD6/AD1	H6	PC4
A2	PC29	C7	PC16	F2	PC26	H7	PA11/PGMM3
A3	VDDIO	C8	PA1/PGMEN1	F3	VDDOUT	H8	PC1
A4	PB9/PGMCK/XIN	C9	PC17	F4	GND	H9	PA6/PGMNOE
A5	PB8/XOUT	C10	PA0/PGMEN0	F5	VDDIO	H10	TDI/PB4
A6	PB13/DAC0	D1	PB3/AD7	F6	PA27/PGMD15	J1	PC15/AD11
A7	DDP/PB11	D2	PB0/AD4	F7	PC8	J2	PC0
A8	DDM/PB10	D3	PC24	F8	PA28	J3	PA16/PGMD4
A9	TMS/SWDIO/PB6	D4	PC22	F9	TST	J4	PC6
A10	JTAGSEL	D5	GND	F10	PC9	J5	PA24/PGMD12
B1	PC30	D6	GND	G1	PA21/PGMD9/AD8	J6	PA25/PGMD13
B2	ADVREF	D7	VDDCORE	G2	PC27	J7	PA10/PGMM2
B3	GNDANA	D8	PA2/PGMEN2	G3	PA15/PGMD3	J8	GND
B4	PB14/DAC1	D9	PC11	G4	VDDCORE	J9	VDDCORE
B5	PC21	D10	PC14	G5	VDDCORE	J10	VDDIO
B6	PC20	E1	PA17/PGMD5/AD0	G6	PA26/PGMD14	K1	PA22/PGMD10/AD9
B7	PA31	E2	PC31	G7	PA12/PGMD0	K2	PC13/AD10
B8	PC19	E3	VDDIN	G8	PC28	K3	PC12/AD12
B9	PC18	E4	GND	G9	PA4/PGMNCMD	K4	PA20/PGMD8/AD3
B10	TDO/TRACESWO/PB5	E5	GND	G10	PA5/PGMRDY	K5	PC5
C1	PB2/AD6	E6	NRST	H1	PA19/PGMD7/AD2	K6	PC3
C2	VDDPLL	E7	PA29/AD13	H2	PA23/PGMD11	K7	PC2
C3	PC25	E8	PA30/AD14	H3	PC7	K8	PA9/PGMM1
C4	PC23	E9	PC10	H4	PA14/PGMD2	K9	PA8/XOUT32/PGMM0
C5	ERASE/PB12	E10	PA3	H5	PA13/PGMD1	K10	PA7/XIN32/PGMNVALID

5. Power Considerations

5.1 Power Supplies

The SAM3S8/SD8 has several types of power supply pins:

- VDDCORE pins: Power the core, the embedded memories and the peripherals. Voltage ranges from 1.62V to 1.95V.
- VDDIO pins: Power the Peripherals I/O lines (Input/Output Buffers), USB transceiver, Backup part, 32 kHz crystal oscillator and oscillator pads. Voltage ranges from 1.62V to 3.6V.
- VDDIN pin: Voltage Regulator Input, ADC, DAC and Analog Comparator Power Supply. Voltage ranges from 1.8V to 3.6V.
- VDDPLL pin: Powers the PLLA, PLLB, the Fast RC and the 3 to 20 MHz oscillator. Voltage ranges from 1.62V to 1.95V.

5.2 Voltage Regulator

The SAM3S8/SD8 embeds a voltage regulator that is managed by the Supply Controller.

This internal regulator is designed to supply the internal core of SAM3S8/SD8. It features two operating modes:

- In Normal mode, the voltage regulator consumes less than 700 µA static current and draws 80 mA of output current. Internal adaptive biasing adjusts the regulator quiescent current depending on the required load current. In Wait Mode quiescent current is only 7 µA.
- In Backup mode, the voltage regulator consumes less than 1 µA while its output (VDDOUT) is driven internally to GND. The default output voltage is 1.80V and the start-up time to reach Normal mode is less than 100 µs.

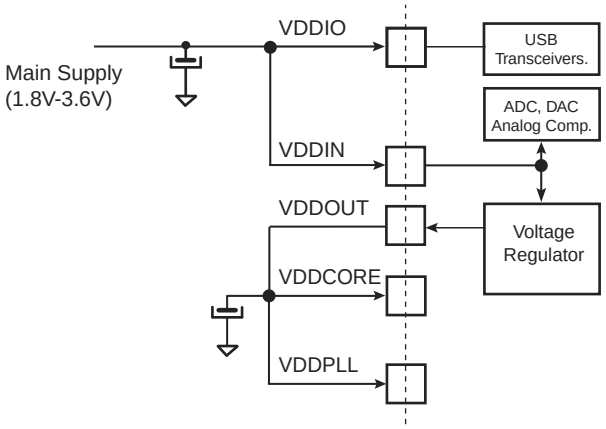
For adequate input and output power supply decoupling/bypassing, refer to the “Voltage Regulator” section in the “Electrical Characteristics” section of the datasheet.

5.3 Typical Powering Schematics

The SAM3S8/SD8 supports a 1.62V-3.6V single supply mode. The internal regulator input connected to the source and its output feeds VDDCORE. Figure 5-1 below shows the power schematics.

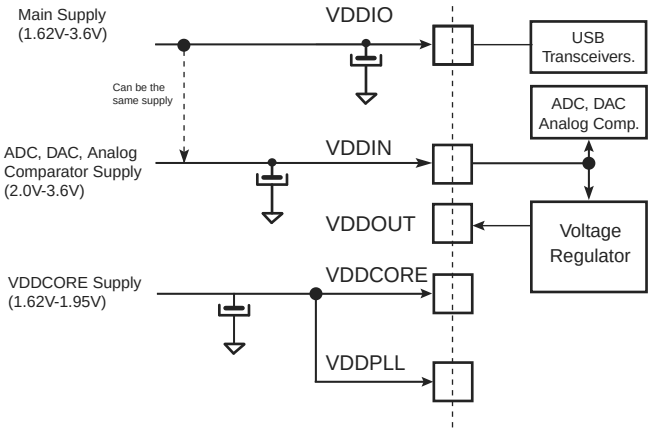
As VDDIN powers the voltage regulator, the ADC, DAC and the analog comparator, when the user does not want to use the embedded voltage regulator, it can be disabled by software via the SUPC (note that this is different from Backup mode).

Figure 5-1. Single Supply



Note: Restrictions
With Main Supply < 2.0 V, USB and ADC/DAC and Analog comparator are not usable.
With Main Supply ≥ 2.0V and < 3V, USB is not usable.
With Main Supply ≥ 3V, all peripherals are usable.

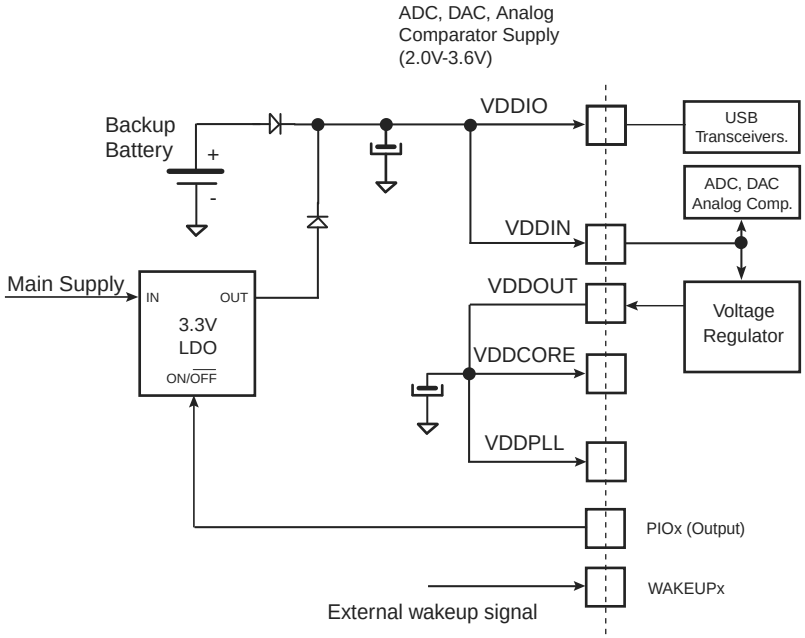
Figure 5-2. Core Externally Supplied



Note: Restrictions
With Main Supply < 2.0V, USB is not usable.
With VDDIN < 2.0V, ADC, DAC and Analog comparator are not usable.
With Main Supply ≥ 2.0V and < 3V, USB is not usable.
With Main Supply and VDDIN ≥ 3V, all peripherals are usable.

Figure 5-3 below provides an example of the powering scheme when using a backup battery. Since the PIO state is preserved when in backup mode, any free PIO line can be used to switch off the external regulator by driving the PIO line at low level (PIO is input, pull-up enabled after backup reset). External wake-up of the system can be from a push button or any signal. See Section 5.6 “Wake-up Sources” for further details.

Figure 5-3. Backup Battery



Note: The two diodes provide a "switchover circuit" (for illustration purpose) between the backup battery and the main supply when the system is put in backup mode.

5.4 Active Mode

Active mode is the normal running mode with the core clock running from the fast RC oscillator, the main crystal oscillator or the PLLA. The power management controller can be used to adapt the frequency and to disable the peripheral clocks.

5.5 Low-power Modes

The various low-power modes of the SAM3S8/SD8 are described below:

5.5.1 Backup Mode

The purpose of backup mode is to achieve the lowest power consumption possible in a system which is performing periodic wake-ups to perform tasks but not requiring fast startup time (<0.1ms). Total current consumption is 1.5 µA typical.

The Supply Controller, zero-power power-on reset, RTT, RTC, Backup registers and 32 kHz oscillator (RC or crystal oscillator selected by software in the Supply Controller) are running. The regulator and the core supply are off.

Backup mode is based on the Cortex-M3 deep sleep mode with the voltage regulator disabled.

The SAM3S8/SD8 can be awakened from this mode through WUP0-15 pins, the supply monitor (SM), the RTT or RTC wake-up event.

Backup mode is entered by using WFE instructions with the SLEEPDEEP bit in the Cortex-M3 System Control Register set to 1. (See the Power management description in The ARM Cortex-M3 Processor section of the product datasheet).

Exit from Backup mode happens if one of the following enable wake up events occurs:

- WKUPEN0-15 pins (level transition, configurable debouncing)

- Supply Monitor alarm
- RTC alarm
- RTT alarm

5.5.2 Wait Mode

The purpose of the wait mode is to achieve very low power consumption while maintaining the whole device in a powered state for a startup time of less than 10 µs. Current Consumption in Wait mode is typically 15 µA (total current consumption) if the internal voltage regulator is used or 8 µA if an external regulator is used.

In this mode, the clocks of the core, peripherals and memories are stopped. However, the core, peripherals and memories power supplies are still powered. From this mode, a fast start up is available.

This mode is entered via Wait for Event (WFE) instructions with LPM = 1 (Low Power Mode bit in PMC_FSMR). The Cortex-M3 is able to handle external events or internal events in order to wake-up the core (WFE). This is done by configuring the external lines WUP0-15 as fast startup wake-up pins (refer to Section 5.7 “Fast Startup”). RTC or RTT Alarm and USB wake-up events can be used to wake up the CPU (exit from WFE).

Entering Wait Mode:

- Select the 4/8/12 MHz fast RC oscillator as Main Clock
- Set the LPM bit in the PMC Fast Startup Mode Register (PMC_FSMR)
- Execute the Wait-For-Event (WFE) instruction of the processor

Note: Internal Main clock resynchronization cycles are necessary between the writing of MOSCRCEN bit and the effective entry in Wait mode. Depending on the user application, waiting for MOSCRCEN bit to be cleared is recommended to ensure that the core will not execute undesired instructions.

5.5.3 Sleep Mode

The purpose of sleep mode is to optimize power consumption of the device versus response time. In this mode, only the core clock is stopped. The peripheral clocks can be enabled. The current consumption in this mode is application dependent.

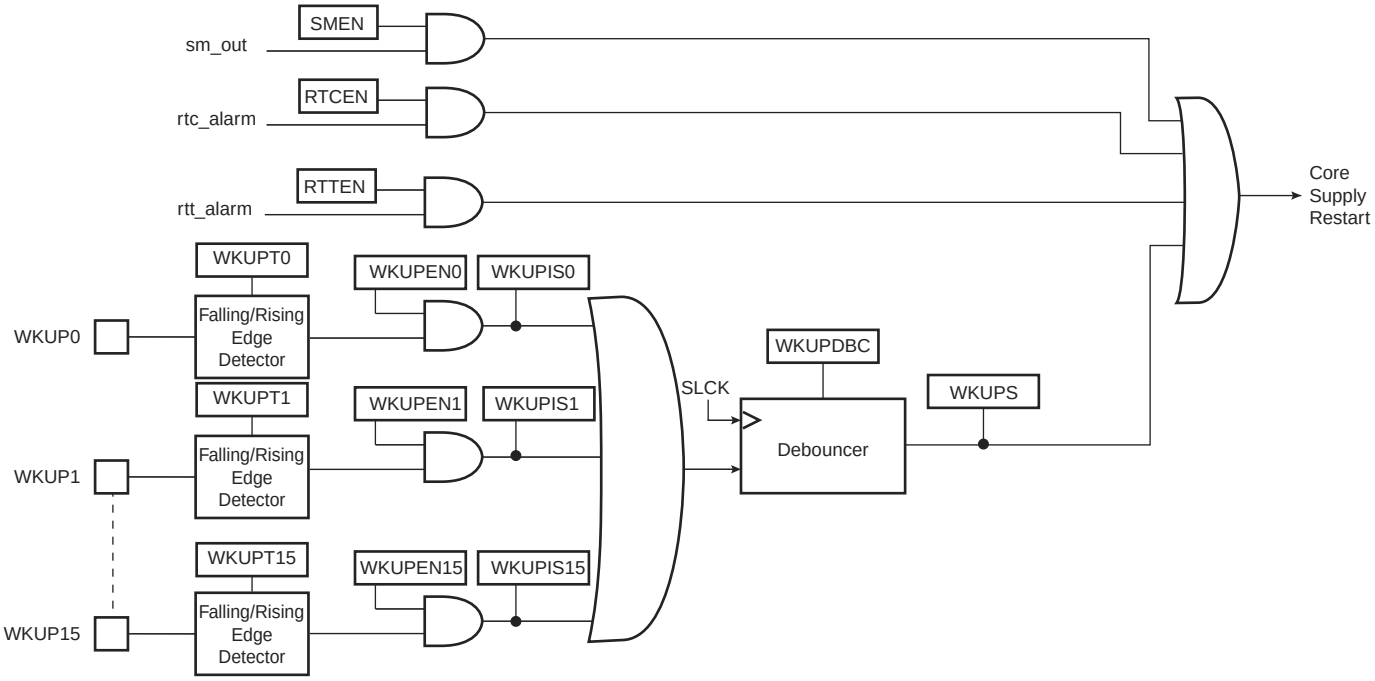
This mode is entered via Wait for Interrupt (WFI) or Wait for Event (WFE) instructions with LPM = 0 in PMC_FSMR.

The processor can be awakened from an interrupt if WFI instruction of the Cortex M3 is used, or from an event if the WFE instruction is used to enter this mode.

5.6 Wake-up Sources

The wake-up events allow the device to exit the backup mode. When a wake-up event is detected, the Supply Controller performs a sequence which automatically reenables the core power supply and the SRAM power supply, if they are not already enabled.

Figure 5-4. Wake-up Source

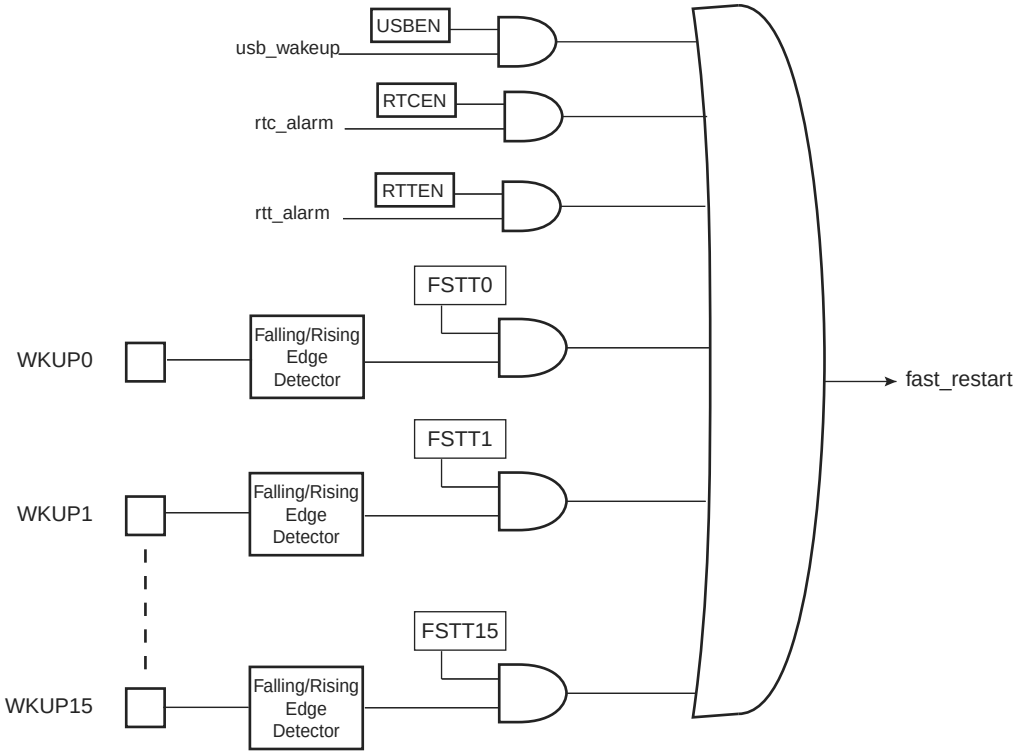


5.7 Fast Startup

The SAM3S8/SD8 allows the processor to restart in a few microseconds while the processor is in wait mode or in sleep mode. A fast start up can occur upon detection of a low level on one of the 19 wake-up inputs (WKUP0 to 15 + SM + RTC + RTT).

The fast restart circuitry, as shown in Figure 5-5, is fully asynchronous and provides a fast start-up signal to the Power Management Controller. As soon as the fast start-up signal is asserted, the PMC automatically restarts the embedded 4 MHz Fast RC oscillator, switches the master clock on this 4MHz clock and reenables the processor clock.

Figure 5-5. Fast Start-Up Sources



6.3 Test Pin

The TST pin is used for JTAG Boundary Scan Manufacturing Test or Fast Flash programming mode of the SAM3S8/SD8 series. The TST pin integrates a permanent pull-down resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations. To enter fast programming mode, see the Fast Flash Programming Interface (FFPI) section. For more on the manufacturing and test mode, refer to the “Debug and Test” section of the product datasheet.

6.4 NRST Pin

The NRST pin is bidirectional. It is handled by the on-chip reset controller and can be driven low to provide a reset signal to the external components or asserted low externally to reset the microcontroller. It will reset the Core and the peripherals except the Backup region (RTC, RTT and Supply Controller). There is no constraint on the length of the reset pulse and the reset controller can guarantee a minimum pulse length. The NRST pin integrates a permanent pull-up resistor to VDDIO of about 100 kΩ. By default, the NRST pin is configured as an input.

6.5 ERASE Pin

The ERASE pin is used to reinitialize the Flash content (and some of its NVM bits) to an erased state (all bits read as logic level 1). It integrates a pull-down resistor of about 100 kΩ to GND, so that it can be left unconnected for normal operations.

This pin is debounced by SCLK to improve the glitch tolerance. When the ERASE pin is tied high during less than 100 ms, it is not taken into account. The pin must be tied high during more than 220 ms to perform a Flash erase operation.

The ERASE pin is a system I/O pin and can be used as a standard I/O. At startup, the ERASE pin is not configured as a PIO pin. If the ERASE pin is used as a standard I/O, startup level of this pin must be low to prevent unwanted erasing. Refer to Section 10.17 “Peripheral Signal Multiplexing on I/O Lines” on page 40. Also, if the ERASE pin is used as a standard I/O output, asserting the pin to low does not erase the Flash.

The FFPI supports read, page program, page erase, full erase, lock, unlock and protect commands.

9.1.3.10 SAM-BA Boot

The SAM-BA Boot is a default Boot Program which provides an easy way to program in-situ the on-chip Flash memory.

The SAM-BA Boot Assistant supports serial communication via the UART and USB.

The SAM-BA Boot provides an interface with SAM-BA Graphic User Interface (GUI).

The SAM-BA Boot is in ROM and is mapped in Flash at address 0x0 when GPNVM bit 1 is set to 0.

9.1.3.11 GPNVM Bits

The SAM3S8 features two GPNVM bits, whereas SAM3SD8 features three GPNVM bits. These bits can be cleared or set respectively through the commands “Clear GPNVM Bit” and “Set GPNVM Bit” of the EEFC User Interface.

The Flash of the SAM3S8 is composed of 512 Kbytes in a single bank, while the SAM3SD8 Flash is composed of dual banks, each containing 256 Kbytes. The dual-bank function enables programming one bank while the other one is read (typically while the application code is running). Only one EEFC (Flash controller) controls the two banks. Note that it is not possible to program simultaneously, or read simultaneously, the dual banks of the Flash.

The first bank of 256 Kbytes is called Bank 0 and the second bank of 256 Kbytes, Bank 1.

The SAM3SD8 embeds an additional GPNVM bit: GPNVM2.

Table 9-2. General-purpose Non volatile Memory Bits

GPNVMBit[#]	Function
0	Security bit
1	Boot mode selection
2	Bank selection (Bank 0 or Bank 1) Only on SAM3SD8

9.1.4 Boot Strategies

The system always boots at address 0x0. To ensure maximum boot possibilities, the memory layout can be changed via GPNVM.

A general purpose NVM (GPNVM) bit is used to boot either on the ROM (default) or from the Flash.

The GPNVM bit can be cleared or set respectively through the commands “Clear General-purpose NVM Bit” and “Set General-purpose NVM Bit” of the EEFC User Interface.

Setting GPNVM Bit 1 selects the boot from the Flash, clearing it selects the boot from the ROM. Asserting ERASE clears the GPNVM Bit 1 and thus selects the boot from the ROM by default.

Setting the GPNVM Bit 2 selects bank 1, clearing it selects the boot from bank 0. Asserting ERASE clears the GPNVM Bit 2 and thus selects the boot from bank 0 by default.

10.1 System Controller and Peripherals Mapping

Please refer to Section 8-1 “SAM3S8/SD8 Product Mapping” on page 27.

All the peripherals are in the bit band region and are mapped in the bit band alias region.

10.2 Power-on-Reset, Brownout and Supply Monitor

The SAM3S8/SD8 embeds three features to monitor, warn and/or reset the chip:

- Power-on-Reset on VDDIO
- Brownout Detector on VDDCORE
- Supply Monitor on VDDIO

10.2.1 Power-on-Reset

The Power-on-Reset monitors VDDIO. It is always activated and monitors voltage at start up but also during power down. If VDDIO goes below the threshold voltage, the entire chip is reset. For more information, refer to the Electrical Characteristics section of the datasheet.

10.2.2 Brownout Detector on VDDCORE

The Brownout Detector monitors VDDCORE. It is active by default. It can be deactivated by software through the Supply Controller (SUPC_MR). It is especially recommended to disable it during low-power modes such as wait or sleep modes.

If VDDCORE goes below the threshold voltage, the reset of the core is asserted. For more information, refer to the Supply Controller (SUPC) and Electrical Characteristics sections of the datasheet.

10.2.3 Supply Monitor on VDDIO

The Supply Monitor monitors VDDIO. It is not active by default. It can be activated by software and is fully programmable with 16 steps for the threshold (between 1.9V to 3.4V). It is controlled by the Supply Controller (SUPC). A sample mode is possible. It allows to divide the supply monitor power consumption by a factor of up to 2048. For more information, refer to the SUPC and Electrical Characteristics sections of the datasheet.

10.3 Reset Controller

The Reset Controller is based on a Power-on-Reset cell, and a Supply Monitor on VDDCORE.

The Reset Controller is capable to return to the software the source of the last reset, either a general reset, a wake-up reset, a software reset, a user reset or a watchdog reset.

The Reset Controller controls the internal resets of the system and the NRST pin input/output. It is capable to shape a reset signal for the external devices, simplifying to a minimum connection of a push-button on the NRST pin to implement a manual reset.

The configuration of the Reset Controller is saved as supplied on VDDIO.

10.4 Supply Controller (SUPC)

The Supply Controller controls the power supplies of each section of the processor and the peripherals (via Voltage regulator control)

The Supply Controller has its own reset circuitry and is clocked by the 32 kHz Slow clock generator.

Table 10-3. Peripheral Identifiers (Continued)

Instance ID	Instance Name	NVIC Interrupt	PMC Clock Control	Instance Description
22	**SSC**	**X**	**X**	Synchronous Serial Controller
23	**TC0**	**X**	**X**	Timer/Counter 0
24	**TC1**	**X**	**X**	Timer/Counter 1
25	**TC2**	**X**	**X**	Timer/Counter 2
26	**TC3**	**X**	**X**	Timer/Counter 3
27	**TC4**	**X**	**X**	Timer/Counter 4
28	**TC5**	**X**	**X**	Timer/Counter 5
29	**ADC**	**X**	**X**	Analog To Digital Converter
30	**DACC**	**X**	**X**	Digital To Analog Converter
31	**PWM**	**X**	**X**	Pulse Width Modulation
32	**CRCCU**	**X**	**X**	CRC Calculation Unit
33	**ACC**	**X**	**X**	Analog Comparator
34	**UDP**	**X**	**X**	USB Device Port

10.17 Peripheral Signal Multiplexing on I/O Lines

The SAM3S8/SD8 features 2 PIO controllers on 64-pin versions (PIOA and PIOB) or 3 PIO controllers on the 100-pin version (PIOA, PIOB and PIOC), that multiplex the I/O lines of the peripheral set.

The SAM3S8/SD8 64-pin and 100-pin PIO Controllers control up to 32 lines. Each line can be assigned to one of three peripheral functions: A, B or C. The multiplexing tables in the following paragraphs define how the I/O lines of the peripherals A, B and C are multiplexed on the PIO Controllers. The column “Comments” has been inserted in this table for the user’s own comments; it may be used to track how pins are defined in an application.

Note that some peripheral functions which are output only, might be duplicated within the tables.

10.17.2 PIO Controller B Multiplexing

Table 10-5. Multiplexing on PIO Controller B (PIOB)

I/O Line	Peripheral A	Peripheral B	Peripheral C	Extra Function	System Function	Comments
PB0	PWMH0			AD4/RTCOUT0		
PB1	PWMH1			AD5/RTCOUT1		
PB2	URXD1	NPCS2		AD6/WKUP12		
PB3	UTXD1	PCK2		AD7		
PB4	TWD1	PWMH2			TDI	
PB5	TWCK1	PWML0		WKUP13	TDO/TRACESWO	
PB6					TMS/SWDIO	
PB7					TCK/SWCLK	
PB8					XOUT	
PB9					XIN	
PB10					DDM	
PB11					DDP	
PB12	PWML1				ERASE	
PB13	PWML2	PCK0		DAC0		64/00 pins versions
PB14	NPCS1	PWMH3		DAC1		64/100 pins versions

  - Interval Measurement
  - Pulse Generation
  - Delay Timing
  - Pulse Width Modulation
  - Up/down Capabilities
- Each channel is user-configurable and contains:
  - Three external clock inputs
  - Five internal clock inputs
  - Two multi-purpose input/output signals
- Two global registers that act on all three TC Channels
- Quadrature decoder
  - Advanced line filtering
  - Position / revolution / speed
- 2-bit Gray Up/Down Counter for Stepper Motor

11.7 Pulse Width Modulation Controller (PWM)

- One Four-channel 16-bit PWM Controller, 16-bit counter per channel
- Common clock generator, providing Thirteen Different Clocks
  - A Modulo n counter providing eleven clocks
  - Two independent Linear Dividers working on modulo n counter outputs
  - High Frequency Asynchronous clocking mode
- Independent channel programming
  - Independent Enable Disable Commands
  - Independent Clock Selection
  - Independent Period and Duty Cycle, with Double Buffering
  - Programmable selection of the output waveform polarity
  - Programmable center or left aligned output waveform
  - Independent Output Override for each channel
  - Independent complementary Outputs with 12-bit dead time generator for each channel
  - Independent Enable Disable Commands
  - Independent Clock Selection
  - Independent Period and Duty Cycle, with Double Buffering
- Synchronous Channel mode
  - Synchronous Channels share the same counter
  - Mode to update the synchronous channels registers after a programmable number of periods
- Connection to one PDC channel
  - Provides Buffer transfer without processor intervention, to update duty cycle of synchronous channels
- Two independent event lines which can send up to 4 triggers on ADC within a period

- One programmable Fault Input providing an asynchronous protection of outputs
- Stepper motor control (2 Channels)

11.8 High Speed Multimedia Card Interface (HSMCI)

- 4-bit or 1-bit Interface
- Compatibility with MultiMedia Card Specification Version 4.3
- Compatibility with SD and SDHC Memory Card Specification Version 2.0
- Compatibility with SDIO Specification Version V1.1.
- Compatibility with CE-ATA Specification 1.1
- Cards clock rate up to Master Clock divided by 2
- Boot Operation Mode support
- High Speed mode support
- Embedded power management to slow down clock rate when not used
- MCI has one slot supporting
  - One MultiMediaCard bus (up to 30 cards) or
  - One SD Memory Card
  - One SDIO Card
- Support for stream, block and multi-block data read and write

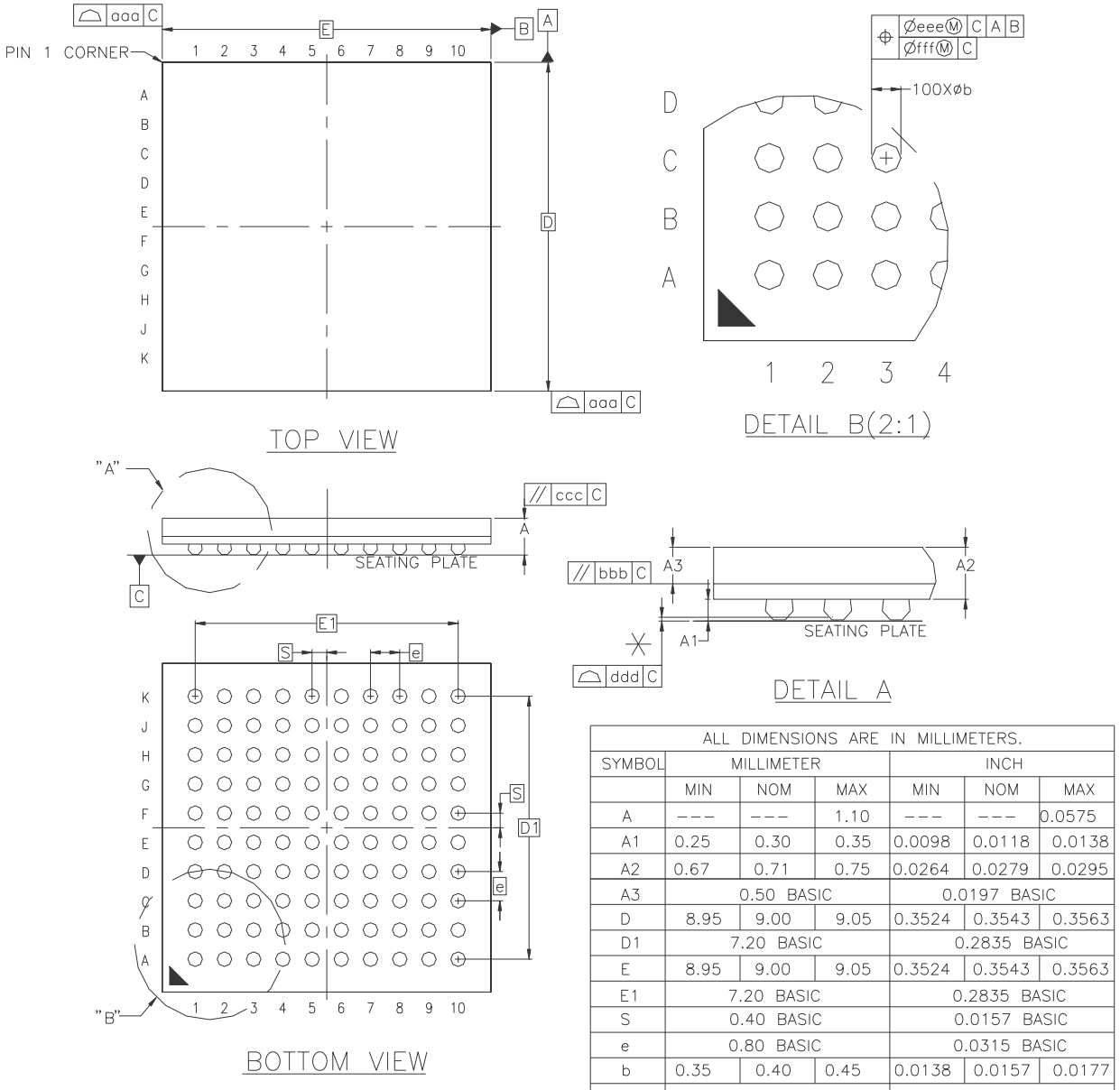
11.9 USB Device Port (UDP)

- USB V2.0 full-speed compliant,12 Mbits per second.
- Embedded USB V2.0 full-speed transceiver
- Embedded 2688-byte dual-port RAM for endpoints
- Eight endpoints
  - Endpoint 0: 64bytes
  - Endpoint 1 and 2: 64 bytes ping-pong
  - Endpoint 3: 64 bytes
  - Endpoint 4 and 5: 512 bytes ping-pong
  - Endpoint 6 and 7: 64 bytes ping-pong
  - Ping-pong Mode (two memory banks) for Isochronous and bulk endpoints
- Suspend/resume logic
- Integrated Pull-up on DDP
- Pull-down resistor on DDM and DDP when disabled

11.10 Analog-to-Digital Converter (ADC12B)

- up to 16 Channels, 12-bit ADC
- 10/12-bit resolution
- up to 1 MSample/s
- Programmable conversion sequence conversion on each channel
- Integrated temperature sensor
- Automatic calibration mode

Figure 12-2. 100-ball TFBGA Package Mechanical Drawing

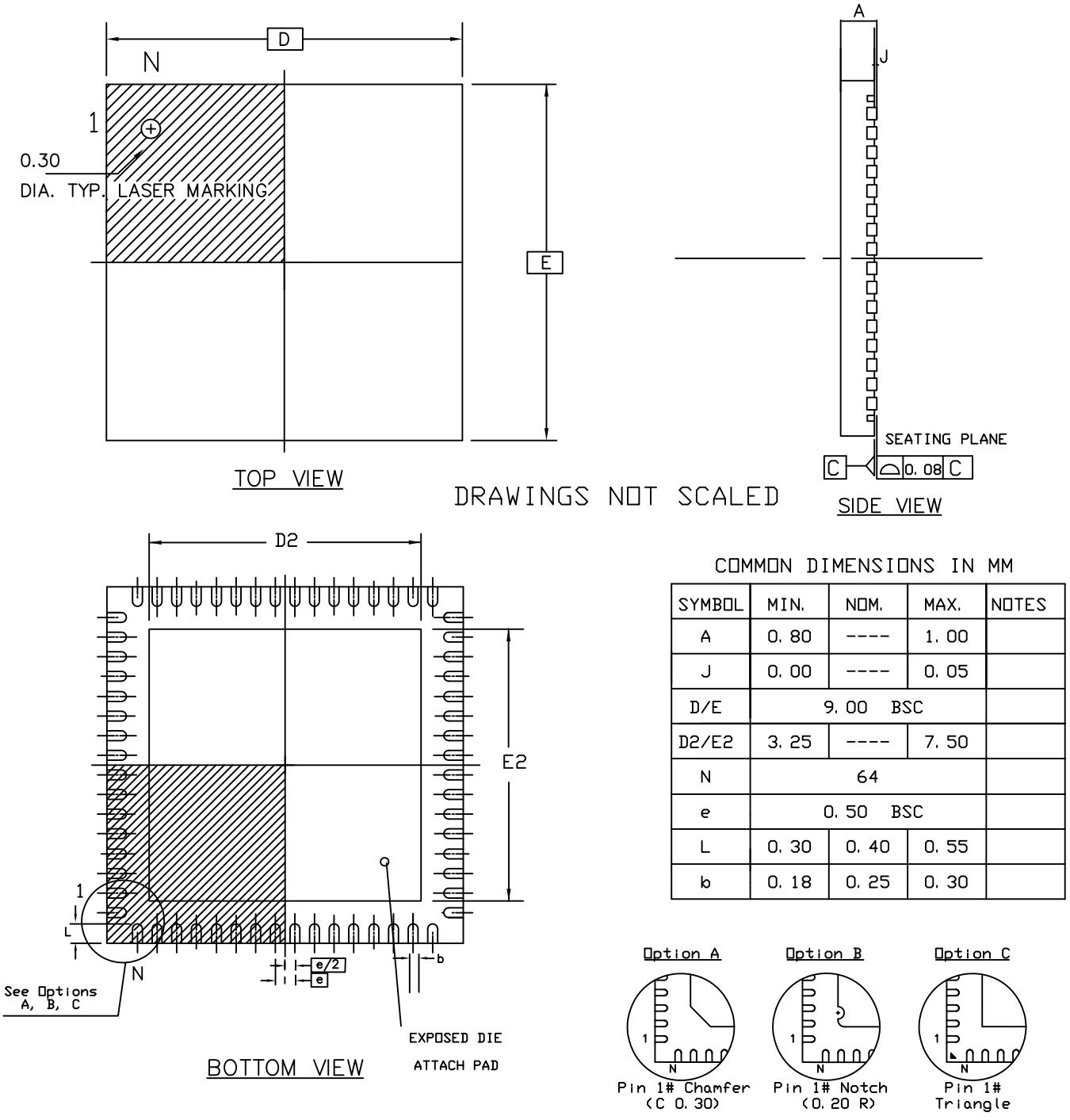


ALL DIMENSIONS ARE IN MILLIMETERS.						
SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	0.0575
A1	0.25	0.30	0.35	0.0098	0.0118	0.0138
A2	0.67	0.71	0.75	0.0264	0.0279	0.0295
A3	0.50 BASIC			0.0197 BASIC		
D	8.95	9.00	9.05	0.3524	0.3543	0.3563
D1	7.20 BASIC			0.2835 BASIC		
E	8.95	9.00	9.05	0.3524	0.3543	0.3563
E1	7.20 BASIC			0.2835 BASIC		
S	0.40 BASIC			0.0157 BASIC		
e	0.80 BASIC			0.0315 BASIC		
b	0.35	0.40	0.45	0.0138	0.0157	0.0177
aaa	0.15			0.0059		
bbb	0.20			0.0079		
ccc	0.20			0.0079		
ddd	0.12			0.0047		
eee	0.15			0.0059		
fff	0.08			0.0031		

Table 12-1. 64-lead LQFP Package Dimensions (in mm) (Continued)

Symbol	Millimeter			Inch		
	Min	**Nom**	**Max**	**Min**	**Nom**	**Max**
S	0.20	–	–	0.008	–	–
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	7.50			0.285		
E2	7.50			0.285		
Tolerances of Form and Position						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

Figure 12-4. 64-lead QFN Package Mechanical Drawing



COMMON DIMENSIONS IN MM

SYMBOL	MIN.	NOM.	MAX.	NOTES
A	0.80	----	1.00	
J	0.00	----	0.05	
D/E	9.00 BSC			
D2/E2	3.25	----	7.50	
N	64			
e	0.50 BSC			
L	0.30	0.40	0.55	
b	0.18	0.25	0.30	