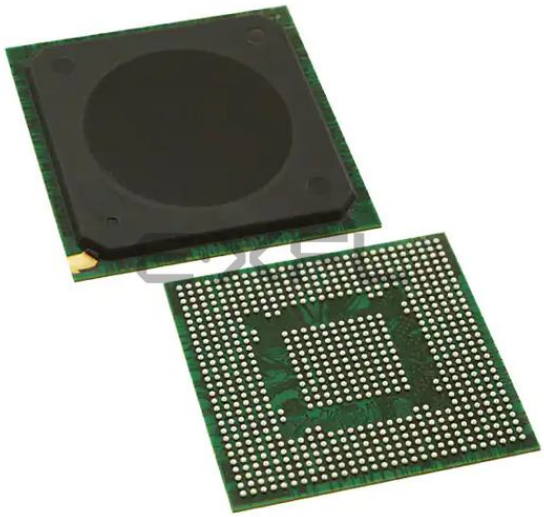

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e300c4s |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 667MHz |
| Co-Processors/DSP | - |
| RAM Controllers | DDR, DDR2 |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (2) |
| SATA | SATA 3Gbps (2) |
| USB | USB 2.0 + PHY (1) |
| Voltage - I/O | 1.8V, 2.5V, 3.3V |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Security Features | - |
| Package / Case | 689-BBGA Exposed Pad |
| Supplier Device Package | 689-TEPBGA II (31x31) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8377cvralg |

## 1.3 Dual Enhanced Three-Speed Ethernet Controllers (eTSECs)

The eTSECs include the following features:

- Two enhanced Ethernet interfaces can be used for RGMII/MII/RMII/RTBI
- Two controllers conform to IEEE Std 802.3®, IEEE 802.3u, IEEE 802.3x, IEEE 802.3z, IEEE 802.3au, IEEE 802.3ab, and IEEE Std 1588™ standards
- Support for Wake-on-Magic Packet™, a method to bring the device from standby to full operating mode
- MII management interface for external PHY control and status

## 1.4 Integrated Programmable Interrupt Controller (IPIC)

The integrated programmable interrupt controller (IPIC) implements the necessary functions to provide a flexible solution for general-purpose interrupt control. The IPIC programming model is compatible with the MPC8260 interrupt controller, and it supports 8 external and 34 internal discrete interrupt sources. Interrupts can also be redirected to an external interrupt controller.

## 1.5 Power Management Controller (PMC)

The power management controller includes the following features:

- Provides power management when the device is used in both host and agent modes
- Supports PCI Power Management 1.2 D0, D1, D2, and D3hot states
- Support for PME generation in PCI agent mode, PME detection in PCI host mode
- Supports Wake-on-LAN (Magic Packet), USB, GPIO, and PCI (PME input as host)
- Supports MPC8349E backward-compatibility mode

## 1.6 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) allows the device to exchange data between other PowerQUICC family chips, Ethernet PHYs for configuration, and peripheral devices such as EEPROMs, real-time clocks, A/D converters, and ISDN devices.

The SPI is a full-duplex, synchronous, character-oriented channel that supports a four-wire interface (receive, transmit, clock, and slave select). The SPI block consists of transmitter and receiver sections, an independent baud-rate generator, and a control unit.

## 1.7 DMA Controller, Dual $I^2C$, DUART, Enhanced Local Bus Controller (eLBC), and Timers

The device provides an integrated four-channel DMA controller with the following features:

- Allows chaining (both extended and direct) through local memory-mapped chain descriptors (accessible by local masters)
- Supports misaligned transfers

There are two $I^2C$ controllers. These synchronous, multi-master buses can be connected to additional devices for expansion and system development.

The DUART supports full-duplex operation and is compatible with the PC16450 and PC16550 programming models. 16-byte FIFOs are supported for both the transmitter and the receiver.

The main component of the enhanced local bus controller (eLBC) is its memory controller, which provides a seamless interface to many types of memory devices and peripherals. The memory controller is responsible for controlling eight memory banks shared by a NAND Flash control machine (FCM), a general-purpose chip-select machine (GPCM), and up to three user-programmable machines (UPMs). As such, it supports a minimal glue logic interface to SRAM, EPROM, NOR Flash EPROM, NAND Flash, EPROM, burstable RAM, regular DRAM devices, extended data output DRAM devices, and other peripherals. The eLBC external address latch enable (LALE) signal allows multiplexing of addresses with data signals to reduce the device pin count.

The enhanced local bus controller also includes a number of data checking and protection features, such as data parity generation and checking, write protection, and a bus monitor to ensure that each bus cycle is terminated within a user-specified period. The local bus can operate at up to 133 MHz.

The system timers include the following features: periodic interrupt timer, real time clock, software watchdog timer, and two general-purpose timer blocks.

## 1.8 Security Engine

The optional security engine is optimized to handle all the algorithms associated with IPSec, IEEE 802.11i, and iSCSI. The security engine contains one crypto-channel, a controller, and a set of crypto execution units (EUs). The execution units are as follows:

- Data encryption standard execution unit (DEU), supporting DES and 3DES
- Advanced encryption standard unit (AESU), supporting AES
- Message digest execution unit (MDEU), supporting MD5, SHA1, SHA-256, and HMAC with any algorithm
- One crypto-channel supporting multi-command descriptor chains

## 1.9 PCI Controller

The PCI controller includes the following features:

- *PCI Specification Revision 2.3* compatible
- Single 32-bit data PCI interface operates at up to 66 MHz
- PCI 3.3-V compatible (not 5-V compatible)
- Support for host and agent modes
- On-chip arbitration, supporting 5 external masters on PCI
- Selectable hardware-enforced coherency

## 4.3 eTSEC Gigabit Reference Clock Timing

This table provides the eTSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications.

**Table 9. EC_GTX_CLK125 AC Timing Specifications**

At recommended operating conditions with $LV_{DD}$ = 2.5 ± 0.125 mV/ 3.3 V ± 165 mV

| Parameter/Condition | Symbol | Min | Typical | Max | Unit | Note |
|---|---|---|---|---|---|---|
| EC_GTX_CLK125 frequency | $t_{G125}$ | — | 125 | — | MHz | — |
| EC_GTX_CLK125 cycle time | $t_{G125}$ | — | 8 | — | ns | — |
| EC_GTX_CLK rise and fall time<br>$LV_{DD}$ = 2.5 V<br>$LV_{DD}$ = 3.3 V | $t_{G125R}/t_{G125F}$ | — | — | <br>0.75<br>1.0 | ns | 1 |
| EC_GTX_CLK125 duty cycle<br>1000Base-T for RGMII, RTBI | $t_{G125H}/t_{G125}$ | <br>47 | — | <br>53 | % | 2 |
| EC_GTX_CLK125 jitter | — | — | — | ±150 | ps | 2 |

**Notes:**

1. Rise and fall times for EC_GTX_CLK125 are measured from 0.5 and 2.0 V for $LV_{DD}$ = 2.5 V and from 0.6 and 2.7 V for $LV_{DD}$ = 3.3 V.
2. EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. The EC_GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 8.2.2, "RGMII and RTBI AC Timing Specifications," for the duty cycle for 10Base-T and 100Base-T reference clock.

# 5 RESET Initialization

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the chip.

## 5.1 RESET DC Electrical Characteristics

This table provides the DC electrical characteristics for the RESET pins of the device.

**Table 10. RESET Pins DC Electrical Characteristics**

| Characteristic | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | — | 2.0 | $OV_{DD}$ + 0.3 | V |
| Input low voltage | $V_{IL}$ | — | –0.3 | 0.8 | V |
| Input current | $I_{IN}$ | — | — | ± 30 | μA |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –8.0 mA | 2.4 | — | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 8.0 mA | — | 0.5 | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 3.2 mA | — | 0.4 | V |

**Notes:**

- This table applies for pins $\overline{\text{PORESET}}$ and $\overline{\text{HRESET}}$. The $\overline{\text{PORESET}}$ is input pin, thus stated output voltages are not relevant.
- $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are open drain pin, thus $V_{OH}$ is not relevant for these pins.

## 5.2 RESET AC Electrical Characteristics

This table provides the reset initialization AC timing specifications of the device.

**Table 11. RESET Initialization Timing Specifications**

| Parameter/Condition | Min | Max | Unit | Note |
|---|---|---|---|---|
| Required assertion time of $\overline{\text{HRESET}}$ to activate reset flow | 32 | — | $t_{PCI\_SYNC\_IN}$ | 1 |
| Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to CLKIN when the device is in PCI host mode | 32 | — | $t_{CLKIN}$ | 2 |
| Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to PCI_CLK when the device is in PCI agent mode | 32 | — | $t_{PCI\_SYNC\_IN}$ | 1 |
| $\overline{\text{HRESET}}$ assertion (output) | 512 | — | $t_{PCI\_SYNC\_IN}$ | 1 |
| $\overline{\text{HRESET}}$ negation to negation (output) | 16 | — | $t_{PCI\_SYNC\_IN}$ | 1 |
| Input setup time for POR config signals (CFG_RESET_SOURCE[0:3], CFG_CLKIN_DIV, and CFG_LBMUX) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI host mode | 4 | — | $t_{CLKIN}$ | 2 |
| Input setup time for POR config signals (CFG_RESET_SOURCE[0:3], CFG_CLKIN_DIV, and CFG_LBMUX) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI agent mode | 4 | — | $t_{PCI\_SYNC\_IN}$ | 1 |
| Input hold time for POR config signals with respect to negation of $\overline{\text{HRESET}}$ | 0 | — | ns | — |
| Time for the device to turn off POR config signals with respect to the assertion of $\overline{\text{HRESET}}$ | — | 4 | ns | 3 |
| Time for the device to start driving functional output signals multiplexed with the POR configuration signals with respect to the negation of HRESET | 1 | — | $t_{PCI\_SYNC\_IN}$ | 1, 3 |

**Notes:**

1. $t_{PCI\_SYNC\_IN}$ is the clock period of the input clock applied to PCI_SYNC_IN. When the device is In PCI host mode the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. See the *MPC8379E Integrated Host Processor Reference Manual* for more details.
2. $t_{CLKIN}$ is the clock period of the input clock applied to CLKIN. It is only valid when the device is in PCI host mode. See the *MPC8379E Integrated Host Processor Reference Manual* for more details.
3. POR config signals consists of CFG_RESET_SOURCE[0:3], CFG_LBMUX, and CFG_CLKIN_DIV.

Table 12 provides the PLL lock times.

**Table 12. PLL Lock Times**

| Parameter | Min | Max | Unit | Note |
|---|---|---|---|---|
| PLL lock times | — | 100 | μs | — |

**Note:**

- The device guarantees the PLL lock if the clock settings are within spec range. The core clock also depends on the core PLL ratio. See Section 23, “Clocking,” for more information.

# 6 DDR1 and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the chip. Note that DDR1 SDRAM is $GV_{DD}$(typ) = 2.5 V and DDR2 SDRAM is $GV_{DD}$(typ) = 1.8 V.

**Table 21. DDR1 and DDR2 SDRAM Output AC Timing Specifications (continued)**

| Parameter | Symbol[1] | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| MDQS epilogue end | $t_{DDKHME}$ | –0.6 | 0.6 | ns | 6, 8 |

**Notes:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, $t_{DDKHAS}$ symbolizes DDR timing (DD) for the time $t_{MCK}$ memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, $t_{DDKLDX}$ symbolizes DDR timing (DD) for the time $t_{MCK}$ memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ//MDM/MDQS.
4. Note that $t_{DDKHMH}$ follows the symbol conventions described in Note 1. For example, $t_{DDKHMH}$ describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). $t_{DDKHMH}$ can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8379E PowerQUICC II Pro Host Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data MDQ, ECC, or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK*n* at the pins of the microprocessor. Note that $t_{DDKHMP}$ follows the symbol conventions described in Note 1.
7. Clock Control register is set to adjust the memory clocks by 1/2 the applied cycle.
8. See AN3665, “MPC837xE Design Checklist,” for proper DDR termination.

The minimum frequency for DDR2 is 250 MHz data rate (125 MHz clock), 167 MHz data rate (83 MHz clock) for DDR1. This figure shows the DDR1 and DDR2 SDRAM output timing for the MCK to MDQS skew measurement ($t_{DDKHMH}$).

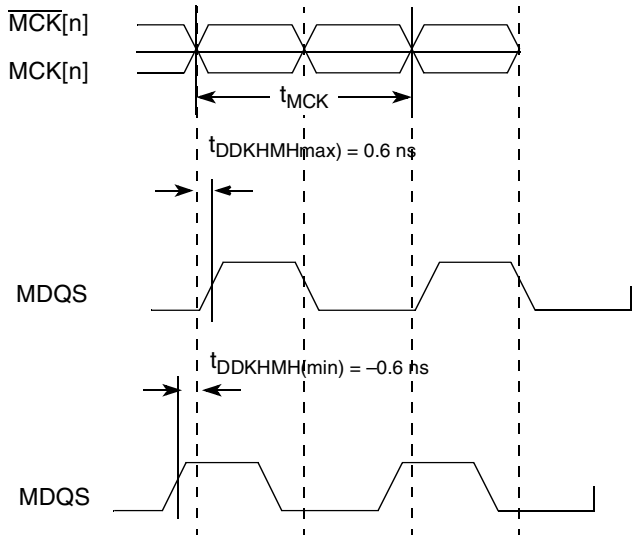



**Figure 4. DDR Timing Diagram for $t_{DDKHMH}$**

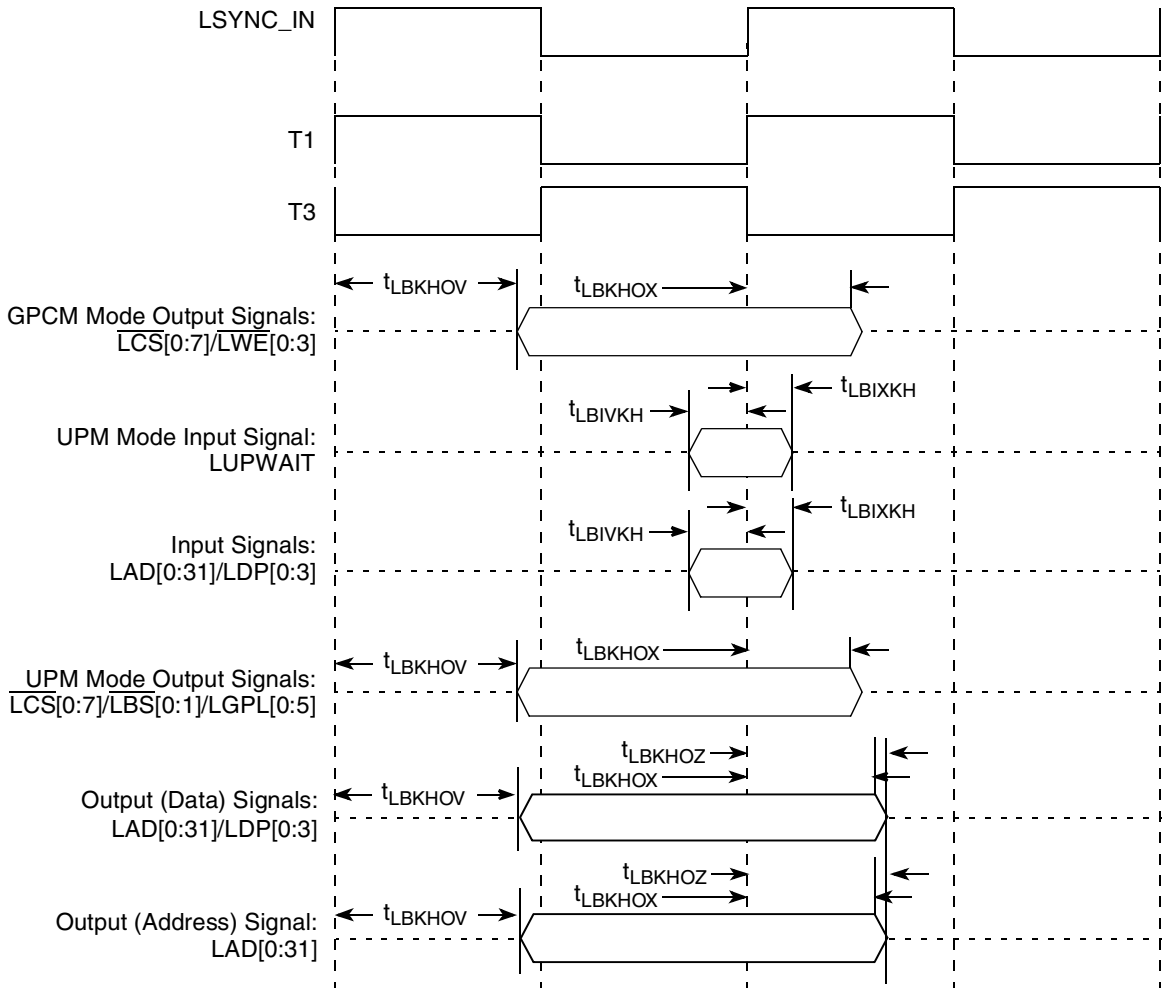



**Figure 22. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (PLL Enable Mode)**

### 15.4.1 Differential Transmitter (Tx) Output

This table defines the specifications for the differential output at all transmitters. The parameters are specified at the component pins.

**Table 52. Differential Transmitter (Tx) Output Specifications**

| Parameter | Conditions | Symbol | Min | Typical | Max | Units | Note |
|---|---|---|---|---|---|---|---|
| Unit interval | Each $U_{PETX}$ is 400 ps ± 300 ppm. $U_{PETX}$ does not account for Spread Spectrum Clock dictated variations. | UI | 399.88 | 400 | 400.12 | ps | 1 |
| Differential peak-to-peak output voltage | $V_{PEDPPTX} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$ | $V_{TX-DIFFp-p}$ | 0.8 | — | 1.2 | V | 2 |
| De-emphasized differential output voltage (ratio) | Ratio of the $V_{PEDPPTX}$ of the second and following bits after a transition divided by the $V_{PEDPPTX}$ of the first bit after a transition. | $V_{TX-DE-RATIO}$ | –3.0 | –3.5 | –4.0 | dB | 2 |
| Minimum Tx eye width | The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - U_{PEEWTX}$= 0.3 UI. | $T_{TX-EYE}$ | 0.70 | — | — | UI | 2, 3 |
| Maximum time between the jitter median and maximum deviation from the median | Jitter is defined as the measurement variation of the crossing points ($V_{PEDPPTX}$ = 0 V) in relation to a recovered Tx UI. A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI. | $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ | — | — | 0.15 | UI | 2, 3 |
| D+/D– Tx output rise/fall time | — | $T_{TX-RISE}$, $T_{TX-FALL}$ | 0.125 | — | — | UI | 2, 5 |
| RMS AC peak common mode output voltage | $V_{PEACPCMTX} = RMS(\lvert V_{TXD+} - V_{TXD-} \rvert/2 - V_{TX-CM-DC})$ $V_{TX-CM-DC} = DC_{(avg)}$ of $\lvert V_{TX-D+} - V_{TX-D-} \rvert/2$ | $V_{TX-CM-ACp}$ | — | — | 20 | mV | 2 |
| Absolute delta of DC common mode voltage during LO and electrical idle | $\lvert V_{TX-CM-DC\ (during\ LO)} - V_{TX-CM-Idle-DC\ (During\ Electrical\ Idle)} \rvert <= 100$ mV $V_{TX-CM-DC} = DC_{(avg)}$ of $\lvert V_{TX-D+} - V_{TX-D-} \rvert/2$ [LO] $V_{TX-CM-Idle-DC} = DC_{(avg)}$ of $\lvert V_{TX-D+} - V_{TX-D-} \rvert/2$ [Electrical Idle] | $V_{TX-CM-DC-\ ACTIVE-IDLE-DELTA}$ | 0 | — | 100 | mV | 2 |

**Table 53. Differential Receiver (Rx) Input Specifications (continued)**

| Parameter | Comments | Symbol | Min | Typical | Max | Units | Note |
|---|---|---|---|---|---|---|---|
| Minimum receiver eye width | The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER} = 1 - U_{PEEWRX} = 0.6$ UI. | $T_{RX-EYE}$ | 0.4 | — | — | UI | 2, 3 |
| Maximum time between the jitter median and maximum deviation from the median. | Jitter is defined as the measurement variation of the crossing points ($V_{PEDPPRX} = 0$ V) in relation to a recovered Tx UI. A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI. | $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ | — | — | 0.3 | UI | 2, 3, 7 |
| AC peak common mode input voltage | $V_{PEACPCMRX} = \lvert V_{RXD+} - V_{RXD-}\rvert/2 - V_{RX-CM-DC}$ $V_{RX-CM-DC} = DC_{(avg)}$ of $\lvert V_{RX-D+} - V_{RX-D-}\rvert/2$ | $V_{RX-CM-ACp}$ | — | — | 150 | mV | 2 |
| Differential return loss | Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at +300 mV and –300 mV, respectively. | $RL_{RX-DIFF}$ | 10 | — | — | dB | 4 |
| Common mode return loss | Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at 0 V. | $RL_{RX-CM}$ | 6 | — | — | dB | 4 |
| DC differential input impedance | RX DC differential mode impedance. | $Z_{RX-DIFF-DC}$ | 80 | 100 | 120 | Ω | 5 |
| DC Input Impedance | Required RX D+ as well as D- DC impedance (50 ± 20% tolerance). | $Z_{RX-DC}$ | 40 | 50 | 60 | Ω | 2, 5 |
| Powered down DC input impedance | Required RX D+ as well as D– DC impedance when the receiver terminations do not have power. | $Z_{RX-HIGH-IMP-DC}$ | 200 k | — | — | Ω | 6 |
| Electrical idle detect threshold | $V_{PEEIDT} = 2 \times \lvert V_{RX-D+} - V_{RX-D-}\rvert$ Measured at the package pins of the receiver | $V_{RX-IDLE-DET-DIFF\ p-p}$ | 65 | — | 175 | mV | — |

**Table 54. SATA Reference Clock Input Requirements (continued)**

| Parameter | Condition | Symbol | Min | Typical | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ cycle to cycle Clock jitter (period jitter) | Cycle-to-cycle at ref clock input | $t_{CLK\_CJ}$ | — | — | 100 | ps | — |
| SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ total reference clock jitter, phase jitter (peak-peak) | Peak-to-peak jitter at ref clock input | $t_{CLK\_PJ}$ | –50 | — | +50 | ps | 2, 3 |

**Notes:**
1. Only 100/125/150 MHz have been tested, other in between values will not work correctly with the rest of the system.
2. In a frequency band from 150 kHz to 15 MHz at BER of $10^{-12}$.
3. Total peak to peak Deterministic Jitter "$D_J$" should be less than or equal to 50 ps.

This figure shows the SATA reference clock timing waveform.

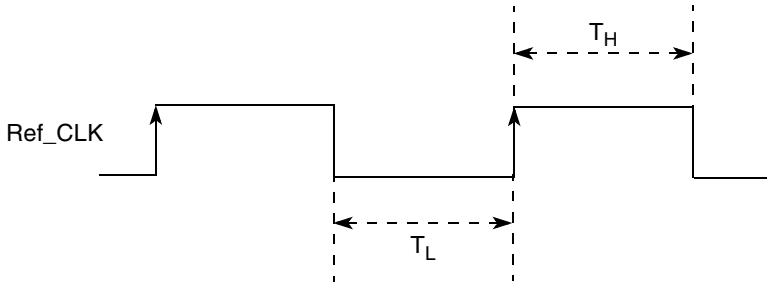



**Figure 45. SATA Reference Clock Timing Waveform**

## 16.2 Transmitter (Tx) Output Characteristics

This section discusses the Gen1i/1.5G and Gen2i/3G transmitter output characteristics for the SATA interface.

### 16.2.1 Gen1i/1.5G Transmitter Specifications

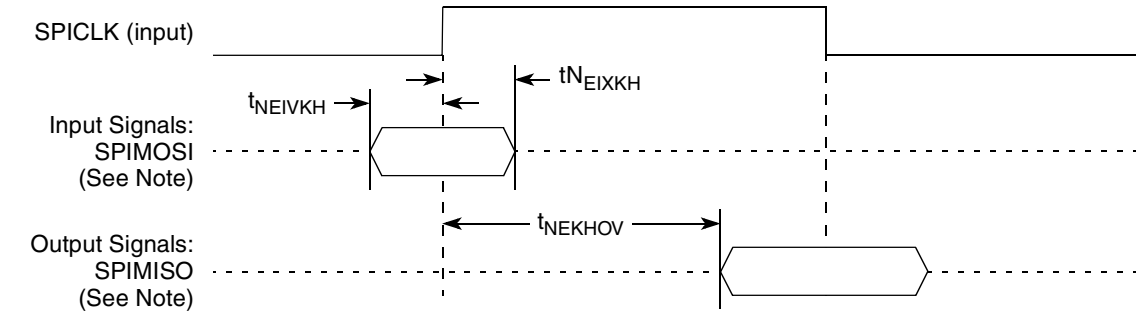
This table provides the DC differential transmitter output DC characteristics for the SATA interface at Gen1i or 1.5 Gbits/s transmission.

**Table 55. Gen1i/1.5G Transmitter (Tx) DC Specifications**

| Parameter | Symbol | Min | Typical | Max | Units | Note |
|---|---|---|---|---|---|---|
| Tx differential output voltage | $V_{SATA\_TXDIFF}$ | 400 | 500 | 600 | $mV_{p-p}$ | 1 |
| Tx differential pair impedance | $Z_{SATA\_TXDIFFIM}$ | 85 | 100 | 115 | Ω | — |

**Note:**
1. Terminated by 50 Ω load.

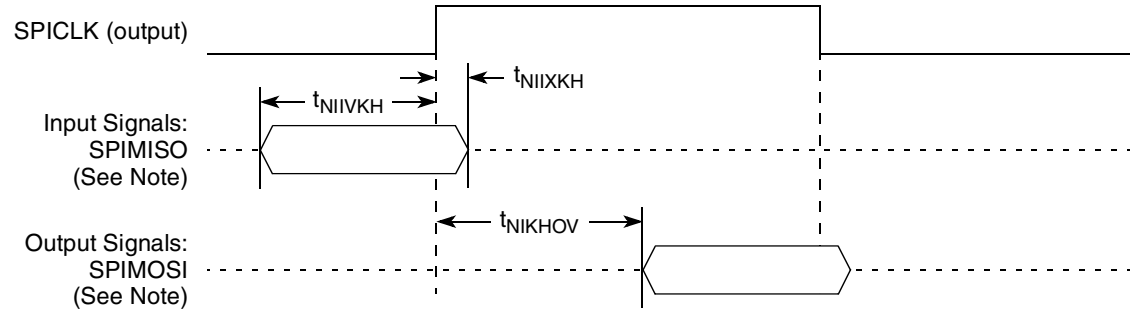
This figure shows the SPI timing in slave mode (external clock).




**Note:** The clock edge is selectable on SPI.

**Figure 49. SPI AC Timing in Slave Mode (External Clock) Diagram**

This figure shows the SPI timing in master mode (internal clock).




**Note:** The clock edge is selectable on SPI.

**Figure 50. SPI AC Timing in Master Mode (Internal Clock) Diagram**

# 21 High-Speed Serial Interfaces (HSSI)

This chip features two serializer/deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications. See Table 1 for the interfaces supported.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

## 21.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 51 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (SD*n*_TX and $\overline{\text{SD}n\text{\_TX}}$) or a receiver input (SD*n*_RX and $\overline{\text{SD}n\text{\_RX}}$). Each signal swings between A volts and B volts where A > B.

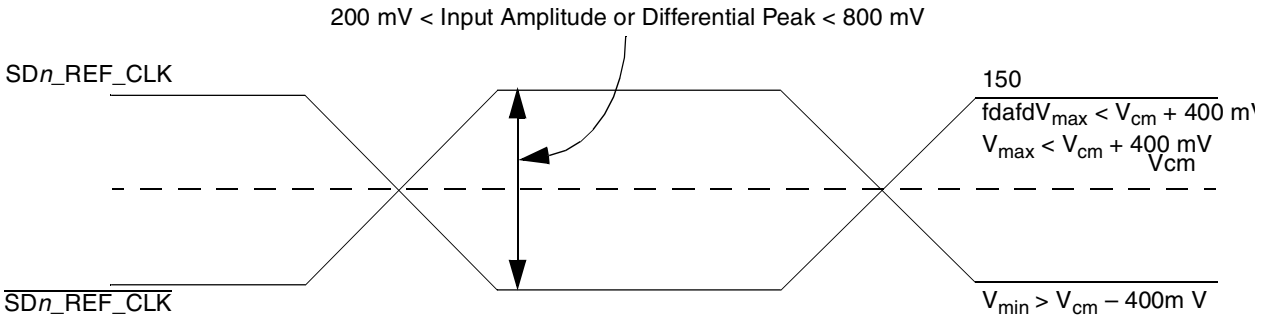



**Figure 54. Differential Reference Clock Input DC Requirements (External AC-Coupled)**

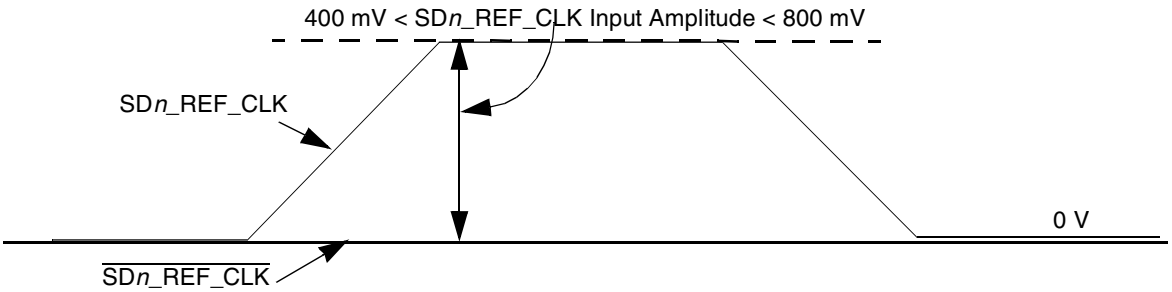



**Figure 55. Single-Ended Reference Clock Input DC Requirements**

## 21.2.3 Interfacing With Other Differential Signaling Levels

The following list provides information about interfacing with other differential signaling levels.

- With on-chip termination to SGND_SRDS*n* (xcorevss), the differential reference clocks inputs are HCSL (high-speed current steering logic) compatible DC-coupled.
- Many other low voltage differential type outputs like LVDS (low voltage differential signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 mV to 400 mV) for DC-coupled connection.
- LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

**Table 72. TePBGA II Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| MBA2 | M3 | O | GVDD | — |
| MCAS_B | W5 | O | GVDD | — |
| MCK_B0 | H1 | O | GVDD | — |
| MCK_B1 | K1 | O | GVDD | — |
| MCK_B2 | V1 | O | GVDD | — |
| MCK_B3 | W2 | O | GVDD | — |
| MCK_B4 | AA1 | O | GVDD | — |
| MCK_B5 | AB2 | O | GVDD | — |
| MCK0 | J1 | O | GVDD | — |
| MCK1 | L1 | O | GVDD | — |
| MCK2 | V2 | O | GVDD | — |
| MCK3 | W1 | O | GVDD | — |
| MCK4 | Y1 | O | GVDD | — |
| MCK5 | AB1 | O | GVDD | — |
| MCKE0 | M4 | O | GVDD | 3 |
| MCKE1 | R5 | O | GVDD | 3 |
| MCS_B0 | W3 | O | GVDD | — |
| MCS_B1 | P3 | O | GVDD | — |
| MCS_B2 | T4 | O | GVDD | — |
| MCS_B3 | R4 | O | GVDD | — |
| MDIC0 | AH8 | I/O | GVDD | 9 |
| MDIC1 | AJ8 | I/O | GVDD | 9 |
| MDM0 | B6 | O | GVDD | — |
| MDM1 | B2 | O | GVDD | — |
| MDM2 | E2 | O | GVDD | — |
| MDM3 | E1 | O | GVDD | — |
| MDM4 | Y6 | O | GVDD | — |
| MDM5 | AC6 | O | GVDD | — |
| MDM6 | AE6 | O | GVDD | — |
| MDM7 | AJ4 | O | GVDD | — |
| MDM8 | L6 | O | GVDD | — |
| MDQ0 | A8 | I/O | GVDD | 11 |
| MDQ1 | A6 | I/O | GVDD | 11 |

**Table 72. TePBGA II Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| UART_RTS_B[2] | L29 | O | OVDD | — |
| **Enhanced Local Bus Controller (eLBC) Interface** | | | | |
| LAD0 | E24 | I/O | LBVDD | — |
| LAD1 | G28 | I/O | LBVDD | — |
| LAD2 | H25 | I/O | LBVDD | — |
| LAD3 | F26 | I/O | LBVDD | — |
| LAD4 | C26 | I/O | LBVDD | — |
| LAD5 | J28 | I/O | LBVDD | — |
| LAD6 | F21 | I/O | LBVDD | — |
| LAD7 | F23 | I/O | LBVDD | — |
| LAD8 | E25 | I/O | LBVDD | — |
| LAD9 | E26 | I/O | LBVDD | — |
| LAD10 | A23 | I/O | LBVDD | — |
| LAD11 | F24 | I/O | LBVDD | — |
| LAD12 | G24 | I/O | LBVDD | — |
| LAD13 | F25 | I/O | LBVDD | — |
| LAD14 | H28 | I/O | LBVDD | — |
| LAD15 | G25 | I/O | LBVDD | — |
| LA11/LAD16 | F27 | I/O | LBVDD | — |
| LA12/LAD17 | B21 | I/O | LBVDD | — |
| LA13/LAD18 | A25 | I/O | LBVDD | — |
| LA14/LAD19 | C28 | I/O | LBVDD | — |
| LA15/LAD20 | H24 | I/O | LBVDD | — |
| LA16/LAD21 | E23 | I/O | LBVDD | — |
| LA17/LAD22 | B28 | I/O | LBVDD | — |
| LA18/LAD23 | D28 | I/O | LBVDD | — |
| LA19/LAD24 | A27 | I/O | LBVDD | — |
| LA20/LAD25 | C25 | I/O | LBVDD | — |
| LA21/LAD26 | B27 | I/O | LBVDD | — |
| LA22/LAD27 | H27 | I/O | LBVDD | — |
| LA23/LAD28 | E21 | I/O | LBVDD | — |
| LA24/LAD29 | F20 | I/O | LBVDD | — |

**Table 72. TePBGA II Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| **eTSEC1/GPIO1/GPIO2/CFG_RESET Interface** | | | | |
| TSEC1_COL/GPIO2[20] | AF22 | I/O | LVDD1 | 16 |
| TSEC1_CRS/GPIO2[21] | AE20 | I/O | LVDD1 | 16 |
| TSEC1_GTX_CLK | AJ25 | O | LVDD1 | 16 |
| TSEC1_RX_CLK | AG22 | I | LVDD1 | 16 |
| TSEC1_RX_DV | AD19 | I | LVDD1 | 16 |
| TSEC1_RX_ER/GPIO2[25] | AD20 | I/O | LVDD1 | 16 |
| TSEC1_RXD0 | AD22 | I | LVDD1 | 16 |
| TSEC1_RXD1 | AE21 | I | LVDD1 | 16 |
| TSEC1_RXD2 | AE22 | I | LVDD1 | 16 |
| TSEC1_RXD3 | AD21 | I | LVDD1 | 16 |
| TSEC1_TX_CLK | AJ22 | I | LVDD1 | 16 |
| TSEC1_TX_EN | AG23 | O | LVDD1 | 16 |
| TSEC1_TX_ER/CFG_LBMUX | AH22 | I/O | LVDD1 | 16 |
| TSEC1_TXD0/ CFG_RESET_SOURCE[0] | AD23 | I/O | LVDD1 | 16 |
| TSEC1_TXD1/ CFG_RESET_SOURCE[1] | AE23 | I/O | LVDD1 | 16 |
| TSEC1_TXD2/ CFG_RESET_SOURCE[2] | AF23 | I/O | LVDD1 | 16 |
| TSEC1_TXD3/ CFG_RESET_SOURCE[3] | AJ24 | I/O | LVDD1 | 16 |
| EC_GTX_CLK125 | AH24 | I | LVDD1 | 16 |
| EC_MDC/CFG_CLKIN_DIV | AJ21 | I/O | LVDD1 | 16 |
| EC_MDIO | AH21 | I/O | LVDD1 | 16 |
| **eTSEC2/GPIO1 Interface** | | | | |
| TSEC2_COL/GPIO1[21]/ TSEC1_TMR_TRIG1 | AJ27 | I/O | LVDD2 | 16 |
| TSEC2_CRS/GPIO1[22]/ TSEC1_TMR_TRIG2 | AG29 | I/O | LVDD2 | 16 |
| TSEC2_GTX_CLK | AF28 | O | LVDD2 | 16 |
| TSEC2_RX_CLK/ TSEC1_TMR_CLK | AF25 | I | LVDD2 | 16 |
| TSEC2_RX_DV/GPIO1[23] | AF26 | I/O | LVDD2 | 16 |
| TSEC2_RX_ER/GPIO1[25] | AG25 | I/O | LVDD2 | 16 |

**Table 72. TePBGA II Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| TSEC2_RXD0/GPIO1[16] | AE28 | I/O | LVDD2 | 16 |
| TSEC2_RXD1/GPIO1[15] | AE29 | I/O | LVDD2 | 16 |
| TSEC2_RXD2/GPIO1[14] | AH26 | I/O | LVDD2 | 16 |
| TSEC2_RXD3/GPIO1[13] | AH25 | I/O | LVDD2 | 16 |
| TSEC2_TX_CLK/GPIO2[24]/ TSEC1_TMR_GCLK | AG28 | I/O | LVDD2 | 16 |
| TSEC2_TX_EN/GPIO1[12]/ TSEC1_TMR_ALARM2 | AJ26 | I/O | LVDD2 | 16 |
| TSEC2_TX_ER/GPIO1[24]/ TSEC1_TMR_ALARM1 | AG26 | I/O | LVDD2 | 16 |
| TSEC2_TXD0/GPIO1[20] | AH28 | I/O | LVDD2 | 16 |
| TSEC2_TXD1/GPIO1[19]/ TSEC1_TMR_PP1 | AF27 | I/O | LVDD2 | 16 |
| TSEC2_TXD2/GPIO1[18]/ TSEC1_TMR_PP2 | AJ28 | I/O | LVDD2 | 16 |
| TSEC2_TXD3/GPIO1[17]/ TSEC1_TMR_PP3 | AF29 | I/O | LVDD2 | 16 |
| **GPIO1 Interface** | | | | |
| GPIO1[0]/GTM1_TIN1/ GTM2_TIN2/DREQ0_B | P25 | I/O | OVDD | — |
| GPIO1[1]/GTM1_TGATE1_B/ GTM2_TGATE2_B/DACK0_B | N25 | I/O | OVDD | — |
| GPIO1[2]/GTM1_TOUT1_B/ DDONE0_B | N26 | I/O | OVDD | — |
| GPIO1[3]/GTM1_TIN2/ GTM2_TIN1/DREQ1_B | B9 | I/O | OVDD | — |
| GPIO1[4]/GTM1_TGATE2_B/ GTM2_TGATE1_B/DACK1_B | N29 | I/O | OVDD | — |
| GPIO1[5]/GTM1_TOUT2_B/ GTM2_TOUT1_B/DDONE1_B | M29 | I/O | OVDD | — |
| GPIO1[6]/GTM1_TIN3/ GTM2_TIN4/DREQ2_B | A9 | I/O | OVDD | — |
| GPIO1[7]/GTM1_TGATE3_B/ GTM2_TGATE4_B/DACK2_B | B10 | I/O | OVDD | — |
| GPIO1[8]/GTM1_TOUT3_B/ DDONE2_B | J26 | I/O | OVDD | — |
| GPIO1[9]/GTM1_TIN4/ GTM2_TIN3/DREQ3_B | J24 | I/O | OVDD | — |

**Table 72. TePBGA II Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| **Programmable Interrupt Controller (PIC) Interface** | | | | |
| MCP_OUT_B | AD14 | O | OVDD | 2 |
| IRQ_B0/MCP_IN_B/GPIO2[12] | F9 | I/O | OVDD | — |
| IRQ_B1/GPIO2[13] | E9 | I/O | OVDD | — |
| IRQ_B2/GPIO2[14] | F10 | I/O | OVDD | — |
| IRQ_B3/GPIO2[15] | D9 | I/O | OVDD | — |
| IRQ_B4/GPIO2[16]/SD_WP | C9 | I/O | OVDD | — |
| IRQ_B5/GPIO2[17]/ USBDR_PWRFAULT | AE10 | I/O | OVDD | — |
| IRQ_B6/GPIO2[18] | AD10 | I/O | OVDD | — |
| IRQ_B7/GPIO2[19] | AD9 | I/O | OVDD | — |
| **PMC Interface** | | | | |
| QUIESCE_B | D13 | O | OVDD | — |
| **SerDes1 Interface** | | | | |
| L1_SD_IMP_CAL_RX | AJ14 | I | L1_XPADVDD | — |
| L1_SD_IMP_CAL_TX | AG19 | I | L1_XPADVDD | — |
| L1_SD_REF_CLK | AJ17 | I | L1_XPADVDD | — |
| L1_SD_REF_CLK_B | AH17 | I | L1_XPADVDD | — |
| L1_SD_RXA_N | AJ15 | I | L1_XPADVDD | — |
| L1_SD_RXA_P | AH15 | I | L1_XPADVDD | — |
| L1_SD_RXE_N | AJ19 | I | L1_XPADVDD | — |
| L1_SD_RXE_P | AH19 | I | L1_XPADVDD | — |
| L1_SD_TXA_N | AF15 | O | L1_XPADVDD | — |
| L1_SD_TXA_P | AE15 | O | L1_XPADVDD | — |
| L1_SD_TXE_N | AF18 | O | L1_XPADVDD | — |
| L1_SD_TXE_P | AE18 | O | L1_XPADVDD | — |
| L1_SDAVDD_0 | AJ18 | SerDes PLL Power (1.0 or 1.05 V) | — | — |
| L1_SDAVSS_0 | AG17 | SerDes PLL GND | — | — |
| L1_XCOREVDD | AH14, AJ16, AF17, AH20, AJ20 | SerDes Core Power (1.0 or 1.05 V) | — | — |

**Table 81. Package Thermal Characteristics for TePBGA II (continued)**

| Parameter | Symbol | Value | Unit | Note |
|---|---|---|---|---|
| Junction-to-package natural convection on top | $\psi_{JT}$ | 6 | °C/W | 6 |

**Notes:**
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

## 24.2 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$ where $P_{I/O}$ is the power dissipation of the I/O drivers.

### 24.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, $T_J$, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

$T_J$ = junction temperature (°C)

$T_A$ = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

$P_D$ = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Generally, the value obtained on a single layer board is appropriate for a tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

### 24.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

**NOTE**

The heat sink cannot be mounted on the package.

Tyco Electronics
Chip Coolers™
www.chipcoolers.com

Wakefield Engineering
www.wakefield.com

Interface material vendors include the following:

Chomerics, Inc.
www.chomerics.com

Dow-Corning Corporation
Dow-Corning Electronic Materials
www.dowcorning.com

Shin-Etsu MicroSi, Inc.
www.microsi.com

The Bergquist Company
www.bergquistcompany.com

## 24.3 Heat Sink Attachment

The device requires the use of heat sinks. When heat sinks are attached, an interface material is required, preferably thermal grease and a spring clip. The spring clip should connect to the printed circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces that can lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. The recommended maximum compressive force on the top of the package is 10 lb force (4.5 kg force). Any adhesive attachment should attach to painted or plastic surfaces, and its performance should be verified under the application requirements.

### 24.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When a heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimize the size of the clearance to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction to case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

where:

$T_J$ = junction temperature (°C)

$T_C$ = case temperature of the package (°C)

## 26.1 Part Numbers Fully Addressed by This Document

Table 84 provides the Freescale part numbering nomenclature for this chip. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

**Table 84. Part Numbering Nomenclature**

| MPC | *8377* | *E* | *C* | *ZQ* | *AF* | *D* | *A* |
|---|---|---|---|---|---|---|---|
| **Product Code** | **Part Identifier** | **Encryption Acceleration** | **Temperature Range [1]** | **Package [2]** | **e300 core Frequency [3]** | **DDR Data Rate** | **Revision Level [4]** |
| MPC | 8377 | Blank = Not included<br>E = included | Blank = 0°C ($T_a$) to 125°C ($T_j$)<br>C = –40°C ($T_a$) to 125°C ($T_j$) | VR = Pb-free 689 TePBGA II | AN = 800 MHz<br>AL = 667 MHz<br>AJ = 533 MHz<br>AG = 400 MHz | G = 400 MHz<br>F = 333 MHz<br>D = 266 MHz | Blank = Freescale ATMC fab<br>A = GlobalFoundries fab |

**Note:**

1 Contact local Freescale office on availability of parts with an extended temperature range.

2 See Section 22, "Package and Pin Listings," for more information on the available package type.

3 Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.

4 No design changes occurred between initial parts and the revision "*A*" parts. Only the fab source has changed in moving to revision "*A*" parts. Initial revision parts and revision "*A*" parts are form, fit, function, and reliability equivalent.

This table lists the available core and DDR data rate frequency combinations.

**Table 85. Available Parts (Core/DDR Data Rate)**

| MPC8377E | MPC8378E | MPC8379E |
|---|---|---|
| 800 MHz/400 MHz | 800 MHz/400 MHz | 800 MHz/400 MHz |
| 667 MHz/400 MHz | 667 MHz/400 MHz | 667 MHz/400 MHz |
| 533 MHz/333 MHz | 533 MHz/333 MHz | 533 MHz/333 MHz |
| 400 MHz/266 MHz | 400 MHz/266 MHz | 400 MHz/266 MHz |

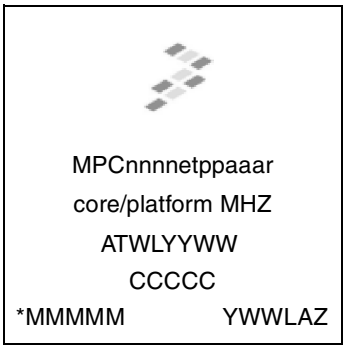
This table shows the SVR and PVR settings by device.

**Table 86. SVR and PVR Settings by Product Revision**

| Device | Package | SVR | | PVR | |
|---|---|---|---|---|---|
| | | Rev 1.0 | Rev. 2.1 | Rev. 1.0 | Rev. 2.1 |
| MPC8377 | TePBGA II | 0x80C7_0010 | 0x80C7_0021 | 0x8086_1010 | 0x8086_1011 |
| MPC8377E | | 0x80C6_0010 | 0x80C6_0021 | | |
| MPC8378 | | 0x80C5_0010 | 0x80C5_0021 | | |
| MPC8378E | | 0x80C4_0010 | 0x80C4_0021 | | |
| MPC8379 | | 0x80C3_0010 | 0x80C3_0021 | | |
| MPC8379E | | 0x80C2_0010 | 0x80C2_0021 | | |

## 26.2 Part Marking

Parts are marked as in the example as shown in this figure.

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Notes:
ATWLYYWW is the traceability code.
CCCCC is the country code.
MMMMM is the mask number.
YWWLAZ is the assembly traceability code.

**Figure 67. Freescale Part Marking for TePBGA II Devices**

# 27 Document Revision History

This table provides a revision history for this document.

**Table 87. Document Revision History**

| Revision | Date | Substantive Change(s) |
|---|---|---|
| 8 | 05/2012 | In Table 15, “DDR SDRAM DC Electrical Characteristics for $GV_{DD}$ (typ) = 2.5 V,” updated Output leakage current ($I_{OZ}$) min and max values. |
| 7 | 10/2011 | • In Table 84, “Part Numbering Nomenclature,” updated “Revision Level description”and added footnote 4.In Section 21.2.4, “AC Requirements for SerDes Reference Clocks,” modified the introductory sentence for Table 71, “SerDes Reference Clock Common AC Parameters.” |