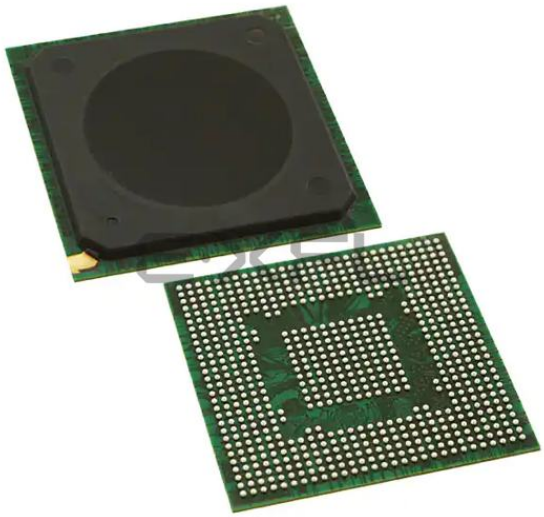

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c4s
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	667MHz
Co-Processors/DSP	Security; SEC 3.0
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 125°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	689-BBGA Exposed Pad
Supplier Device Package	689-TEPBGA II (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8377ecvralg

controller, dual I^2C controllers, a 4-channel DMA controller, an enhanced secured digital host controller, and a general-purpose I/O port. This figure shows the block diagram of the chip.

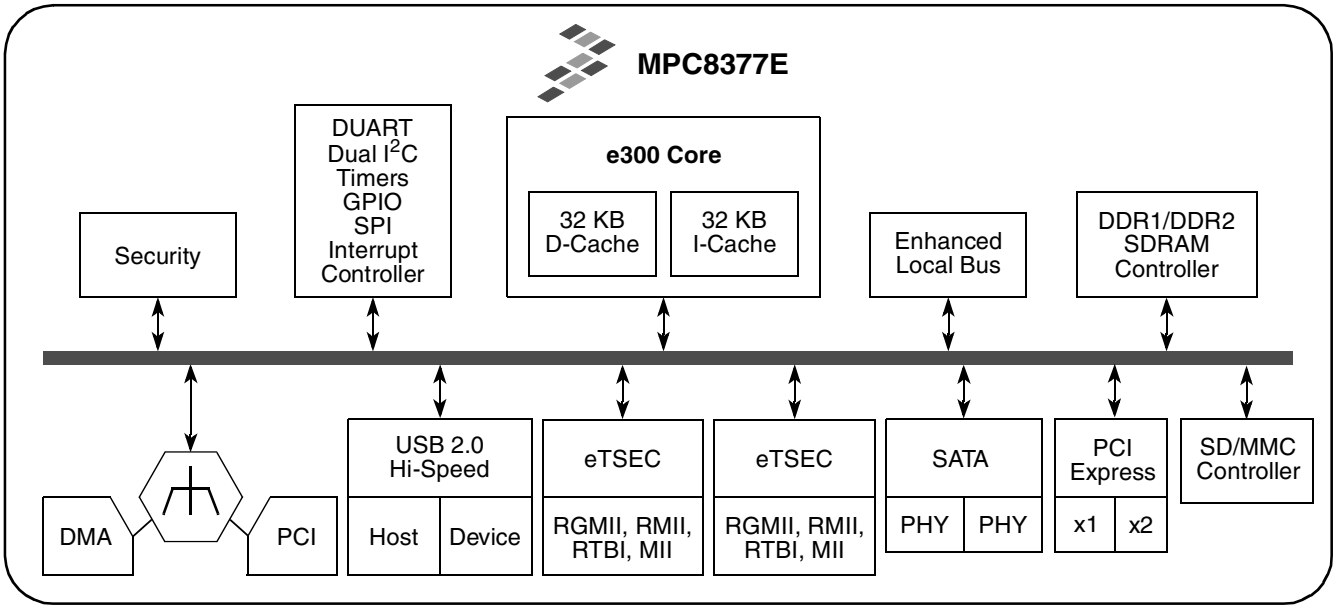


Figure 1. MPC8377E Block Diagram and Features

The following features are supported in the chip:

- e300c4s core built on Power Architecture® technology with 32 KB instruction cache and 32 KB data cache, a floating point unit, and two integer units
- DDR1/DDR2 memory controller supporting a 32/64-bit interface
- Peripheral interfaces, such as a 32-bit PCI interface with up to 66-MHz operation
- 32-bit local bus interface running up to 133-MHz
- USB 2.0 (full/high speed) support
- Power management controller for low-power consumption
- High degree of software compatibility with previous-generation PowerQUICC processor-based designs for backward compatibility and easier software migration
- Optional security engine provides acceleration for control and data plane security protocols

The optional security engine (SEC 3.0) is noted with the extension “E” at the end. It allows CPU-intensive cryptographic operations to be offloaded from the main CPU core. The security-processing accelerator provides hardware acceleration for the DES, 3DES, AES, SHA-1, and MD-5 algorithms.

Table 21. DDR1 and DDR2 SDRAM Output AC Timing Specifications (continued)

Parameter	Symbol[1]	Min	Max	Unit	Note
MDQS epilogue end	t_{DDKHME}	–0.6	0.6	ns	6, 8

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ//MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in Note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8379E PowerQUICC II Pro Host Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data MDQ, ECC, or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK*n* at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in Note 1.
7. Clock Control register is set to adjust the memory clocks by 1/2 the applied cycle.
8. See AN3665, “MPC837xE Design Checklist,” for proper DDR termination.

The minimum frequency for DDR2 is 250 MHz data rate (125 MHz clock), 167 MHz data rate (83 MHz clock) for DDR1. This figure shows the DDR1 and DDR2 SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

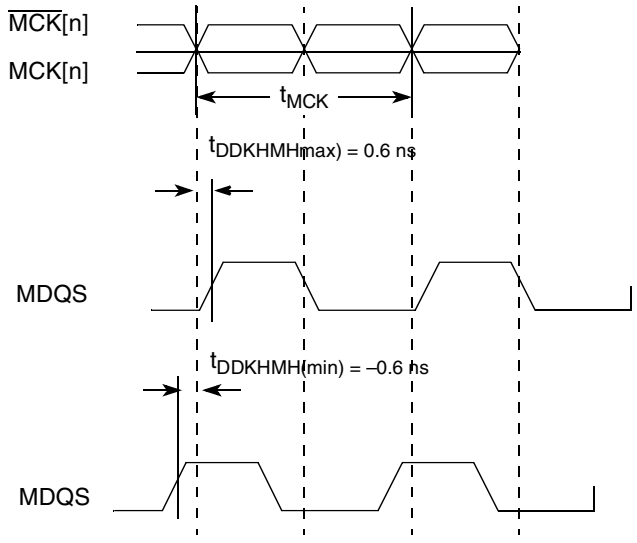


Figure 4. DDR Timing Diagram for t_{DDKHMH}

8.2.3 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.3.1 RMII Transmit AC Timing Specifications

This table shows the RMII transmit AC timing specifications.

Table 29. RMII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter	Symbol[1]	Min	Typical	Max	Unit
REF_CLK clock period	t_{RMT}	15.0	20.0	25.0	ns
REF_CLK duty cycle	t_{RMTH}	35	50	65	%
REF_CLK peak-to-peak jitter	t_{RMTJ}	—	—	250	ps
Rise time REF_CLK (20%–80%)	t_{RMTR}	1.0	—	2.0	ns
Fall time REF_CLK (80%–20%)	t_{RMTF}	1.0	—	2.0	ns
REF_CLK to RMII data TXD[1:0], TX_EN delay	t_{RMTDX}	2.0	—	10.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the RMII transmit AC timing diagram.

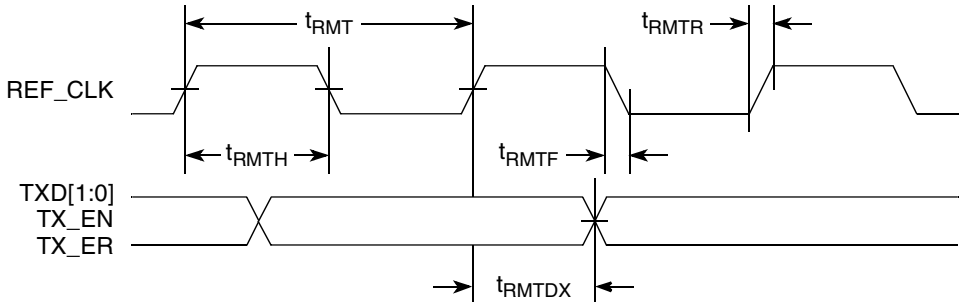


Figure 12. RMII Transmit AC Timing Diagram

8.2.3.2 RMII Receive AC Timing Specifications

This table shows the RMII receive AC timing specifications.

Table 30. RMII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typical	Max	Unit
Input low voltage at 3.3 LV_{DD}	V_{IL}	—	—	0.8	V
Input high voltage at 3.3 LV_{DD}	V_{IH}	2.0	—	—	V
REF_CLK clock period	t_{RMR}	15.0	20.0	25.0	ns
REF_CLK duty cycle	t_{RMRH}	35	50	65	%
REF_CLK peak-to-peak jitter	t_{RMRJ}	—	—	250	ps
Rise time REF_CLK (20%–80%)	t_{RMRR}	1.0	—	2.0	ns
Fall time REF_CLK (80%–20%)	t_{RMRF}	1.0	—	2.0	ns
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK rising edge	t_{RMRDV}	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK rising edge	t_{RMRDX}	2.0	—	—	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure provides the AC test load for eTSEC.

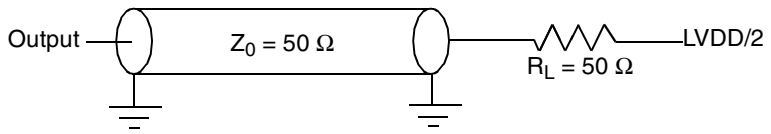


Figure 13. eTSEC AC Test Load

This figure shows the RMII receive AC timing diagram.

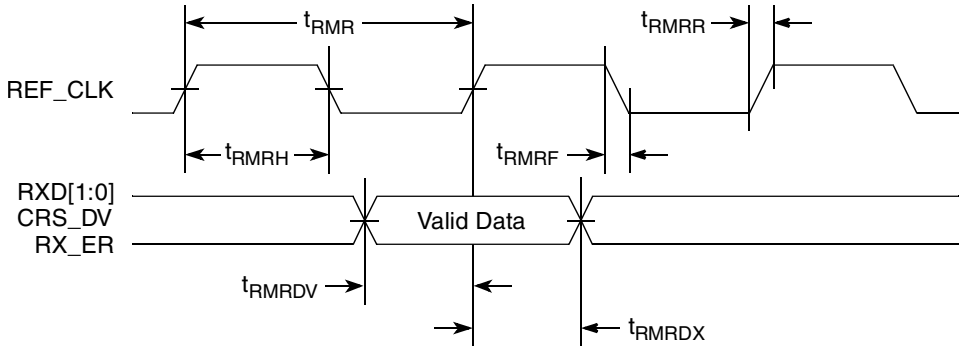


Figure 14. RMII Receive AC Timing Diagram

8.3 Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock).

This figure provides the AC test load for eTSEC.

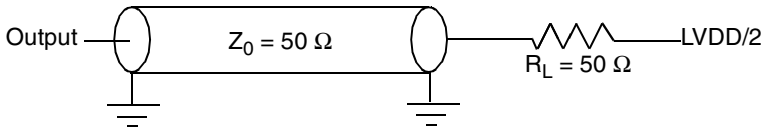


Figure 15. eTSEC AC Test Load

8.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 2.5 V or 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 31 and Table 32.

Table 31. MII Management DC Electrical Characteristics When Powered at 2.5 V

Parameter	Conditions		Symbol	Min	Max	Unit
Supply voltage (2.5 V)	—		LV_{DD1}	2.37	2.63	V
Output high voltage	I_{OH} = –1.0 mA	LV_{DD1} = Min	V_{OH}	2.00	LV_{DD1} + 0.3	V
Output low voltage	I_{OL} = 1.0 mA	LV_{DD1} = Min	V_{OL}	GND – 0.3	0.40	V
Input high voltage	—	LV_{DD1} = Min	V_{IH}	1.7	—	V
Input low voltage	—	LV_{DD1} = Min	V_{IL}	–0.3	0.70	V
Input high current	V_{IN} = LV_{DD1}		I_{IH}	—	20	μA
Input low current	V_{IN} = LV_{DD1}		I_{IL}	–15	—	μA

This figures show the local bus signals.

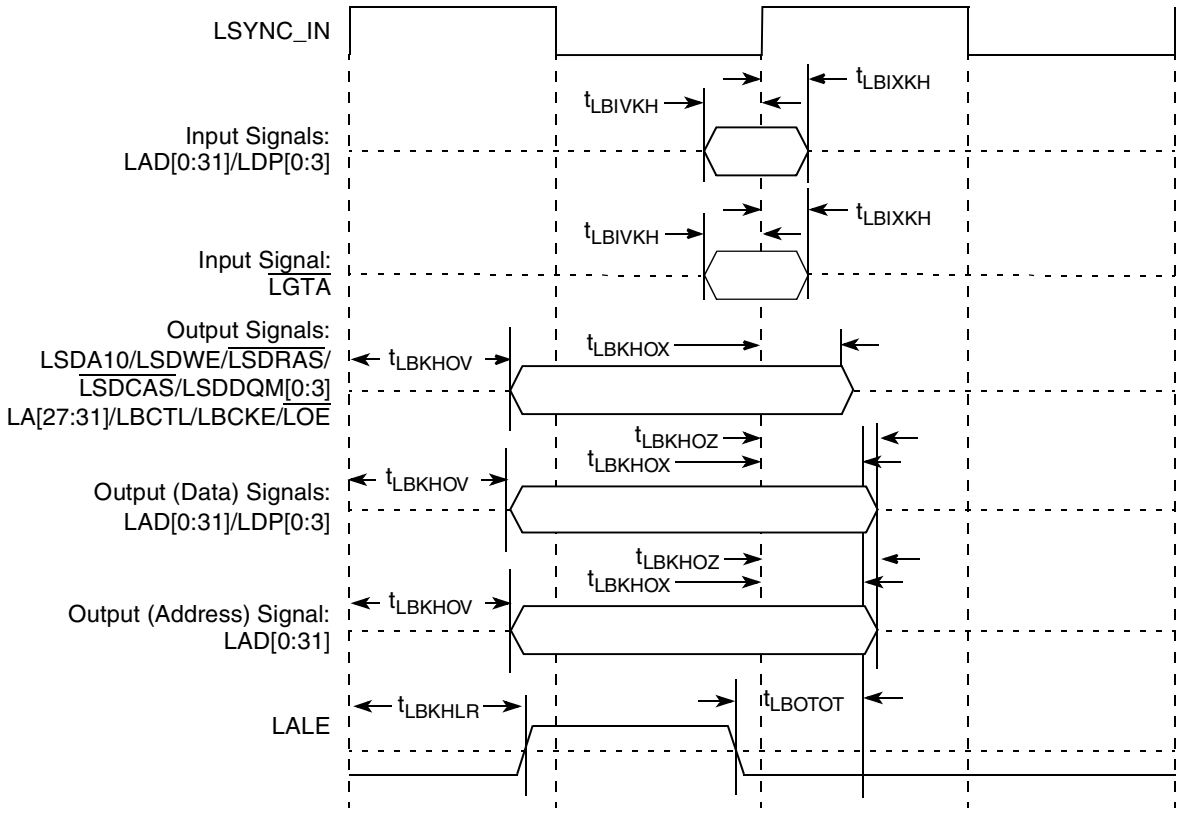


Figure 20. Local Bus Signals, Non-special Signals Only (PLL Enable Mode)

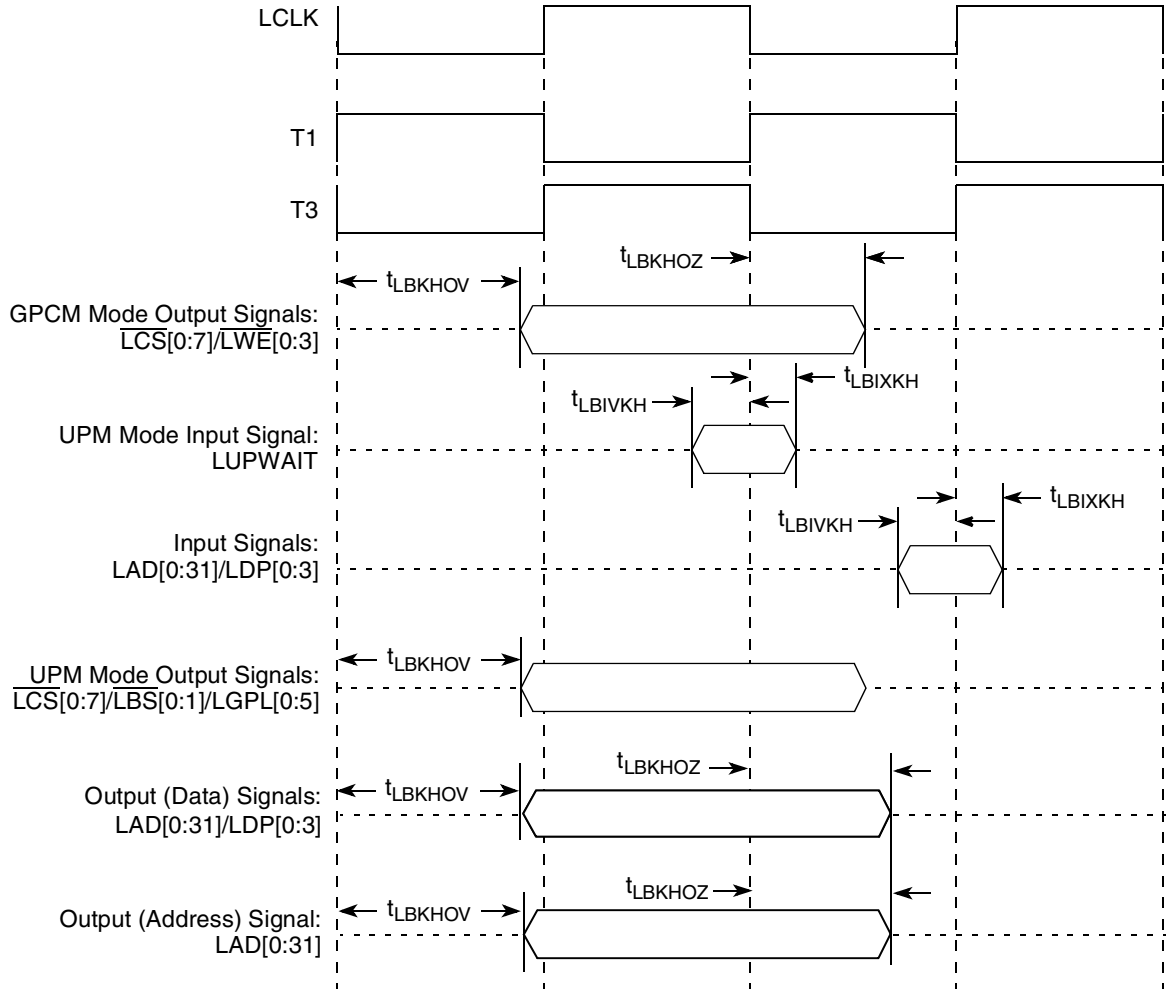


Figure 23. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (PLL Bypass Mode)

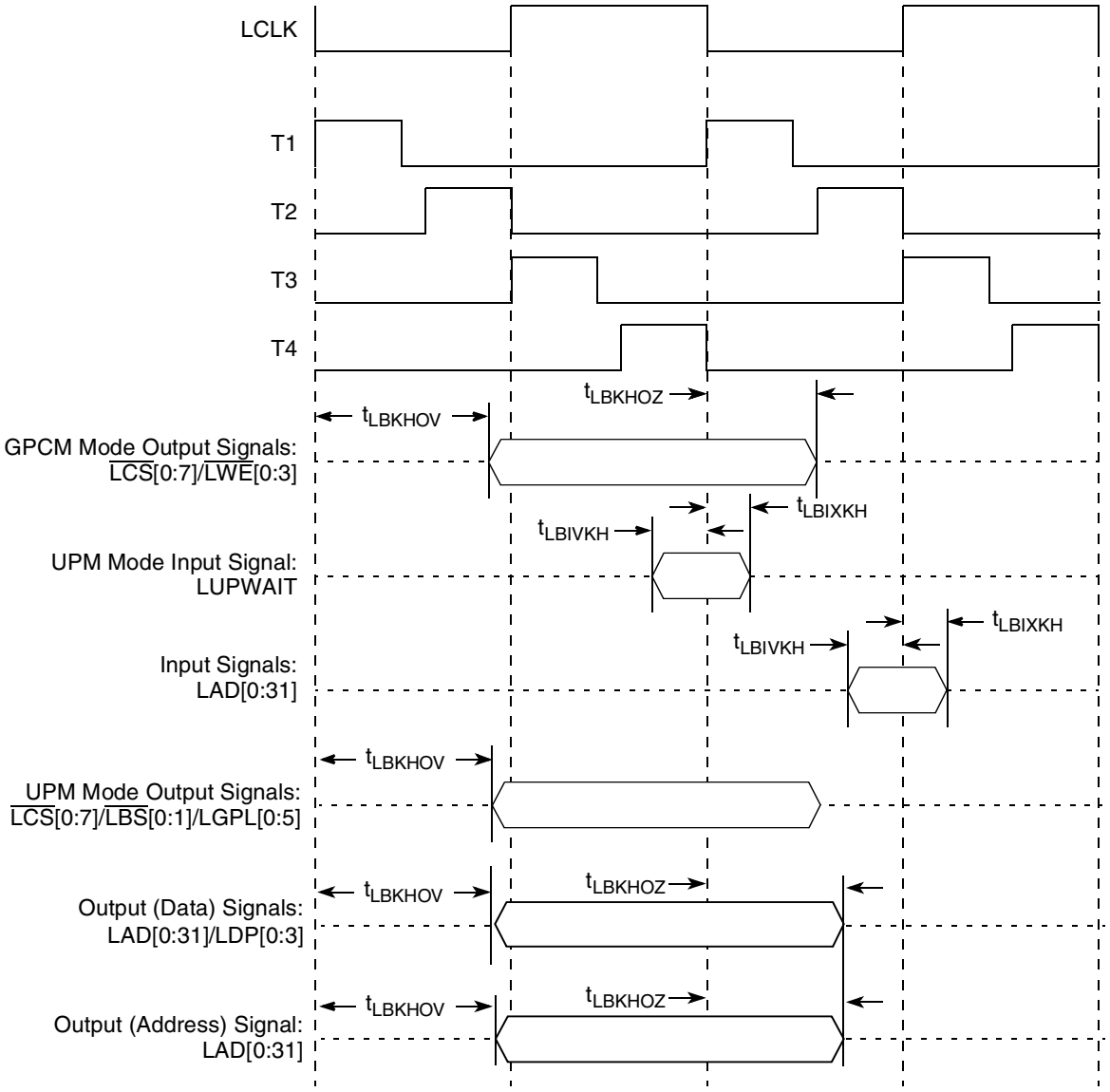


Figure 25. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 (PLL Bypass Mode)

11 Enhanced Secure Digital Host Controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC (SD/MMC) interface of the chip.

The eSDHC controller always uses the falling edge of the SD_CLK in order to drive the SD_DAT[0:3]/CMD as outputs and sample the SD_DAT[0:3] as inputs. This behavior is true for both full- and high-speed modes.

Note that this is a non-standard implementation, as the SD card specification assumes that in high-speed mode, data is driven at the rising edge of the clock.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI.

NOTE

It is recommended that the recovered Tx UI be calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (that is, least squares and median deviation fits).

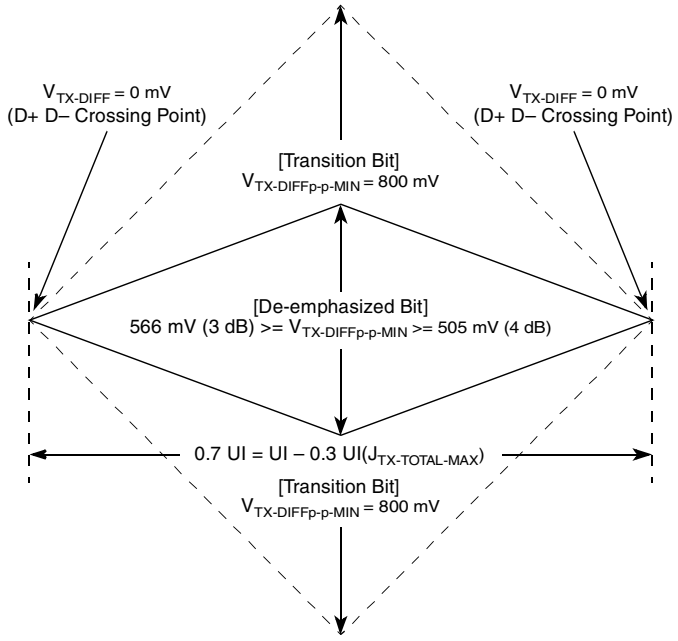


Figure 42. Minimum Transmitter Timing and Voltage Output Compliance Specifications

15.4.3 Differential Receiver (Rx) Input Specifications

This table defines the specifications for the differential input at all receivers. The parameters are specified at the component pins.

Table 53. Differential Receiver (Rx) Input Specifications

Parameter	Comments	Symbol	Min	Typical	Max	Units	Note
Unit interval	Each U_{PERX} is 400 ps ± 300 ppm. U_{PERX} does not account for Spread Spectrum Clock dictated variations.	UI	399.88	400	400.12	ps	1
Differential peak-to-peak output voltage	$V_{PEDPPRX} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$	$V_{RX-DIFFp-p}$	0.175	—	1.200	V	2

17 Timers

This section describes the DC and AC electrical specifications for the timers of the chip.

17.1 Timers DC Electrical Characteristics

This table provides the DC electrical characteristics for the device timers pins, including TIN, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$, and RTC_CLK.

Table 63. Timers DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Output high voltage	I_{OH} = –6.0 mA	V_{OH}	2.4	—	V
Output low voltage	I_{OL} = 6.0 mA	V_{OL}	—	0.5	V
Output low voltage	I_{OL} = 3.2 mA	V_{OL}	—	0.4	V
Input high voltage	—	V_{IH}	2.0	OV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.8	V
Input current	0 V ≤ V_{IN} ≤ OV_{DD}	I_{IN}	—	± 30	μA

17.2 Timers AC Timing Specifications

This table provides the timers input and output AC timing specifications.

Table 64. Timers Input AC Timing Specifications[1]

Parameter	Symbol [2]	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs should be synchronized before use by any external synchronous logic. Timers inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation

This figure provides the AC test load for the timers.

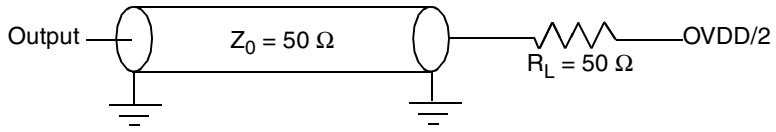


Figure 46. Timers AC Test Load

18 GPIO

This section describes the DC and AC electrical specifications for the GPIO of the chip.

18.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for the device GPIO.

Table 65. GPIO DC Electrical Characteristics

This specification applies when operating at 3.3 V ± 165 mV supply.

Parameter	Condition	Symbol	Min	Max	Unit
Output high voltage	I_{OH} = –6.0 mA	V_{OH}	2.4	—	V
Output low voltage	I_{OL} = 6.0 mA	V_{OL}	—	0.5	V
Output low voltage	I_{OL} = 3.2 mA	V_{OL}	—	0.4	V
Input high voltage	—	V_{IH}	2.0	OV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.8	V
Input current	0 V ≤ V_{IN} ≤ OV_{DD}	I_{IN}	—	± 30	μA

18.2 GPIO AC Timing Specifications

This table provides the GPIO input and output AC timing specifications.

Table 66. GPIO Input AC Timing Specifications

Parameter	Symbol	Min	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

This figure provides the AC test load for the GPIO.

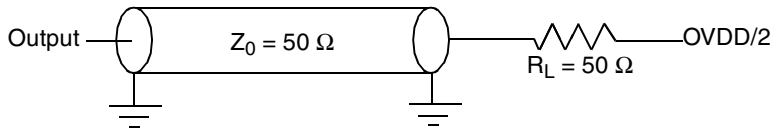
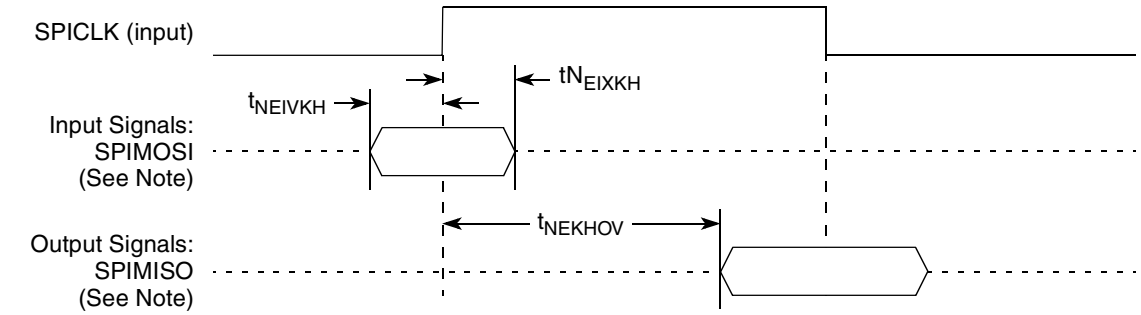


Figure 47. GPIO AC Test Load

19 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins of the chip.

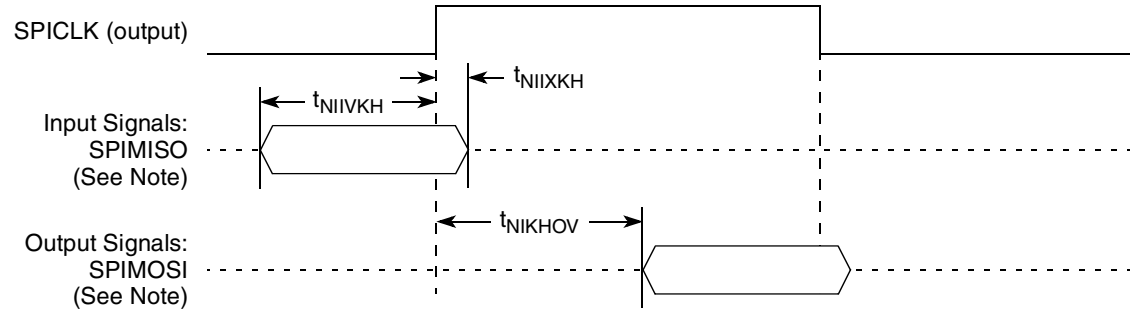
This figure shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 49. SPI AC Timing in Slave Mode (External Clock) Diagram

This figure shows the SPI timing in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 50. SPI AC Timing in Master Mode (Internal Clock) Diagram

21 High-Speed Serial Interfaces (HSSI)

This chip features two serializer/deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications. See Table 1 for the interfaces supported.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

21.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 51 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (SD*n*_TX and $\overline{\text{SD}n\text{\_TX}}$) or a receiver input (SD*n*_RX and $\overline{\text{SD}n\text{\_RX}}$). Each signal swings between A volts and B volts where A > B.

NOTE

Figure 56 to Figure 59 below are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance, and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by the clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the device SerDes reference clock receiver requirement provided in this document.

This figure shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with device SerDes reference clock input's DC requirement.

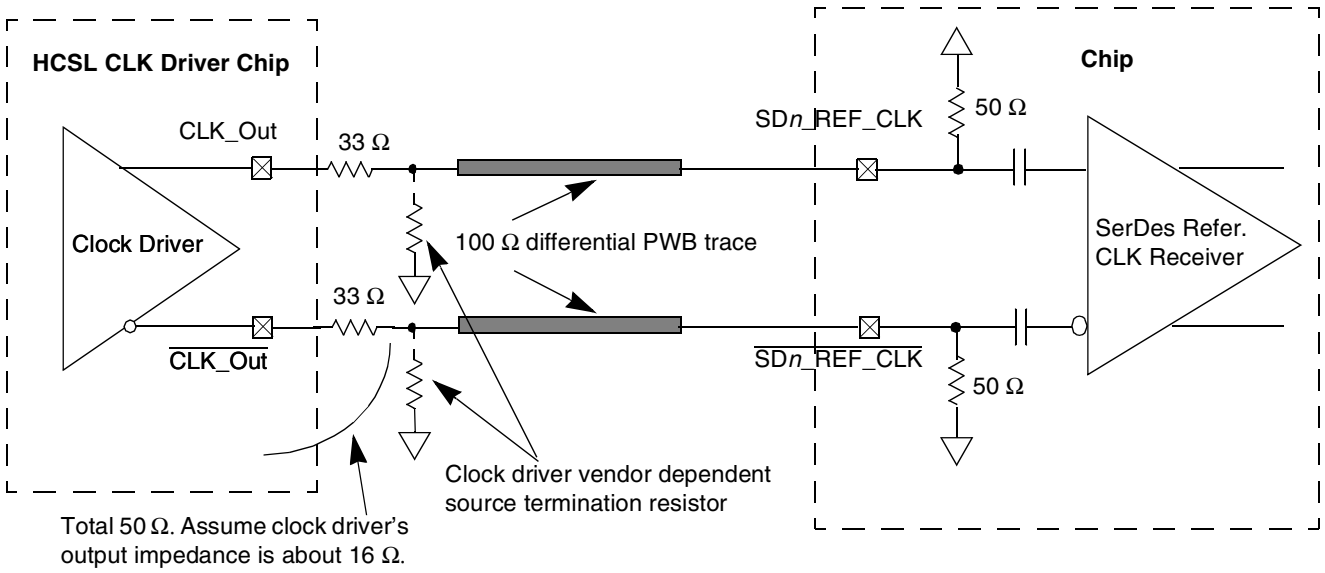


Figure 56. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)

This figure shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Since LVDS clock driver's common-mode voltage is higher than the device SerDes reference clock input's allowed range (100 to 400 mV), AC-coupled connection scheme must be used. It assumes the LVDS

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
MDQ35	AE1	I/O	GVDD	11
MDQ36	V6	I/O	GVDD	11
MDQ37	Y5	I/O	GVDD	11
MDQ38	AA4	I/O	GVDD	11
MDQ39	AB6	I/O	GVDD	11
MDQ40	AD3	I/O	GVDD	11
MDQ41	AC4	I/O	GVDD	11
MDQ42	AD4	I/O	GVDD	11
MDQ43	AF1	I/O	GVDD	11
MDQ44	AE4	I/O	GVDD	11
MDQ45	AC5	I/O	GVDD	11
MDQ46	AE2	I/O	GVDD	11
MDQ47	AE3	I/O	GVDD	11
MDQ48	AG1	I/O	GVDD	11
MDQ49	AG2	I/O	GVDD	11
MDQ50	AG3	I/O	GVDD	11
MDQ51	AF5	I/O	GVDD	11
MDQ52	AE5	I/O	GVDD	11
MDQ53	AD7	I/O	GVDD	11
MDQ54	AH2	I/O	GVDD	11
MDQ55	AG4	I/O	GVDD	11
MDQ56	AH3	I/O	GVDD	11
MDQ57	AG5	I/O	GVDD	11
MDQ58	AF8	I/O	GVDD	11
MDQ59	AJ5	I/O	GVDD	11
MDQ60	AF6	I/O	GVDD	11
MDQ61	AF7	I/O	GVDD	11
MDQ62	AH6	I/O	GVDD	11
MDQ63	AH7	I/O	GVDD	11
MDQS0	C8	I/O	GVDD	11
MDQS1	C4	I/O	GVDD	11
MDQS2	E3	I/O	GVDD	11
MDQS3	G2	I/O	GVDD	11

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
GND (VSS)	A1, AJ1, H2, N2, AA2, AD2, D3, R3, AF3, A4, F4, J4, L4, V4, Y4, AB4, B5, E5, P5, AH5, K6, T6, AA6, AD6, AG6, F7, J7, Y7, AJ7, B8, AE8, AG8, G9, AC9,B11, D11, F11, L11, M11, N11, P11, T11, U11, V11, W11,L12, M12, N12, P12, R12, T12, U12, V12, W12, E12, E13, L13, M13, N13, P13, R13, T13, U13, V13, W13, AE13, AJ13, F14, L14, M14, N14, P14, R14, T14, U14, V14, W14, M15, N15, P15, R15, T15, U15, V15, L16, M16, N16, P16, R16, T16, U16, V16, W16, L17, M17, N17, P17, R17, T17, U17, V17, W17, L18, M18, N18, P18, R18, T18, U18, V18, W18, L19, M19, N19, P19, T19, U19, V19, W19, AC20, G21, AF21, C22, J23, AA23, AJ23, B24, W24, AF24, K25, R25, AD25, D26, G27, M27, T27, Y27, AB27, AG27, A29, AJ29	—	—	—
AVDD_C	AD13	Power for e300 core PLL (1.0 V or 1.05 V)	—	15
AVDD_L	F13	Power for eLBC PLL (1.0 V or 1.05 V)	—	15
AVDD_P	F12	Power for system PLL (1.0 V or 1.05 V)	—	15
GVDD	A2, D2, R2, U2, AC2, AF2, AJ2, F3, H3, L3, N3, Y3, AB3, B4, P4, AF4, AH4, C5, F5, K5, V5, AA5, AD5, N6, R6, AJ6, B7, E7, K7, AA7, AE7, AG7, AD8	Power for DDR SDRAM I/O Voltage (2.5 or 1.8 V)	GVDD	—
OVDD	AC10, AF12, AJ12, K23, Y23, R24, AD24, L25, W25, AB26, U27, M28, Y28, G10, A11, C11	PCI, USB, and other Standard (3.3 V)	OVDD	—
No Connect				
NC	F16, F17, AD16, AD17	—	—	8
Pull Down				

Table 73. Configurable Clock Units (continued)

Unit	Default Frequency	Options
PCI Express1, 2	csb_clk/3	Off, c*sb_clk, csb_clk/2, csb_clk/3*
SATA1, 2	csb_clk/3	Off, *csb_clk*

1 This only applies to I^2C1 (I^2C2 clock is not configurable).

This table provides the operating frequencies for the TePBGA II package under recommended operating conditions (see Table 3).

Table 74. Operating Frequencies for TePBGA II

Parameter[1]	Minimum Operating Frequency (MHz)	Maximum Operating Frequency (MHz)
e300 core frequency (*core_clk*)	333	800
Coherent system bus frequency (*csb_clk*)	133	400
DDR2 memory bus frequency (MCK)[1]	250	400
DDR1 memory bus frequency (MCK) [2]	167	333
Local bus frequency (LCLK*n*)[1]	—	133
Local bus controller frequency (*lbc_clk*)	—	400
PCI input frequency (CLKIN or PCI_CLK)	25	66
eTSEC frequency	133	400
Security encryption controller frequency	—	200
USB controller frequency	—	200
eSDHC controller frequency	—	200
PCI Express controller frequency	—	400
SATA controller frequency	—	200

Notes:
1. The CLKIN frequency, RCWLR[SPMF], and RCWLR[COREPLL] settings must be chosen such that the resulting *csb_clk*, MCK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies. The value of SCCR[xCM] must be programmed such that the maximum internal operating frequency of the Security core, USB modules, SATA, and eSDHC will not exceed their respective value listed in this table.
2. The DDR data rate is 2× the DDR memory bus frequency.
3. The local bus frequency is ½, ¼, or 1/8 of the *lbiu_clk* frequency (depending on LCRR[CLKDIV]) which is in turn 1× or 2× the *csb_clk* frequency (depending on RCWLR[LBCM]).

23.1 System PLL Configuration

The system PLL is controlled by the RCWLR[SPMF] parameter. The system PLL VCO frequency depends on RCWLR[DDRCM] and RCWLR[LBCM]. Table 75 shows the multiplication factor encodings for the system PLL.

NOTE

If RCWLR[DDRCM] and RCWLR[LBCM] are both cleared, the system PLL VCO frequency = (CSB frequency) × (System PLL VCO Divider).

If either RCWLR[DDRCM] or RCWLR[LBCM] are set, the system PLL VCO frequency = 2 × (CSB frequency) × (System PLL VCO Divider).

The VCO divider needs to be set properly so that the System PLL VCO frequency is in the range of 400–800 MHz.

Table 75. System PLL Multiplication Factors

RCWLR[SPMF]	System PLL Multiplication Factor
0000	Reserved
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110	× 6
0111–1111	× 7 to × 15

As described in Section 23, “Clocking,” The LBIUCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (CLKIN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). Table 77 and Table 78 show the expected frequency values for the CSB frequency for select *csb_clk* to CLKIN/PCI_SYNC_IN ratios.

The RCWLR[SVCOD] denotes the system PLL VCO internal frequency as shown in Table 76.

Table 76. System PLL VCO Divider

RCWLR[SVCOD]	VCO Division Factor
00	4
01	8
10	2
11	1

Table 79. e300 Core PLL Configuration (continued)

RCWLR[COREPLL]			*core_clk* : *csb_clk* Ratio	VCO Divider [1]
0–1	2–5	6		
01	**0001**	1	1.5:1	4
10	**0001**	1	1.5:1	8
00	**0010**	0	2:1	2
01	**0010**	0	2:1	4
10	**0010**	0	2:1	8
00	**0010**	1	2.5:1	2
01	**0010**	1	2.5:1	4
10	**0010**	1	2.5:1	8
00	**0011**	0	3:1	2
01	**0011**	0	3:1	4
10	**0011**	0	3:1	8
00	**0011**	1	3.5:1	2
01	**0011**	1	3.5:1	4
10	**0011**	1	3.5:1	8
00	**0100**	0	4:1	2
01	**0100**	0	4:1	4
10	**0100**	0	4:1	8

Notes:
1. Core VCO frequency = Core frequency × VCO divider. Note that VCO divider has to be set properly so that the core VCO frequency is in the range of 800–1600 MHz.

23.3 Suggested PLL Configurations

This table shows suggested PLL configurations for different input clocks (LBCM = 0).

Table 80. Example Clock Frequency Combinations

								eLBC [1]			e300 Core [1]				
Ref [1]	**LBCM**	**DDRCM**	**SVCOD**	**SPMF**	**Sys VCO[1,2]**	**CSB[1,3]**	**DDR data rate[1,4]**	**/2**	**/4**	**/8**	**× 1**	**× 1.5**	**× 2**	**× 2.5**	**× 3**
25.0	0	1	2	5	500	125	250	62.5	31.3	15.6	—	—	—	—	375
25.0	0	1	2	6	600	150	300	75 [6]	37.5	18.8	—	—	—	375	450
33.3	0	1	2	5	667	167	333	83.3 [6]	41.6	20.8	—	—	333	416	500
33.3	0	1	2	4	533	133	267	66.7	33.3	16.7	—	—	—	333	400

This table shows the heat sink thermal resistance for TePBGA II package with heat sinks, simulated in a standard JEDEC environment, per JESD 51-6.

Table 82. Thermal Resistance with Heat Sink in Open Flow (TePBGA II)

Heat Sink Assuming Thermal Grease	Air Flow	Thermal Resistance (°/W)
AAVID 30 × 30 × 9.4 mm Pin Fin	Natural Convection	13.1
	0.5 m/s	10.6
	1 m/s	9.3
	2 m/s	8.2
	4 m/s	7.5
AAVID 31 × 35 × 23 mm Pin Fin	Natural Convection	11.1
	0.5 m/s	8.5
	1 m/s	7.7
	2 m/s	7.2
	4 m/s	6.8
AAVID 43× 41× 16.5mm Pin Fin	Natural Convection	11.3
	0.5 m/s	9.0
	1 m/s	7.8
	2 m/s	7.0
	4 m/s	6.5
Wakefield, 53 × 53 × 25 mm Pin Fin	Natural Convection	9.7
	0.5 m/s	7.7
	1 m/s	6.8
	2 m/s	6.4
	4 m/s	6.1

Heat sink vendors include the following:

Aavid Thermalloy
www.aavidthermalloy.com

Alpha Novatech
www.alphanovatech.com

International Electronic Research Corporation (IERC)
www.ctscorp.com

Millennium Electronics (MEI)
www.mei-thermal.com

26.1 Part Numbers Fully Addressed by This Document

Table 84 provides the Freescale part numbering nomenclature for this chip. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

Table 84. Part Numbering Nomenclature

MPC	*8377*	*E*	*C*	*ZQ*	*AF*	*D*	*A*
Product Code	**Part Identifier**	**Encryption Acceleration**	**Temperature Range [1]**	**Package [2]**	**e300 core Frequency [3]**	**DDR Data Rate**	**Revision Level [4]**
MPC	8377	Blank = Not included E = included	Blank = 0°C (T_a) to 125°C (T_j) C = –40°C (T_a) to 125°C (T_j)	VR = Pb-free 689 TePBGA II	AN = 800 MHz AL = 667 MHz AJ = 533 MHz AG = 400 MHz	G = 400 MHz F = 333 MHz D = 266 MHz	Blank = Freescale ATMC fab A = GlobalFoundries fab

Note:

1 Contact local Freescale office on availability of parts with an extended temperature range.

2 See Section 22, "Package and Pin Listings," for more information on the available package type.

3 Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.

4 No design changes occurred between initial parts and the revision "*A*" parts. Only the fab source has changed in moving to revision "*A*" parts. Initial revision parts and revision "*A*" parts are form, fit, function, and reliability equivalent.

This table lists the available core and DDR data rate frequency combinations.

Table 85. Available Parts (Core/DDR Data Rate)

MPC8377E	MPC8378E	MPC8379E
800 MHz/400 MHz	800 MHz/400 MHz	800 MHz/400 MHz
667 MHz/400 MHz	667 MHz/400 MHz	667 MHz/400 MHz
533 MHz/333 MHz	533 MHz/333 MHz	533 MHz/333 MHz
400 MHz/266 MHz	400 MHz/266 MHz	400 MHz/266 MHz