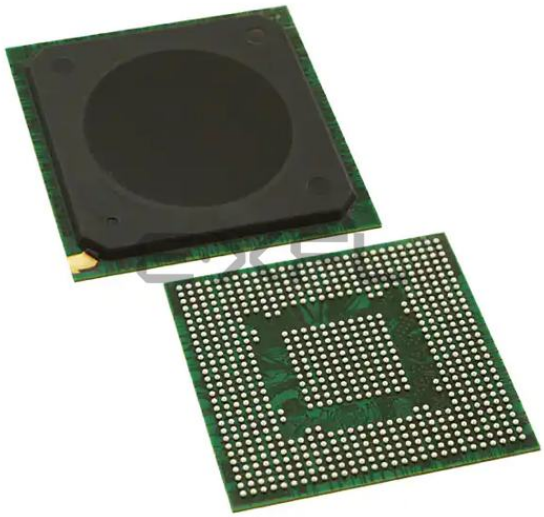

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c4s
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	667MHz
Co-Processors/DSP	Security; SEC 3.0
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 125°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	689-BBGA Exposed Pad
Supplier Device Package	689-TEPBGA II (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8377evralg

In addition to the security engine, new high-speed interfaces, such as PCI Express and SATA are included. This table compares the differences between MPC837xE derivatives and provides the number of ports available for each interface.

Table 1. High-Speed Interfaces on the MPC8377E, MPC8378E, and MPC8379E

Descriptions	MPC8377E	MPC8378E	MPC8379E
SGMII	0	2	0
PCI Express®	2	2	0
SATA	2	0	4

1.1 DDR Memory Controller

The DDR1/DDR2 memory controller includes the following features:

- Single 32- or 64-bit interface supporting both DDR1 and DDR2 SDRAM
- Support for up to 400-MHz data rate
- Support up to 4 chip selects
- 64-Mbit to 2-Gbit (for DDR1) and to 4-Gbit (for DDR2) devices with ×8/×16/×32 data ports (no direct ×4 support)
- Support for up to 32 simultaneous open pages
- Supports auto refresh
- On-the-fly power management using CKE
- 1.8-/2.5-V SSTL2 compatible I/O

1.2 USB Dual-Role Controller

The USB controller includes the following features:

- Supports USB on-the-go mode, including both device and host functionality, when using an external ULPI (UTMI + low-pin interface) PHY
- Complies with *USB Specification, Rev. 2.0*
- Supports operation as a stand-alone USB device
  - Supports one upstream facing port
  - Supports three programmable USB endpoints
- Supports operation as a stand-alone USB host controller
  - Supports USB root hub with one downstream-facing port
  - Enhanced host controller interface (EHCI) compatible
- Supports high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operation; low-speed operation is supported only in host mode
- Supports UTMI + low pin interface (ULPI)

1.10 PCI Express Controller

The PCI Express controller includes the following features:

- PCI Express 1.0a compatible
- Two ×1 links or one ×2 link width
- Auto-detection of number of connected lanes
- Selectable operation as root complex or endpoint
- Both 32- and 64-bit addressing
- 128-byte maximum payload size
- Support for MSI and INTx interrupt messages
- Virtual channel 0 only
- Selectable Traffic Class
- Full 64-bit decode with 32-bit wide windows
- Dedicated four channel descriptor-based DMA engine per interface

1.11 Serial ATA (SATA) Controllers

The serial ATA (SATA) controllers have the following features:

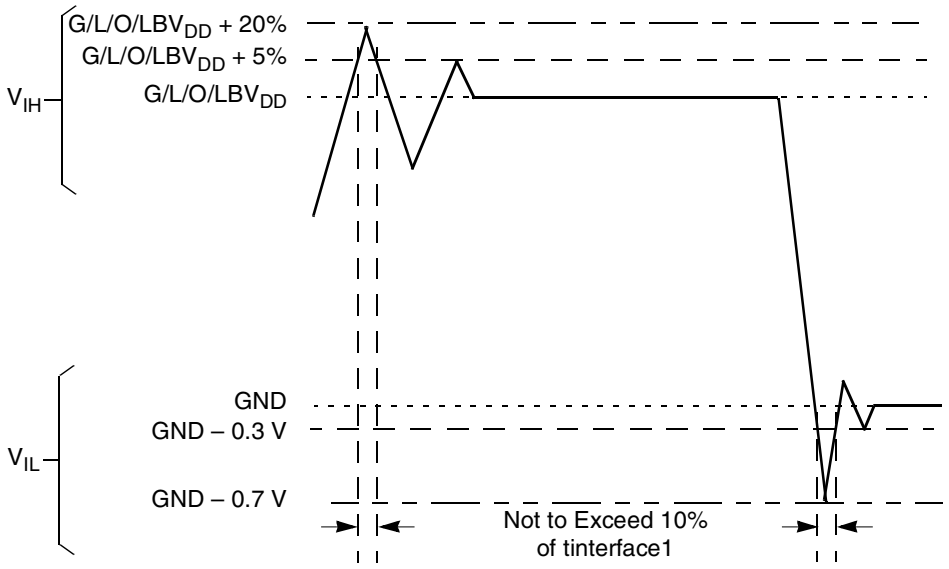
- Supports *Serial ATA Rev 2.5 Specification*
- Spread spectrum clocking on receive
- Asynchronous notification
- Hot Plug including asynchronous signal recovery
- Link power management
- Native command queuing
- Staggered spin-up and port multiplier support
- Port multiplier support
- SATA 1.5 and 3.0 Gb/s operation
- Interrupt driven
- Power management support
- Error handling and diagnostic features
  - — Far end/near end loopback
  - — Failed CRC error reporting
  - — Increased ALIGN insertion rates
- Scrambling and CONT override

Table 3. Recommended Operating Conditions (continued)

Characteristic		Symbol	Recommended Value	Unit	Note
SerDes	up to 667 MHz	L[1,2]_nV_{DD}	1.0 ± 50 mV	V	1, 3
	800 MHz		1.05 V ± 50 mV	V	1, 3
Operating temperature range	commerical	T_a T_j	T_a=0 (min)— T_j=125 (max)	°C	—
	extended temperature	T_a T_j	T_a=–40 (min)— T_j=125 (max)	°C	—

Notes:
1. GV_{DD}, OV_{DD}, AV_{DD}, and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.
2. AV_{DD} is the input to the filter discussed in Section 25.1, "PLL Power Supply Filtering," and is not necessarily the voltage at the AVDD pin.
3. L[1,2]_nV_{DD}, $SDAV_{DD\_0}$, $XCOREV_{DD}$, and $XPADV_{DD}$ power inputs.

This figure shows the undershoot and overshoot voltages at the interfaces of the device.



Note:
1. Note that $t_{interface}$ refers to the clock period associated with the bus clock interface.
2. Note that with the PCI overshoot allowed (as specified above), the device does not fully comply with the maximum AC ratings and device protection guideline outlined in the *PCI Rev. 2.3 Specification* (Section 4.2.2.3).

Figure 2. Overshoot/Undershoot Voltage for GV_{DD}/LV_{DD}/OV_{DD}/LBV_{DD}

Table 5. Power Dissipation [1] (continued)

Core Frequency (MHz)	CSB/DDR Frequency (MHz)	Sleep Power at T_j = 65°C (W) [2]	Typical Application at T_j = 65°C (W) [2]	Typical Application at T_j = 125°C (W) [3]	Max Application at T_j = 125°C (W) [4]
600	400	1.45	2.1	3.4	4.1
	300	1.45	2.0	3.3	4.0
667	333	1.45	2.1	3.3	4.1
	266	1.45	2.0	3.3	3.9
800	400	1.45	2.5	3.8	4.3

Notes:
1. The values do not include I/O supply power (OV_{DD}, LV_{DD}, GV_{DD}) or AV_{DD}. For I/O power values, see Table 6.
2. Typical power is based on a voltage of V_{DD} = 1.0 V for core frequencies ≤ 667 MHz or V_{DD} = 1.05 V for core frequencies of 800 MHz, and running a Dhrystone benchmark application.
3. Typical power is based on a voltage of V_{DD} = 1.0 V for core frequencies ≤ 667 MHz or V_{DD} = 1.05 V for core frequencies of 800 MHz, and running a Dhrystone benchmark application.
4. Maximum power is based on a voltage of V_{DD} = 1.0 V for core frequencies ≤ 667 MHz or V_{DD} = 1.05 V for core frequencies of 800 MHz, worst case process, and running an artificial smoke test.

This table shows the estimated typical I/O power dissipation for the device.

Table 6. Typical I/O Power Dissipation

Interface	Parameter	GV_{DD} (1.8 V)	GV_{DD}/LBV_{DD} (2.5 V)	OV_{DD} (3.3 V)	LV_{DD} (3.3 V)	LV_{DD} (2.5 V)	L[1,2]_$n$$V_{DD}$ (1.0 V)	Unit	Comments
DDR I/O 65% utilization 2 pair of clocks	200 MHz data rate, 32-bit	0.28	0.35	—	—	—	—	W	—
	200 MHz data rate, 64-bit	0.41	0.49	—	—	—	—	W	
	266 MHz data rate, 32-bit	0.31	0.4	—	—	—	—	W	
	266 MHz data rate, 64-bit	0.46	0.56	—	—	—	—	W	
	300 MHz data rate, 32-bit	0.33	0.43	—	—	—	—	W	
	300 MHz data rate, 64-bit	0.48	0.6	—	—	—	—	W	
	333 MHz data rate, 32-bit	0.35	0.45	—	—	—	—	W	
	333 MHz data rate, 64-bit	0.51	0.64	—	—	—	—	W	
	400 MHz data rate, 32-bit	0.38	—	—	—	—	—	W	
	400 MHz data rate, 64-bit	0.56	—	—	—	—	—	W	

4.1 DC Electrical Characteristics

This table provides the clock input (CLKIN/PCI_CLK) DC timing specifications for the device.

Table 7. CLKIN DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit	Note
Input high voltage	—	V_{IH}	2.7	OV_{DD} + 0.3	V	1
Input low voltage	—	V_{IL}	–0.3	0.4	V	1
CLKIN Input current	0 V ≤ V_{IN} ≤ OV_{DD}	I_{IN}	—	± 10	μA	—
PCI_CLK Input current	0 V ≤ V_{IN} ≤ 0.5 V or OV_{DD} – 0.5 V ≤ V_{IN} ≤ OV_{DD}	I_{IN}	—	± 30	μA	—

Note:
1. In PCI agent mode, this specification does not comply with *PCI 2.3 Specification*.

4.2 AC Electrical Characteristics

The primary clock source for the device can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. This table provides the clock input (CLKIN/PCI_CLK) AC timing specifications for the device.

Table 8. CLKIN AC Timing Specifications

Parameter	Symbol	Min	Typical	Max	Unit	Note
CLKIN/PCI_CLK frequency	f_{CLKIN}	25	—	66.666	MHz	1, 6
CLKIN/PCI_CLK cycle time	t_{CLKIN}	15	—	40	ns	—
CLKIN/PCI_CLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	2.3	ns	2
CLKIN/PCI_CLK duty cycle	t_{KHK}/t_{CLKIN}	40	—	60	%	3
CLKIN/PCI_CLK jitter	—	—	—	± 150	ps	4, 5

Notes:
1. **Caution:** The system, core and security block must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for CLKIN/PCI_CLK are measured at 0.4 V and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter-short term and long term-and is guaranteed by design.
5. The CLKIN/PCI_CLK driver's closed loop jitter bandwidth should be < 500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track CLKIN drivers with the specified jitter.
6. Spread spectrum is allowed up to 1% down-spread on CLKIN/PCI_CLK up to 60 KHz.

6.2 DDR1 and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface.

6.2.1 DDR1 and DDR2 SDRAM Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR2 SDRAM when GVDD(typ) = 1.8 V.

Table 18. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	MV_{REF} – 0.25	V
AC input high voltage	V_{IH}	MV_{REF} + 0.25	—	V

This table provides the input AC timing specifications for the DDR1 SDRAM when GV_{DD}(typ) = 2.5 V.

Table 19. DDR1 SDRAM Input AC Timing Specifications for 2.5-V Interface

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	MV_{REF} – 0.31	V
AC input high voltage	V_{IH}	MV_{REF} + 0.31	—	V

This table provides the input AC timing specifications for the DDR1 and DDR2 SDRAM interface.

Table 20. DDR1 and DDR2 SDRAM Input AC Timing Specifications

Parameter	Symbol	Min	Max	Unit	Note
Controller skew for MDQS-MDQ/MECC/MDM	t_{CISKEW}			ps	1, 2
400 MHz data rate		–500	500		3
333 MHz data rate		–750	750		—
266 MHz data rate		–750	750		—

Note:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS*n* and any corresponding bit that will be captured with MDQS*n*. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: $t_{DISKEW} = \pm[T/4 - |t_{CISKEW}|]$ where T is the MCK clock period and $|t_{CISKEW}|$ is the absolute value of t_{CISKEW}.
3. This specification applies only to DDR2 interface.

6.2.2 DDR1 and DDR2 SDRAM Output AC Timing Specifications

This table shows the DDR1 and DDR2 SDRAM output AC timing specifications.

Table 21. DDR1 and DDR2 SDRAM Output AC Timing Specifications

Parameter	Symbol[1]	Min	Max	Unit	Note
MCK*n* cycle time, MCK*n*/$\overline{\text{MCK}n}$ crossing	t_{MCK}	5	10	ns	2
ADDR/CMD output setup with respect to MCK 400 MHz data rate 333 MHz data rate 266 MHz data rate 200 MHz data rate	t_{DDKHAS}	 1.95 2.40 3.15 4.20	 — — — —	ns	3, 7
ADDR/CMD output hold with respect to MCK 400 MHz data rate 333 MHz data rate 266 MHz data rate 200 MHz data rate	t_{DDKHAX}	 1.95 2.40 3.15 4.20	 — — — —	ns	3, 7
$\overline{\text{MCS}n}$ output setup with respect to MCK 400 MHz data rate 333 MHz data rate 266 MHz data rate 200 MHz data rate	t_{DDKHCS}	 1.95 2.40 3.15 4.20	 — — — —	ns	3
$\overline{\text{MCS}n}$ output hold with respect to MCK 400 MHz data rate 333 MHz data rate 266 MHz data rate 200 MHz data rate	t_{DDKHCX}	 1.95 2.40 3.15 4.20	 — — — —	ns	3
MCK to MDQS skew	t_{DDKHMH}	–0.6	0.6	ns	4, 8
MDQ//MDM output setup with respect to MDQS 400 MHz data rate 333 MHz data rate 266 MHz data rate 200 MHz data rate	t_{DDKHDS}, t_{DDKLDS}	 550 800 1100 1200	 — — — —	ps	5, 8
MDQ//MDM output hold with respect to MDQS 400 MHz data rate 333 MHz data rate 266 MHz data rate 200 MHz data rate	t_{DDKHDX}, t_{DDKLDX}	 700 800 1100 1200	 — — — —	ps	5, 8
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6, 8

8.1.1 MII, RMII, RGMII, and RTBI DC Electrical Characteristics

MII and RMII drivers and receivers comply with the DC parametric attributes specified in Table 24 and Table 25. The RGMII and RTBI signals in Table 25 are based on a 2.5 V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 24. MII and RMII DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage 3.3 V	LV_{DD1} LV_{DD2}	3.13	3.47	V	1
Output high voltage (LV_{DD1}/LV_{DD2} = Min, I_{OH} = –4.0 mA)	V_{OH}	2.40	LV_{DD1}/LV_{DD2} + 0.3	V	—
Output low voltage (LV_{DD1}/LV_{DD2} = Min, I_{OL} = 4.0 mA)	V_{OL}	GND	0.50	V	—
Input high voltage	V_{IH}	2.0	LV_{DD1}/LV_{DD2} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	0.90	V	—
Input high current (V_{IN} = LV_{DD1}, V_{IN} = LV_{DD2})	I_{IH}	—	30	µA	1
Input low current (V_{IN} = GND)	I_{IL}	–600	—	µA	—

Notes:
1. LV_{DD1} supports eTSEC 1. LV_{DD2} supports eTSEC 2.

Table 25. RGMII and RTBI DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage 2.5 V	LV_{DD1} LV_{DD2}	2.37	2.63	V	1
Output high voltage (LV_{DD1}/LV_{DD2} = Min, IOH = –1.0 mA)	V_{OH}	2.00	LV_{DD1}/LV_{DD2} + 0.3	V	—
Output low voltage (LV_{DD1}/LV_{DD2} = Min, I_{OL} = 1.0 mA)	V_{OL}	GND – 0.3	0.40	V	—
Input high voltage	V_{IH}	1.7	LV_{DD1}/LV_{DD2} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	0.70	V	—
Input high current (V_{IN} = LV_{DD1}, V_{IN} = LV_{DD2})	I_{IH}	—	–20	µA	1
Input low current (V_{IN} = GND)	I_{IL}	–20	—	µA	—

Notes:
1. LV_{DD1} supports eTSEC 1. LV_{DD2} supports eTSEC 2.

8.2.3 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.3.1 RMII Transmit AC Timing Specifications

This table shows the RMII transmit AC timing specifications.

Table 29. RMII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter	Symbol[1]	Min	Typical	Max	Unit
REF_CLK clock period	t_{RMT}	15.0	20.0	25.0	ns
REF_CLK duty cycle	t_{RMTH}	35	50	65	%
REF_CLK peak-to-peak jitter	t_{RMTJ}	—	—	250	ps
Rise time REF_CLK (20%–80%)	t_{RMTR}	1.0	—	2.0	ns
Fall time REF_CLK (80%–20%)	t_{RMTF}	1.0	—	2.0	ns
REF_CLK to RMII data TXD[1:0], TX_EN delay	t_{RMTDX}	2.0	—	10.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the RMII transmit AC timing diagram.

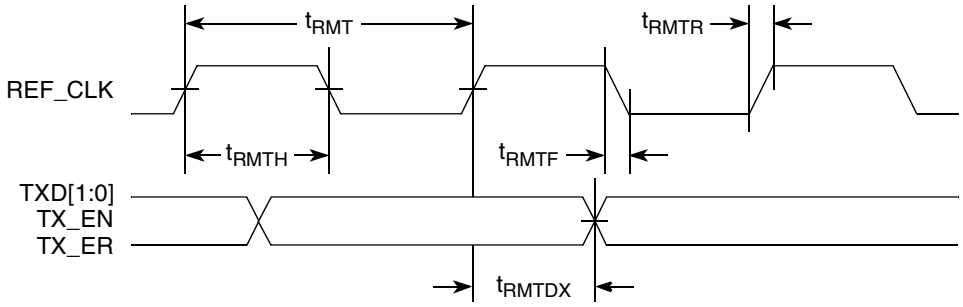


Figure 12. RMII Transmit AC Timing Diagram

compliance/test measurement load. The input receiver eye diagram is implementation specific and is not specified. Rx component designer should provide additional margin to adequately compensate for the degraded minimum receiver eye diagram (shown in Figure 43) expected at the input receiver based on an adequate combination of system simulations and the return loss measured looking into the Rx package and silicon. The Rx eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI.

NOTE

The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D– line (that is, as measured by a Vector Network Analyzer with 50 Ω probes—see Figure 44). Note that the series capacitors, $C_{PEACCTX}$, are optional for the return loss measurement.

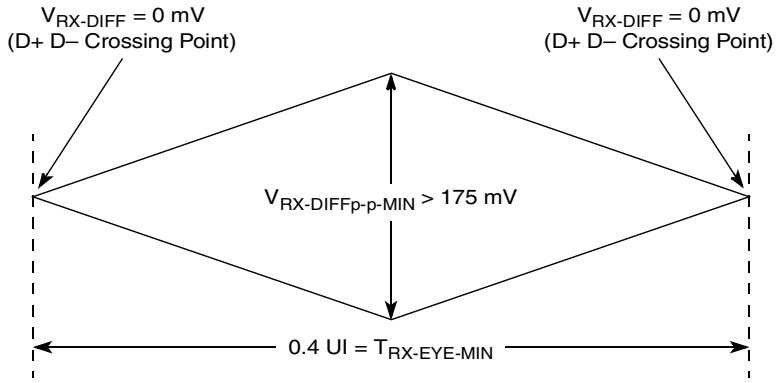


Figure 43. Minimum Receiver Eye Timing and Voltage Compliance Specification

17 Timers

This section describes the DC and AC electrical specifications for the timers of the chip.

17.1 Timers DC Electrical Characteristics

This table provides the DC electrical characteristics for the device timers pins, including TIN, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$, and RTC_CLK.

Table 63. Timers DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Output high voltage	I_{OH} = –6.0 mA	V_{OH}	2.4	—	V
Output low voltage	I_{OL} = 6.0 mA	V_{OL}	—	0.5	V
Output low voltage	I_{OL} = 3.2 mA	V_{OL}	—	0.4	V
Input high voltage	—	V_{IH}	2.0	OV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.8	V
Input current	0 V ≤ V_{IN} ≤ OV_{DD}	I_{IN}	—	± 30	μA

17.2 Timers AC Timing Specifications

This table provides the timers input and output AC timing specifications.

Table 64. Timers Input AC Timing Specifications[1]

Parameter	Symbol [2]	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs should be synchronized before use by any external synchronous logic. Timers inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation

This figure provides the AC test load for the timers.

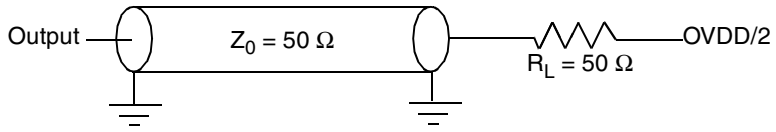


Figure 46. Timers AC Test Load

19.1 IPIC DC Electrical Characteristics

This table provides the DC electrical characteristics for the external interrupt pins of the chip.

Table 67. IPIC DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.0	OV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.8	V
Input current	—	I_{IN}	—	±30	μA
Output low voltage	I_{OL} = 6.0 mA	V_{OL}	—	0.5	V
Output low voltage	I_{OL} = 3.2 mA	V_{OL}	—	0.4	V

Note:
1. This table applies for pins $\overline{\text{IRQ}}$[0:7], $\overline{\text{IRQ\_OUT}}$, $\overline{\text{MCP\_OUT}}$.
2. $\overline{\text{IRQ\_OUT}}$ and $\overline{\text{MCP\_OUT}}$ are open drain pins, thus V_{OH} is not relevant for those pins.

19.2 IPIC AC Timing Specifications

This table provides the IPIC input and output AC timing specifications.

Table 68. IPIC Input AC Timing Specifications

Parameter	Symbol	Min	Unit
IPIC inputs—minimum pulse width	t_{PIWID}	20	ns

Note:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.

20 SPI

This section describes the DC and AC electrical specifications for the SPI of the chip.

20.1 SPI DC Electrical Characteristics

This table provides the DC electrical characteristics for the device SPI.

Table 69. SPI DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.0	OV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.8	V
Input current	—	I_{IN}	—	± 30	μA
Output high voltage	I_{OH} = –8.0 mA	V_{OH}	2.4	—	V

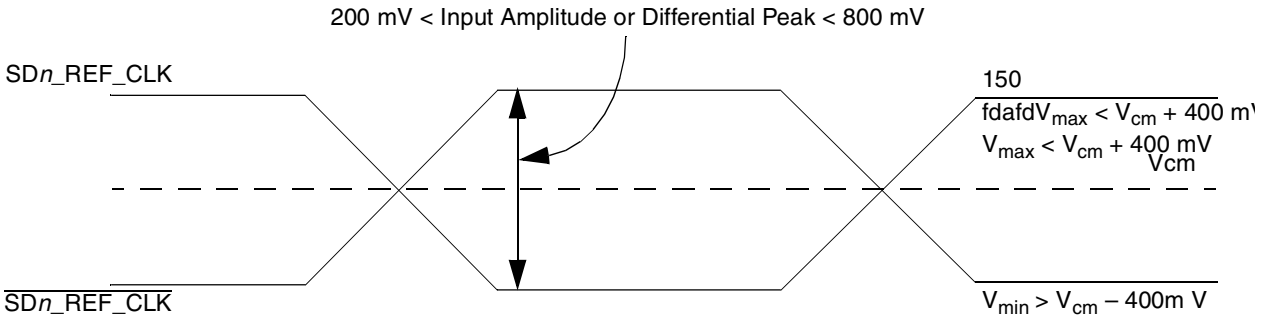


Figure 54. Differential Reference Clock Input DC Requirements (External AC-Coupled)

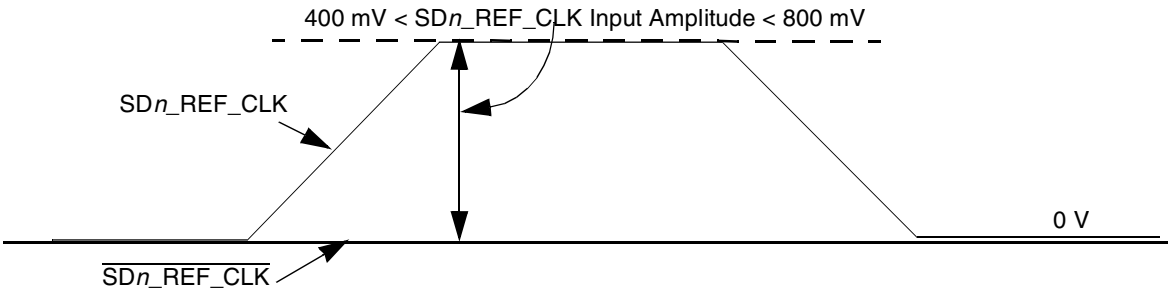


Figure 55. Single-Ended Reference Clock Input DC Requirements

21.2.3 Interfacing With Other Differential Signaling Levels

The following list provides information about interfacing with other differential signaling levels.

- With on-chip termination to SGND_SRDS*n* (xcorevss), the differential reference clocks inputs are HCSL (high-speed current steering logic) compatible DC-coupled.
- Many other low voltage differential type outputs like LVDS (low voltage differential signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 mV to 400 mV) for DC-coupled connection.
- LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
TSEC2_RXD0/GPIO1[16]	AE28	I/O	LVDD2	16
TSEC2_RXD1/GPIO1[15]	AE29	I/O	LVDD2	16
TSEC2_RXD2/GPIO1[14]	AH26	I/O	LVDD2	16
TSEC2_RXD3/GPIO1[13]	AH25	I/O	LVDD2	16
TSEC2_TX_CLK/GPIO2[24]/ TSEC1_TMR_GCLK	AG28	I/O	LVDD2	16
TSEC2_TX_EN/GPIO1[12]/ TSEC1_TMR_ALARM2	AJ26	I/O	LVDD2	16
TSEC2_TX_ER/GPIO1[24]/ TSEC1_TMR_ALARM1	AG26	I/O	LVDD2	16
TSEC2_TXD0/GPIO1[20]	AH28	I/O	LVDD2	16
TSEC2_TXD1/GPIO1[19]/ TSEC1_TMR_PP1	AF27	I/O	LVDD2	16
TSEC2_TXD2/GPIO1[18]/ TSEC1_TMR_PP2	AJ28	I/O	LVDD2	16
TSEC2_TXD3/GPIO1[17]/ TSEC1_TMR_PP3	AF29	I/O	LVDD2	16
GPIO1 Interface				
GPIO1[0]/GTM1_TIN1/ GTM2_TIN2/DREQ0_B	P25	I/O	OVDD	—
GPIO1[1]/GTM1_TGATE1_B/ GTM2_TGATE2_B/DACK0_B	N25	I/O	OVDD	—
GPIO1[2]/GTM1_TOUT1_B/ DDONE0_B	N26	I/O	OVDD	—
GPIO1[3]/GTM1_TIN2/ GTM2_TIN1/DREQ1_B	B9	I/O	OVDD	—
GPIO1[4]/GTM1_TGATE2_B/ GTM2_TGATE1_B/DACK1_B	N29	I/O	OVDD	—
GPIO1[5]/GTM1_TOUT2_B/ GTM2_TOUT1_B/DDONE1_B	M29	I/O	OVDD	—
GPIO1[6]/GTM1_TIN3/ GTM2_TIN4/DREQ2_B	A9	I/O	OVDD	—
GPIO1[7]/GTM1_TGATE3_B/ GTM2_TGATE4_B/DACK2_B	B10	I/O	OVDD	—
GPIO1[8]/GTM1_TOUT3_B/ DDONE2_B	J26	I/O	OVDD	—
GPIO1[9]/GTM1_TIN4/ GTM2_TIN3/DREQ3_B	J24	I/O	OVDD	—

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
GPIO1[10]/GTM1_TGATE4_B/ GTM2_TGATE3_B/DACK3_B	J27	I/O	OVDD	—
GPIO1[11]/GTM1_TOUT4_B/ GTM2_TOUT3_B/DDONE3_B	P24	I/O	OVDD	—
USB/GPIO2 Interface				
USBDR_CLK/GPIO2[23]	AJ11	I/O	OVDD	—
USBDR_DIR_DPPULLUP/ GPIO2[9]	AG12	I/O	OVDD	—
USBDR_NXT/GPIO2[8]	AJ10	I/O	OVDD	—
USBDR_PCTL0/GPIO2[11]/ SD_DAT2	AF10	I/O	OVDD	—
USBDR_PCTL1/GPIO2[22]/ SD_DAT3	AE9	I/O	OVDD	—
USBDR_PWRFAULT/ GPIO2[10]/SD_DAT1	AG13	I/O	OVDD	—
USBDR_STP_SUSPEND	AH12	O	OVDD	12
USBDR_D0_ENABLEN/ GPIO2[0]	AG10	I/O	OVDD	—
USBDR_D1_SER_TXD/ GPIO2[1]	AF13	I/O	OVDD	—
USBDR_D2_VMO_SE0/ GPIO2[2]	AG11	I/O	OVDD	—
USBDR_D3_SPEED/GPIO2[3]	AH11	I/O	OVDD	—
USBDR_D4_DP/GPIO2[4]	AG9	I/O	OVDD	—
USBDR_D5_DM/GPIO2[5]	AF9	I/O	OVDD	—
USBDR_D6_SER_RCV/ GPIO2[6]	AH13	I/O	OVDD	—
USBDR_D7_DRVVBUS/ GPIO2[7]	AH10	I/O	OVDD	—
I^2C Interface				
IIC1_SCL	C12	I/O	OVDD	2
IIC1_SDA	B12	I/O	OVDD	2
IIC2_SCL	A10	I/O	OVDD	2
IIC2_SDA	A12	I/O	OVDD	2
JTAG Interface				
TCK	B13	I	OVDD	—

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
GND (VSS)	A1, AJ1, H2, N2, AA2, AD2, D3, R3, AF3, A4, F4, J4, L4, V4, Y4, AB4, B5, E5, P5, AH5, K6, T6, AA6, AD6, AG6, F7, J7, Y7, AJ7, B8, AE8, AG8, G9, AC9,B11, D11, F11, L11, M11, N11, P11, T11, U11, V11, W11,L12, M12, N12, P12, R12, T12, U12, V12, W12, E12, E13, L13, M13, N13, P13, R13, T13, U13, V13, W13, AE13, AJ13, F14, L14, M14, N14, P14, R14, T14, U14, V14, W14, M15, N15, P15, R15, T15, U15, V15, L16, M16, N16, P16, R16, T16, U16, V16, W16, L17, M17, N17, P17, R17, T17, U17, V17, W17, L18, M18, N18, P18, R18, T18, U18, V18, W18, L19, M19, N19, P19, T19, U19, V19, W19, AC20, G21, AF21, C22, J23, AA23, AJ23, B24, W24, AF24, K25, R25, AD25, D26, G27, M27, T27, Y27, AB27, AG27, A29, AJ29	—	—	—
AVDD_C	AD13	Power for e300 core PLL (1.0 V or 1.05 V)	—	15
AVDD_L	F13	Power for eLBC PLL (1.0 V or 1.05 V)	—	15
AVDD_P	F12	Power for system PLL (1.0 V or 1.05 V)	—	15
GVDD	A2, D2, R2, U2, AC2, AF2, AJ2, F3, H3, L3, N3, Y3, AB3, B4, P4, AF4, AH4, C5, F5, K5, V5, AA5, AD5, N6, R6, AJ6, B7, E7, K7, AA7, AE7, AG7, AD8	Power for DDR SDRAM I/O Voltage (2.5 or 1.8 V)	GVDD	—
OVDD	AC10, AF12, AJ12, K23, Y23, R24, AD24, L25, W25, AB26, U27, M28, Y28, G10, A11, C11	PCI, USB, and other Standard (3.3 V)	OVDD	—
No Connect				
NC	F16, F17, AD16, AD17	—	—	8
Pull Down				

Table 73. Configurable Clock Units (continued)

Unit	Default Frequency	Options
PCI Express1, 2	csb_clk/3	Off, c*sb_clk, csb_clk/2, csb_clk/3*
SATA1, 2	csb_clk/3	Off, *csb_clk*

1 This only applies to I^2C1 (I^2C2 clock is not configurable).

This table provides the operating frequencies for the TePBGA II package under recommended operating conditions (see Table 3).

Table 74. Operating Frequencies for TePBGA II

Parameter[1]	Minimum Operating Frequency (MHz)	Maximum Operating Frequency (MHz)
e300 core frequency (*core_clk*)	333	800
Coherent system bus frequency (*csb_clk*)	133	400
DDR2 memory bus frequency (MCK)[1]	250	400
DDR1 memory bus frequency (MCK) [2]	167	333
Local bus frequency (LCLK*n*)[1]	—	133
Local bus controller frequency (*lbc_clk*)	—	400
PCI input frequency (CLKIN or PCI_CLK)	25	66
eTSEC frequency	133	400
Security encryption controller frequency	—	200
USB controller frequency	—	200
eSDHC controller frequency	—	200
PCI Express controller frequency	—	400
SATA controller frequency	—	200

Notes:
1. The CLKIN frequency, RCWLR[SPMF], and RCWLR[COREPLL] settings must be chosen such that the resulting *csb_clk*, MCK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies. The value of SCCR[xCM] must be programmed such that the maximum internal operating frequency of the Security core, USB modules, SATA, and eSDHC will not exceed their respective value listed in this table.
2. The DDR data rate is 2× the DDR memory bus frequency.
3. The local bus frequency is ½, ¼, or 1/8 of the *lbiu_clk* frequency (depending on LCRR[CLKDIV]) which is in turn 1× or 2× the *csb_clk* frequency (depending on RCWLR[LBCM]).

Table 77. CSB Frequency Options for Host Mode

CFG_CLKIN_DIV at Reset[1]	SPMF	*csb_clk* : Input Clock Ratio[1]	Input Clock Frequency (MHz)[2]		
			25	33.33	66.67
			csb_clk Frequency (MHz)		
High	0010	2 : 1			133
High	0011	3 : 1			200
High	0100	4 : 1		133	267
High	0101	5 : 1		167	333
High	0110	6 : 1	150	200	400
High	0111	7 : 1	175	233	
High	1000	8 : 1	200	267	
High	1001	9 : 1	225	300	
High	1010	10 : 1	250	333	
High	1011	11 : 1	275	367	
High	1100	12 : 1	300	400	
High	1101	13 : 1	325		
High	1110	14 : 1	350		
High	1111	15 : 1	375		

Notes:
1. CFG_CLKIN_DIV select the ratio between CLKIN and PCI_SYNC_OUT.
2. CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

Table 78. CSB Frequency Options for Agent Mode

CFG_CLKIN_DIV at reset[1]	SPMF	*csb_clk* : Input Clock Ratio[1]	Input Clock Frequency (MHz)[2]		
			25	33.33	66.67
			csb_clk Frequency (MHz)		
Low	0010	2 : 1			133
Low	0011	3 : 1			200
Low	0100	4 : 1		133	267
Low	0101	5 : 1		167	333
Low	0110	6 : 1	150	200	400

Table 79. e300 Core PLL Configuration (continued)

RCWLR[COREPLL]			*core_clk* : *csb_clk* Ratio	VCO Divider [1]
0–1	2–5	6		
01	**0001**	1	1.5:1	4
10	**0001**	1	1.5:1	8
00	**0010**	0	2:1	2
01	**0010**	0	2:1	4
10	**0010**	0	2:1	8
00	**0010**	1	2.5:1	2
01	**0010**	1	2.5:1	4
10	**0010**	1	2.5:1	8
00	**0011**	0	3:1	2
01	**0011**	0	3:1	4
10	**0011**	0	3:1	8
00	**0011**	1	3.5:1	2
01	**0011**	1	3.5:1	4
10	**0011**	1	3.5:1	8
00	**0100**	0	4:1	2
01	**0100**	0	4:1	4
10	**0100**	0	4:1	8

Notes:
1. Core VCO frequency = Core frequency × VCO divider. Note that VCO divider has to be set properly so that the core VCO frequency is in the range of 800–1600 MHz.

23.3 Suggested PLL Configurations

This table shows suggested PLL configurations for different input clocks (LBCM = 0).

Table 80. Example Clock Frequency Combinations

								eLBC [1]			e300 Core [1]				
Ref [1]	**LBCM**	**DDRCM**	**SVCOD**	**SPMF**	**Sys VCO[1,2]**	**CSB[1,3]**	**DDR data rate[1,4]**	**/2**	**/4**	**/8**	**× 1**	**× 1.5**	**× 2**	**× 2.5**	**× 3**
25.0	0	1	2	5	500	125	250	62.5	31.3	15.6	—	—	—	—	375
25.0	0	1	2	6	600	150	300	75 [6]	37.5	18.8	—	—	—	375	450
33.3	0	1	2	5	667	167	333	83.3 [6]	41.6	20.8	—	—	333	416	500
33.3	0	1	2	4	533	133	267	66.7	33.3	16.7	—	—	—	333	400

26.1 Part Numbers Fully Addressed by This Document

Table 84 provides the Freescale part numbering nomenclature for this chip. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

Table 84. Part Numbering Nomenclature

MPC	*8377*	*E*	*C*	*ZQ*	*AF*	*D*	*A*
Product Code	**Part Identifier**	**Encryption Acceleration**	**Temperature Range [1]**	**Package [2]**	**e300 core Frequency [3]**	**DDR Data Rate**	**Revision Level [4]**
MPC	8377	Blank = Not included E = included	Blank = 0°C (T_a) to 125°C (T_j) C = –40°C (T_a) to 125°C (T_j)	VR = Pb-free 689 TePBGA II	AN = 800 MHz AL = 667 MHz AJ = 533 MHz AG = 400 MHz	G = 400 MHz F = 333 MHz D = 266 MHz	Blank = Freescale ATMC fab A = GlobalFoundries fab

Note:

1 Contact local Freescale office on availability of parts with an extended temperature range.

2 See Section 22, "Package and Pin Listings," for more information on the available package type.

3 Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.

4 No design changes occurred between initial parts and the revision "*A*" parts. Only the fab source has changed in moving to revision "*A*" parts. Initial revision parts and revision "*A*" parts are form, fit, function, and reliability equivalent.

This table lists the available core and DDR data rate frequency combinations.

Table 85. Available Parts (Core/DDR Data Rate)

MPC8377E	MPC8378E	MPC8379E
800 MHz/400 MHz	800 MHz/400 MHz	800 MHz/400 MHz
667 MHz/400 MHz	667 MHz/400 MHz	667 MHz/400 MHz
533 MHz/333 MHz	533 MHz/333 MHz	533 MHz/333 MHz
400 MHz/266 MHz	400 MHz/266 MHz	400 MHz/266 MHz