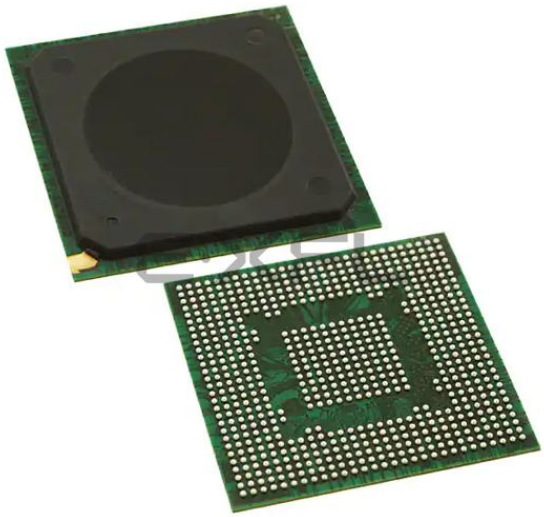

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c4s
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	667MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 125°C (TA)
Security Features	-
Package / Case	689-BBGA Exposed Pad
Supplier Device Package	689-TEPBGA II (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8377vralg

1.10 PCI Express Controller

The PCI Express controller includes the following features:

- PCI Express 1.0a compatible
- Two ×1 links or one ×2 link width
- Auto-detection of number of connected lanes
- Selectable operation as root complex or endpoint
- Both 32- and 64-bit addressing
- 128-byte maximum payload size
- Support for MSI and INTx interrupt messages
- Virtual channel 0 only
- Selectable Traffic Class
- Full 64-bit decode with 32-bit wide windows
- Dedicated four channel descriptor-based DMA engine per interface

1.11 Serial ATA (SATA) Controllers

The serial ATA (SATA) controllers have the following features:

- Supports *Serial ATA Rev 2.5 Specification*
- Spread spectrum clocking on receive
- Asynchronous notification
- Hot Plug including asynchronous signal recovery
- Link power management
- Native command queuing
- Staggered spin-up and port multiplier support
- Port multiplier support
- SATA 1.5 and 3.0 Gb/s operation
- Interrupt driven
- Power management support
- Error handling and diagnostic features
  - — Far end/near end loopback
  - — Failed CRC error reporting
  - — Increased ALIGN insertion rates
- Scrambling and CONT override

Table 2. Absolute Maximum Ratings[1] (continued)

Characteristic		Symbol	Max Value	Unit	Note
Input voltage	DDR DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2, 4
	DDR DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	2, 4
	Three-speed Ethernet signals	LV_{IN}	–0.3 to (LV_{DD} + 0.3)	V	—
	PCI, DUART, CLKIN, system control and power management, I^2C, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	3, 4, 5
	Local Bus	LB_{IN}	–0.3 to (LBV_{DD} + 0.3)	V	—
Storage temperature range		T_{STG}	–55 to 150	°C	—

Notes:
1. Functional and tested operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. (M,O)V_{IN} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
5. Overshoot/undershoot by OV_{IN} on the PCI interface does not comply to the *PCI Electrical Specification* for 3.3-V operation, as shown in Figure 2.
6. L[1,2]_$n$$V_{DD}$ includes $SDAV_{DD\_0}$, $XCOREV_{DD}$, and $XPADV_{DD}$ power inputs.

2.1.2 Power Supply Voltage Specification

This table provides recommended operating conditions for the device. Note that the values in this table are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

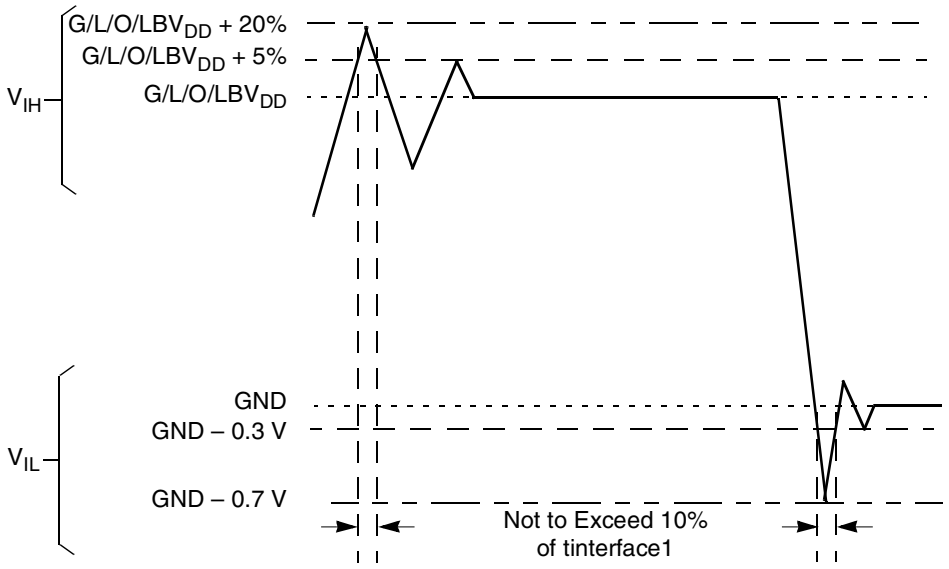
Characteristic		Symbol	Recommended Value	Unit	Note
Core supply voltage	up to 667 MHz	V_{DD}	1.0 ± 50 mV	V	1
	800 MHz		1.05 ± 50 mV	V	1
PLL supply voltage (e300 core, eLBC and system)	up to 667 MHz	AV_{DD}	1.0 ± 50 mV	V	1, 2
	800 MHz		1.05 ± 50 mV	V	1, 2
DDR1 and DDR2 DRAM I/O voltage		GV_{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	1
Three-speed Ethernet I/O, MII management voltage		LV_{DD}[1,2]	3.3 V ± 165 mV 2.5 V ± 125 mV	V	—
PCI, local bus, DUART, system control and power management, I^2C, and JTAG I/O voltage		OV_{DD}	3.3 V ± 165 mV	V	1
Local Bus		LBV_{DD}	1.8 V ± 90 mV 2.5 V ± 125 mV 3.3 V ± 165 mV	V	—

Table 3. Recommended Operating Conditions (continued)

Characteristic		Symbol	Recommended Value	Unit	Note
SerDes	up to 667 MHz	L[1,2]_nV_{DD}	1.0 ± 50 mV	V	1, 3
	800 MHz		1.05 V ± 50 mV	V	1, 3
Operating temperature range	commerical	T_a T_j	T_a=0 (min)— T_j=125 (max)	°C	—
	extended temperature	T_a T_j	T_a=–40 (min)— T_j=125 (max)	°C	—

Notes:
1. GV_{DD}, OV_{DD}, AV_{DD}, and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.
2. AV_{DD} is the input to the filter discussed in Section 25.1, "PLL Power Supply Filtering," and is not necessarily the voltage at the AVDD pin.
3. L[1,2]_nV_{DD}, $SDAV_{DD\_0}$, $XCOREV_{DD}$, and $XPADV_{DD}$ power inputs.

This figure shows the undershoot and overshoot voltages at the interfaces of the device.



Note:
1. Note that $t_{interface}$ refers to the clock period associated with the bus clock interface.
2. Note that with the PCI overshoot allowed (as specified above), the device does not fully comply with the maximum AC ratings and device protection guideline outlined in the *PCI Rev. 2.3 Specification* (Section 4.2.2.3).

Figure 2. Overshoot/Undershoot Voltage for GV_{DD}/LV_{DD}/OV_{DD}/LBV_{DD}

voltage supplies—GV_{DD}, LV_{DD}, and OV_{DD}—do not have any ordering requirements with respect to one another.

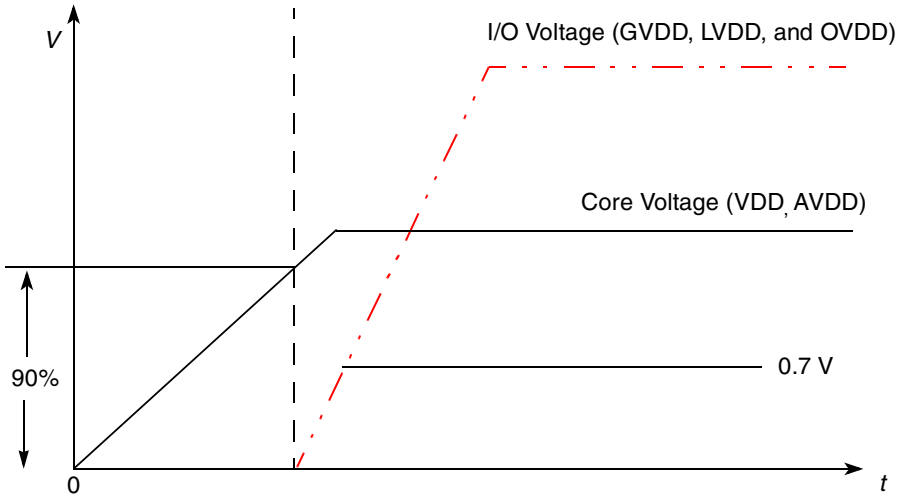


Figure 3. Power-Up Sequencing Example

Note that the SerDes power supply (L[1,2]_$n$$V_{DD}$) should follow the same timing as the core supply (V_{DD}).

The device does not require the core supply voltage and I/O supply voltages to be powered down in any particular order.

3 Power Characteristics

The estimated typical power dissipation for the chip device is shown in this table.

Table 5. Power Dissipation [1]

Core Frequency (MHz)	CSB/DDR Frequency (MHz)	Sleep Power at T_j = 65°C (W) [2]	Typical Application at T_j = 65°C (W) [2]	Typical Application at T_j = 125°C (W) [3]	Max Application at T_j = 125°C (W) [4]
333	333	1.45	1.9	3.2	3.8
	167	1.45	1.8	3.0	3.6
400	400	1.45	2.0	3.3	4.0
	266	1.45	1.9	3.1	3.8
450	300	1.45	2.0	3.2	3.8
	225	1.45	1.9	3.1	3.7
500	333	1.45	2.0	3.3	3.9
	250	1.45	1.9	3.2	3.8
533	355	1.45	2.0	3.3	4.0
	266	1.45	2.0	3.2	3.9

Table 6. Typical I/O Power Dissipation (continued)

Interface	Parameter	GV_{DD} (1.8 V)	GV_{DD}/LBV_{DD} (2.5 V)	OV_{DD} (3.3 V)	LV_{DD} (3.3 V)	LV_{DD} (2.5 V)	$L[1,2]\_nV_{DD}$ (1.0 V)	Unit	Comments
PCI I/O Load = 30 pf	33 MHz, 32-bit	—	—	0.04	—	—	—	W	—
	66 MHz, 32-bit	—	—	0.07	—	—	—	W	
Local Bus I/O Load = 25 pf	167 MHz, 32-bit	0.09	0.17	0.29	—	—	—	W	—
	133 MHz, 32-bit	0.07	0.14	0.24	—	—	—	W	
	83 MHz, 32-bit	0.05	0.09	0.15	—	—	—	W	
	66 MHz, 32-bit	0.04	0.07	0.13	—	—	—	W	
	50 MHz, 32-bit	0.03	0.06	0.1	—	—	—	W	
eTSEC I/O Load = 25 pf	MII or RMII	—	—	—	0.02	—	—	W	Multiply by number of interfaces used.
	RGMII or RTBI	—	—	—	—	0.05	—	W	—
USB (60MHz Clock)	12 Mbps	—	—	0.01	—	—	—	W	—
	480 Mbps	—	—	0.2	—	—	—	W	
SerDes	per lane	—	—		—	—	0.029	W	—
Other I/O	—	—	—	0.01	—	—	—	W	—

Note: The values given are for typical, and not worst case, switching.

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the chip. Note that the PCI_CLK/PCI_SYNC_IN signal or CLKIN signal is used as the PCI input clock depending on whether the device is configured as a host or agent device. CLKIN is used when the device is in host mode.

Table 15. DDR SDRAM DC Electrical Characteristics for GV_{DD} (typ) = 2.5 V (continued)

Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.18	V	—
Output leakage current	I_{OZ}	–50	50	μA	4
Output high current (V_{OUT} = 1.9 V)	I_{OH}	–15.2	—	mA	—
Output low current (V_{OUT} = 0.38 V)	I_{OL}	15.2	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.
5. See AN3665, “MPC837xE Design Checklist,” for proper DDR termination.

Table 16 provides the DDR capacitance when GV_{DD}(typ) = 2.5 V.

Table 16. DDR SDRAM Capacitance for GV_{DD} (typ) = 2.5 V

Parameter	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the current draw characteristics for MV_{REF}.

Table 17. Current Draw Characteristics for MV_{REF}

Parameter	Symbol	Min	Typ	Max	Unit	Note
Current draw for MV_{REF}	I_{MVREF}				μA	1, 2
DDR1		—	250	600		
DDR2		—	150	400		

Note:
1. The voltage regulator for MV_{REF} must be able to supply up to the stated maximum current.
2. This current is divided equally between MVREF1 and MVREF2, where half the current flows through each pin.

6.2 DDR1 and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface.

6.2.1 DDR1 and DDR2 SDRAM Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR2 SDRAM when GVDD(typ) = 1.8 V.

Table 18. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	MV_{REF} – 0.25	V
AC input high voltage	V_{IH}	MV_{REF} + 0.25	—	V

This table provides the input AC timing specifications for the DDR1 SDRAM when GV_{DD}(typ) = 2.5 V.

Table 19. DDR1 SDRAM Input AC Timing Specifications for 2.5-V Interface

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	MV_{REF} – 0.31	V
AC input high voltage	V_{IH}	MV_{REF} + 0.31	—	V

This table provides the input AC timing specifications for the DDR1 and DDR2 SDRAM interface.

Table 20. DDR1 and DDR2 SDRAM Input AC Timing Specifications

Parameter	Symbol	Min	Max	Unit	Note
Controller skew for MDQS-MDQ/MECC/MDM	t_{CISKEW}			ps	1, 2
400 MHz data rate		–500	500		3
333 MHz data rate		–750	750		—
266 MHz data rate		–750	750		—

Note:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS*n* and any corresponding bit that will be captured with MDQS*n*. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: $t_{DISKEW} = \pm[T/4 - |t_{CISKEW}|]$ where T is the MCK clock period and $|t_{CISKEW}|$ is the absolute value of t_{CISKEW}.
3. This specification applies only to DDR2 interface.

Table 22. DUART DC Electrical Characteristics (continued)

Parameter	Symbol	Min	Max	Unit
Low-level output voltage, I_{OL} = 100 µA	V_{OL}	—	0.2	V
Input current, (0 V ≤V_{IN} ≤ OV_{DD})	I_{IN}	—	±30	µA

Note: The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 2.

7.2 DUART AC Electrical Specifications

this table provides the AC timing parameters for the DUART interface of the device.

Table 23. DUART AC Timing Specifications

Parameter	Value	Unit	Note
Minimum baud rate	256	baud	—
Maximum baud rate	> 1,000,000	baud	1
Oversample rate	16	—	2

Notes:
1. Actual attainable baud rate will be limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the 8^{th} sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16^{th} sample.

8 Ethernet: Enhanced Three-Speed Ethernet (eTSEC)

This section provides the AC and DC electrical characteristics for the enhanced three-speed Ethernet controller.

8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RGMII/RTBI/RMII DC Electrical Characteristics

The electrical characteristics specified here apply to media independent interface (MII), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), reduced media independent interface (RMII) signals, management data input/output (MDIO) and management data clock (MDC).

The MII and RMII interfaces are defined for 3.3 V, while the RGMII and RTBI interfaces can be operated at 2.5 V. The RGMII and RTBI interfaces follow the *Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3*. The RMII interface follows the *RMII Consortium RMII Specification Version 1.2*.

This figure shows the RMII receive AC timing diagram.

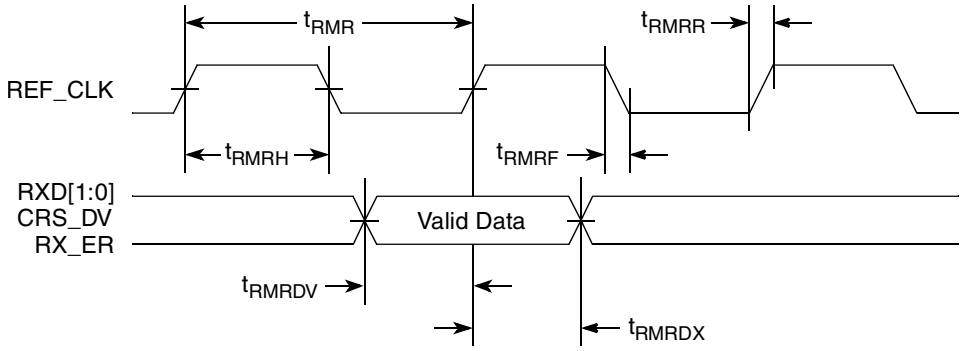


Figure 14. RMII Receive AC Timing Diagram

8.3 Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock).

This figure provides the AC test load for eTSEC.

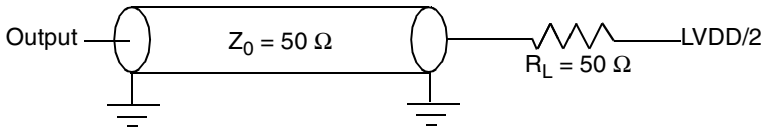


Figure 15. eTSEC AC Test Load

8.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 2.5 V or 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 31 and Table 32.

Table 31. MII Management DC Electrical Characteristics When Powered at 2.5 V

Parameter	Conditions		Symbol	Min	Max	Unit
Supply voltage (2.5 V)	—		LV_{DD1}	2.37	2.63	V
Output high voltage	I_{OH} = –1.0 mA	LV_{DD1} = Min	V_{OH}	2.00	LV_{DD1} + 0.3	V
Output low voltage	I_{OL} = 1.0 mA	LV_{DD1} = Min	V_{OL}	GND – 0.3	0.40	V
Input high voltage	—	LV_{DD1} = Min	V_{IH}	1.7	—	V
Input low voltage	—	LV_{DD1} = Min	V_{IL}	–0.3	0.70	V
Input high current	V_{IN} = LV_{DD1}		I_{IH}	—	20	μA
Input low current	V_{IN} = LV_{DD1}		I_{IL}	–15	—	μA

This table describes the general timing parameters of the local bus interface of the device when in PLL bypass mode.

Table 40. Local Bus General Timing Parameters—PLL Bypass Mode

Parameter	Symbol[1]	Min	Max	Unit	Note
Local bus cycle time	t_{LBK}	15	—	ns	2
Input setup to local bus clock	t_{LBIVKH}	7.0	—	ns	3, 4
Input hold from local bus clock	t_{LBIXKH}	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3.0	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7
Local bus clock to LALE rise	t_{LBKHLR}	—	4.5	ns	—
Local bus clock to output valid	t_{LBKHOV}	—	3.0	ns	3
Local bus clock to output high impedance for LAD/LDP	t_{LBKHOZ}	—	4.0	ns	3, 8

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to falling edge of LCLK0 (for all outputs and for $\overline{\text{LGTA}}$ and LUPWAIT inputs) or rising edge of LCLK0 (for all other inputs).
3. All signals are measured from $LBV_{DD}/2$ of the rising/falling edge of LCLK0 to $0.4 \times LBV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. $t_{LBOTOT1}$ should be used when LBCR[AHD] is set and the load on LALE output pin is at least 10pF less than the load on LAD output pins.
6. $t_{LBOTOT2}$ should be used when LBCR[AHD] is not set and the load on LALE output pin is at least 10pF less than the load on LAD output pins.
7. $t_{LBOTOT3}$ should be used when LBCR[AHD] is not set and the load on LALE output pin equals to the load on LAD output pins.
8. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

This figure provides the AC test load for the local bus.

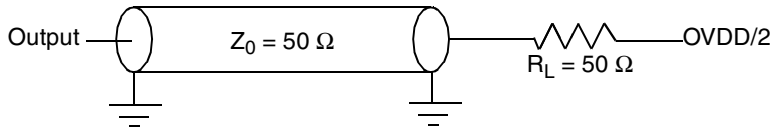


Figure 19. Local Bus AC Test Load

This figures show the local bus signals.

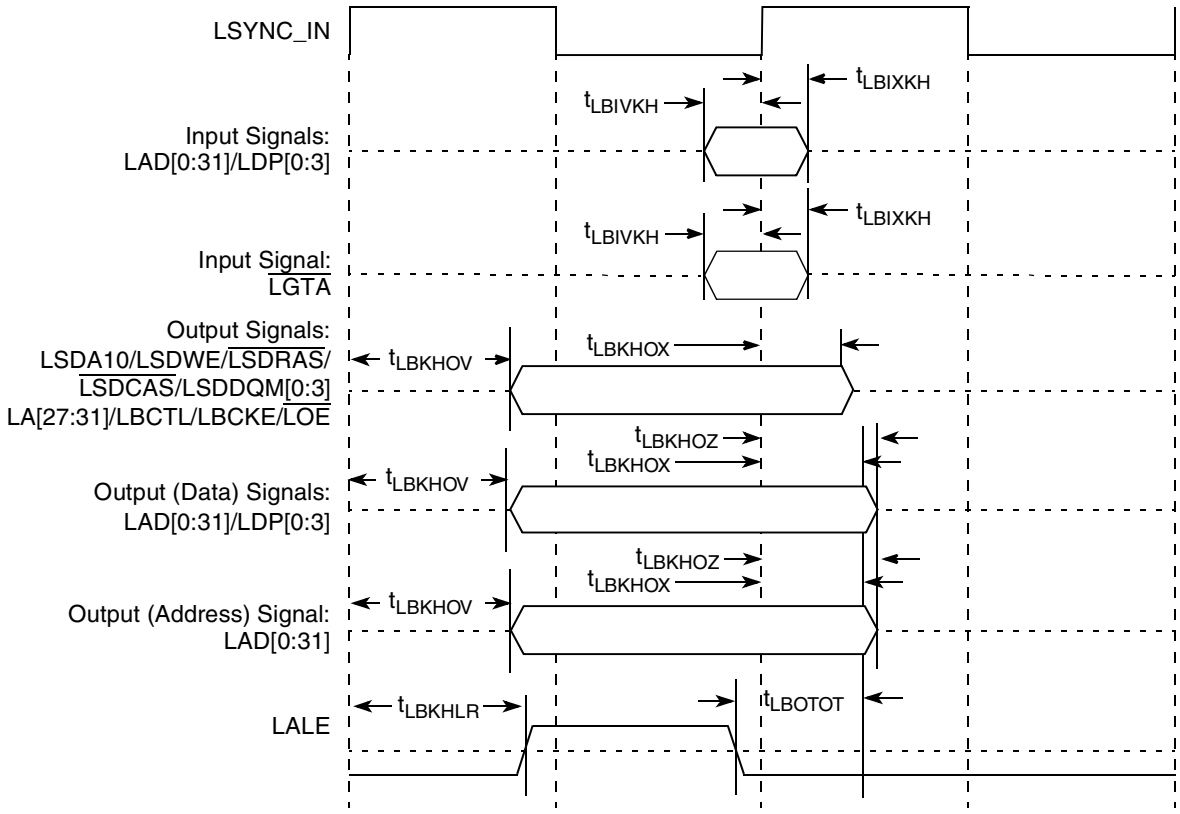


Figure 20. Local Bus Signals, Non-special Signals Only (PLL Enable Mode)

$$t_{CLK\_DELAY} + t_{IH} - t_{SFSKHOX} < t_{SFSCKL} + t_{DATA\_DELAY} \quad \text{Eqn. 5}$$

This means that clock can be delayed versus data up to 15 ns (external delay line) in ideal case of $t_{SFSCLKL}$ = 20 ns:

$t_{CLK\_DELAY} + 5 - 0 < 20 + t_{DATA\_DELAY}$

$t_{CLK\_DELAY} < 15 + t_{DATA\_DELAY}$

11.2.1.3 Full-Speed Write Combined Formula

The following equation is the combined formula to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

$$t_{CLK\_DELAY} + t_{IH} - t_{SFSKHOX} < t_{SFSCKL} + t_{DATA\_DELAY} < t_{SFSCK} + t_{CLK\_DELAY} - t_{ISU} - t_{SFSKHOV} \quad \text{Eqn. 6}$$

11.2.2 Full-Speed Input Path (Read)

This figure provides the data and command input timing diagram.

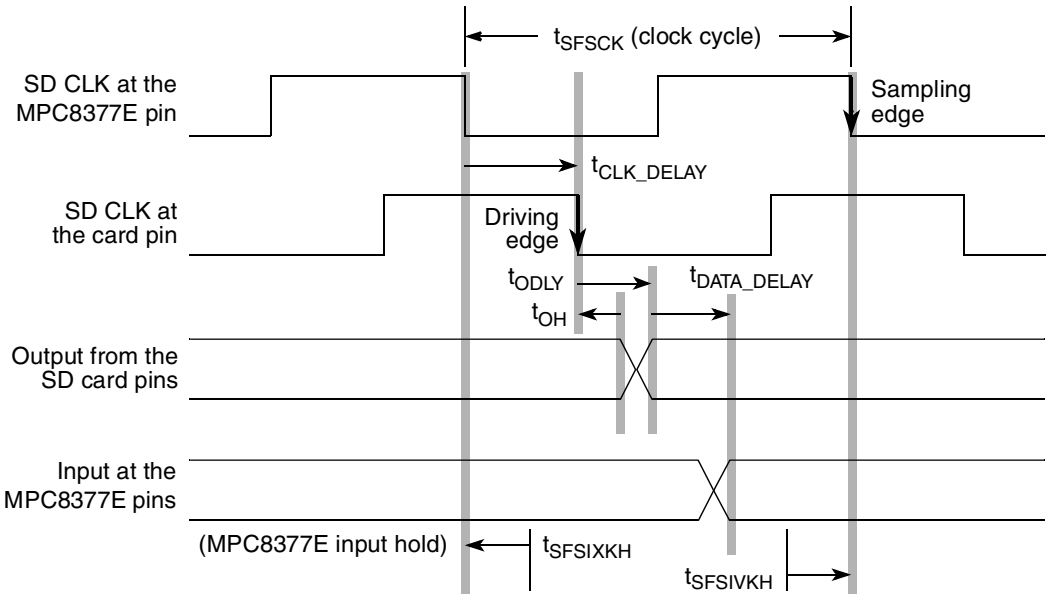


Figure 28. Full Speed Input Path

11.2.2.1 Full-Speed Read Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed combined propagation delay range of the SD_CLK and SD_DAT/CMD signals on the PCB.

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} + t_{ODLY} + t_{SFSIVKH} < t_{SFSCK} \quad \text{Eqn. 7}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} < t_{SFSCK} - t_{ODLY} - t_{SFSIVKH} - t_{INT\_CLK\_DLY} \quad \text{Eqn. 8}$$

This figure provides the eSDHC clock input timing diagram.

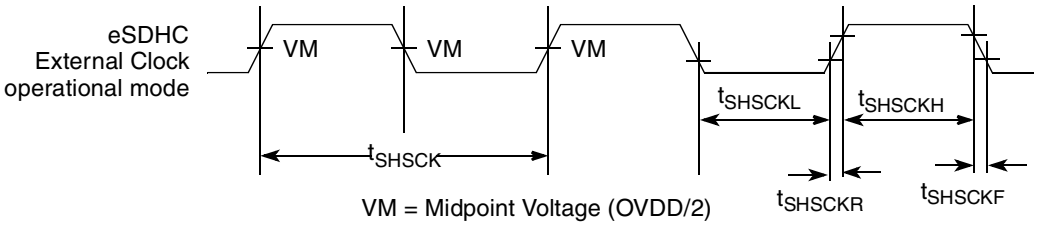


Figure 29. eSDHC Clock Input Timing Diagram

11.3.1 High-Speed Output Path (Write)

This figure provides the data and command output timing diagram.

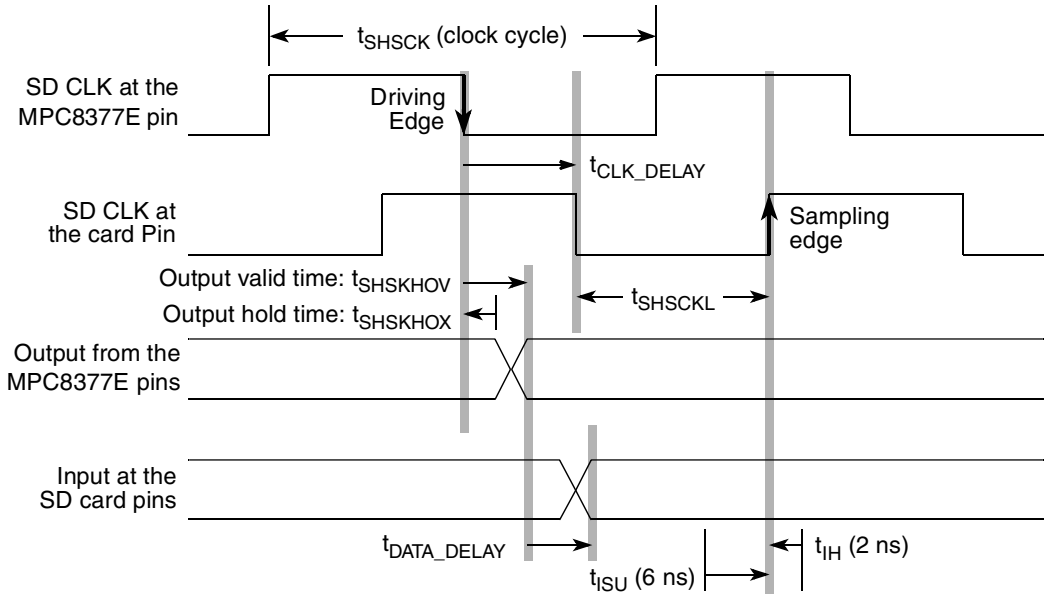


Figure 30. High Speed Output Path

11.3.1.1 High-Speed Write Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

Zero clock delay:

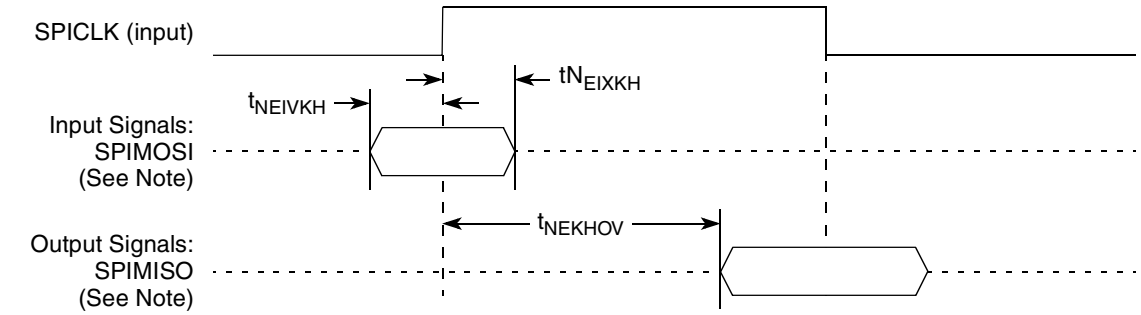
$$t_{SHSKHOV} + t_{DATA\_DELAY} + t_{ISU} < t_{SHSCKL} \quad \textit{Eqn. 10}$$

With clock delay:

$$t_{SHSKHOV} + t_{DATA\_DELAY} + t_{ISU} < t_{SHSCKL} + t_{CLK\_DELAY} \quad \textit{Eqn. 11}$$

$$t_{DATA\_DELAY} - t_{CLK\_DELAY} < t_{SHSCKL} - t_{ISU} - t_{SHSKHOV} \quad \textit{Eqn. 12}$$

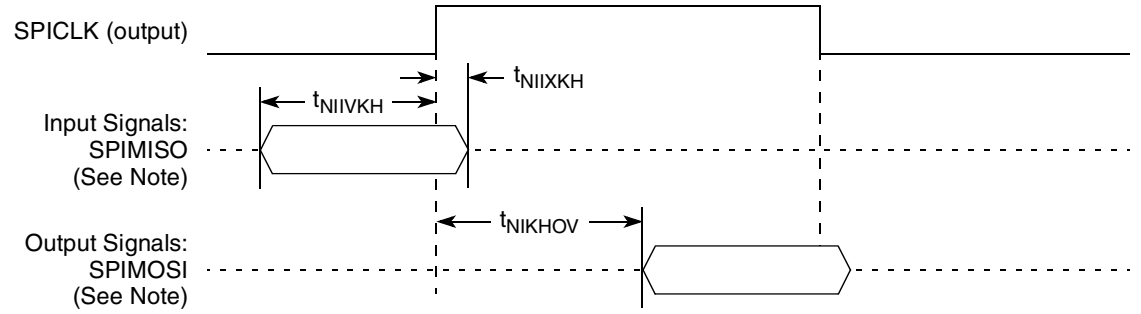
This figure shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 49. SPI AC Timing in Slave Mode (External Clock) Diagram

This figure shows the SPI timing in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 50. SPI AC Timing in Master Mode (Internal Clock) Diagram

21 High-Speed Serial Interfaces (HSSI)

This chip features two serializer/deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications. See Table 1 for the interfaces supported.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

21.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 51 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (SD*n*_TX and $\overline{\text{SD}n\text{\_TX}}$) or a receiver input (SD*n*_RX and $\overline{\text{SD}n\text{\_RX}}$). Each signal swings between A volts and B volts where A > B.

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
MDQ2	C7	I/O	GVDD	11
MDQ3	D8	I/O	GVDD	11
MDQ4	A7	I/O	GVDD	11
MDQ5	A5	I/O	GVDD	11
MDQ6	A3	I/O	GVDD	11
MDQ7	C6	I/O	GVDD	11
MDQ8	D7	I/O	GVDD	11
MDQ9	E8	I/O	GVDD	11
MDQ10	B1	I/O	GVDD	11
MDQ11	D5	I/O	GVDD	11
MDQ12	B3	I/O	GVDD	11
MDQ13	D6	I/O	GVDD	11
MDQ14	C3	I/O	GVDD	11
MDQ15	C2	I/O	GVDD	11
MDQ16	D4	I/O	GVDD	11
MDQ17	E6	I/O	GVDD	11
MDQ18	F6	I/O	GVDD	11
MDQ19	G4	I/O	GVDD	11
MDQ20	F8	I/O	GVDD	11
MDQ21	E4	I/O	GVDD	11
MDQ22	C1	I/O	GVDD	11
MDQ23	G6	I/O	GVDD	11
MDQ24	F2	I/O	GVDD	11
MDQ25	G5	I/O	GVDD	11
MDQ26	H6	I/O	GVDD	11
MDQ27	H4	I/O	GVDD	11
MDQ28	D1	I/O	GVDD	11
MDQ29	G3	I/O	GVDD	11
MDQ30	H5	I/O	GVDD	11
MDQ31	F1	I/O	GVDD	11
MDQ32	W6	I/O	GVDD	11
MDQ33	AC1	I/O	GVDD	11
MDQ34	AC3	I/O	GVDD	11

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
MDQS4	AB5	I/O	GVDD	11
MDQS5	AD1	I/O	GVDD	11
MDQS6	AH1	I/O	GVDD	11
MDQS7	AJ3	I/O	GVDD	11
MDQS8	G1	I/O	GVDD	11
MECC0/MSRCID0	J6	I/O	GVDD	—
MECC1/MSRCID1	J3	I/O	GVDD	—
MECC2/MSRCID2	K2	I/O	GVDD	—
MECC3/MSRCID3	K3	I/O	GVDD	—
MECC4/MSRCID4	J5	I/O	GVDD	—
MECC5/MDVAL	J2	I/O	GVDD	—
MECC6	L5	I/O	GVDD	—
MECC7	L2	I/O	GVDD	—
MODT0	N5	O	GVDD	6
MODT1	U6	O	GVDD	6
MODT2	M6	O	GVDD	6
MODT3	P6	O	GVDD	6
MRAS_B	AA3	O	GVDD	—
MVREF1	K4	I	GVDD	11
MVREF2	W4	I	GVDD	11
MWE_B	Y2	O	GVDD	—
DUART Interface				
UART_SIN1/ MSRCID2/LSRCID2	L28	I/O	OVDD	—
UART_SOUT1/ MSRCID0/LSRCID0	L27	O	OVDD	—
UART_CTS_B[1]/ MSRCID4/LSRCID4	K26	I/O	OVDD	—
UART_RTS_B1	N27	O	OVDD	—
UART_SIN2/ MSRCID3/LSRCID3	K27	I/O	OVDD	—
UART_SOUT2/ MSRCID1/LSRCID1	K28	O	OVDD	—
UART_CTS_B[2]/ MDVAL/LDVAL	K29	I/O	OVDD	—

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
UART_RTS_B[2]	L29	O	OVDD	—
Enhanced Local Bus Controller (eLBC) Interface				
LAD0	E24	I/O	LBVDD	—
LAD1	G28	I/O	LBVDD	—
LAD2	H25	I/O	LBVDD	—
LAD3	F26	I/O	LBVDD	—
LAD4	C26	I/O	LBVDD	—
LAD5	J28	I/O	LBVDD	—
LAD6	F21	I/O	LBVDD	—
LAD7	F23	I/O	LBVDD	—
LAD8	E25	I/O	LBVDD	—
LAD9	E26	I/O	LBVDD	—
LAD10	A23	I/O	LBVDD	—
LAD11	F24	I/O	LBVDD	—
LAD12	G24	I/O	LBVDD	—
LAD13	F25	I/O	LBVDD	—
LAD14	H28	I/O	LBVDD	—
LAD15	G25	I/O	LBVDD	—
LA11/LAD16	F27	I/O	LBVDD	—
LA12/LAD17	B21	I/O	LBVDD	—
LA13/LAD18	A25	I/O	LBVDD	—
LA14/LAD19	C28	I/O	LBVDD	—
LA15/LAD20	H24	I/O	LBVDD	—
LA16/LAD21	E23	I/O	LBVDD	—
LA17/LAD22	B28	I/O	LBVDD	—
LA18/LAD23	D28	I/O	LBVDD	—
LA19/LAD24	A27	I/O	LBVDD	—
LA20/LAD25	C25	I/O	LBVDD	—
LA21/LAD26	B27	I/O	LBVDD	—
LA22/LAD27	H27	I/O	LBVDD	—
LA23/LAD28	E21	I/O	LBVDD	—
LA24/LAD29	F20	I/O	LBVDD	—

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
LA25/LAD30	D29	I/O	LBVDD	—
LA26/LAD31	E20	I/O	LBVDD	—
LA27	H26	O	LBVDD	—
LA28	C29	O	LBVDD	—
LA29	E28	O	LBVDD	—
LA30	B26	O	LBVDD	—
LA31	J25	O	LBVDD	—
LA10/LALE	H29	O	LBVDD	—
LBCTL	A22	O	LBVDD	—
LCLK0	B22	O	LBVDD	—
LCLK1	C23	O	LBVDD	—
LCLK2	B23	O	LBVDD	—
LCS_B0	D25	O	LBVDD	—
LCS_B1	F19	O	LBVDD	—
LCS_B2	C27	O	LBVDD	—
LCS_B3	D24	O	LBVDD	—
LCS_B4/LDP0	C24	I/O	LBVDD	—
LCS_B5/LDP1	B29	I/O	LBVDD	—
LA7/LCS_B6/LDP2	E29	I/O	LBVDD	—
LA8/LCS_B7/LDP3	F29	I/O	LBVDD	—
LFCLE/LGPL0	D21	O	LBVDD	—
LFALE/LGPL1	A26	O	LBVDD	—
LFRE_B/LGPL2/LOE_B	F22	O	LBVDD	—
LFWP_B/LGPL3	C21	O	LBVDD	—
LGPL4/LFRB_B/LGTA_B/ LUPWAIT/LPBSE	J29	I/O	LBVDD	16
LA9/LGPL5	G29	O	LBVDD	—
LSYNC_IN	A21	I	LBVDD	—
LSYNC_OUT	D23	O	LBVDD	—
LWE_B0/LFWE0/LBS_B0	E22	O	LBVDD	—
LWE_B1/LFWE1/LBS_B1	B25	O	LBVDD	—
LWE_B2/LFWE2/LBS_B2	E27	O	LBVDD	—
LWE_B3/LFWE3/LBS_B3	F28	O	LBVDD	—

Table 81. Package Thermal Characteristics for TePBGA II (continued)

Parameter	Symbol	Value	Unit	Note
Junction-to-package natural convection on top	ψ_{JT}	6	°C/W	6

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

24.2 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$ where $P_{I/O}$ is the power dissipation of the I/O drivers.

24.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Generally, the value obtained on a single layer board is appropriate for a tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

24.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

NOTE

The heat sink cannot be mounted on the package.

The thermal performance of a device cannot be adequately predicted from the junction to ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_A + (R_{\theta JB} \times P_D)$$

where:

T_A = ambient temperature for the package (°C)

$R_{\theta JB}$ = junction to board thermal resistance (°C/W) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

24.2.3 Experimental Determination of Junction Temperature

NOTE

The heat sink cannot be mounted on the package.

To determine the junction temperature of the device in the application after prototypes are available, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature and a measure of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_T = thermocouple temperature on top of package (°C)

Ψ_{JT} = junction to ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per the JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

24.2.4 Heat Sinks and Junction-to-Case Thermal Resistance

For the power values the device is expected to operate at, it is anticipated that a heat sink will be required. A preliminary estimate of heat sink performance can be obtained from the following first-cut approach.