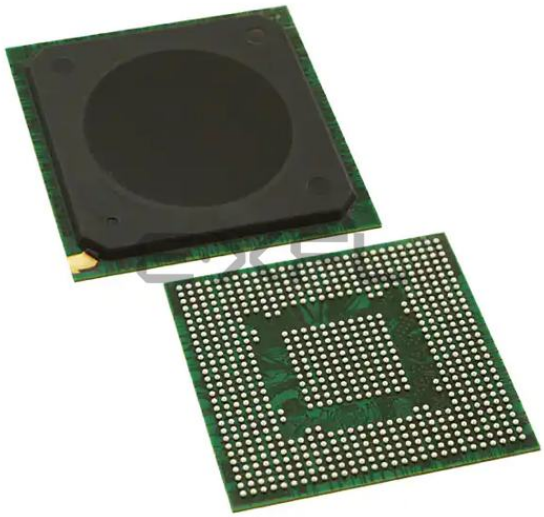

Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c4s
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 125°C (TA)
Security Features	-
Package / Case	689-BBGA Exposed Pad
Supplier Device Package	689-TEPBGA II (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8377cvragda

Table 2. Absolute Maximum Ratings[1] (continued)

Characteristic		Symbol	Max Value	Unit	Note
Input voltage	DDR DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2, 4
	DDR DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	2, 4
	Three-speed Ethernet signals	LV_{IN}	–0.3 to (LV_{DD} + 0.3)	V	—
	PCI, DUART, CLKIN, system control and power management, I^2C, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	3, 4, 5
	Local Bus	LB_{IN}	–0.3 to (LBV_{DD} + 0.3)	V	—
Storage temperature range		T_{STG}	–55 to 150	°C	—

Notes:
1. Functional and tested operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. (M,O)V_{IN} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
5. Overshoot/undershoot by OV_{IN} on the PCI interface does not comply to the *PCI Electrical Specification* for 3.3-V operation, as shown in Figure 2.
6. L[1,2]_$n$$V_{DD}$ includes $SDAV_{DD\_0}$, $XCOREV_{DD}$, and $XPADV_{DD}$ power inputs.

2.1.2 Power Supply Voltage Specification

This table provides recommended operating conditions for the device. Note that the values in this table are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

Characteristic		Symbol	Recommended Value	Unit	Note
Core supply voltage	up to 667 MHz	V_{DD}	1.0 ± 50 mV	V	1
	800 MHz		1.05 ± 50 mV	V	1
PLL supply voltage (e300 core, eLBC and system)	up to 667 MHz	AV_{DD}	1.0 ± 50 mV	V	1, 2
	800 MHz		1.05 ± 50 mV	V	1, 2
DDR1 and DDR2 DRAM I/O voltage		GV_{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	1
Three-speed Ethernet I/O, MII management voltage		LV_{DD}[1,2]	3.3 V ± 165 mV 2.5 V ± 125 mV	V	—
PCI, local bus, DUART, system control and power management, I^2C, and JTAG I/O voltage		OV_{DD}	3.3 V ± 165 mV	V	1
Local Bus		LBV_{DD}	1.8 V ± 90 mV 2.5 V ± 125 mV 3.3 V ± 165 mV	V	—

6.1 DDR1 and DDR2 SDRAM DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR2 SDRAM component(s) of the device when GV_{DD}(typ) = 1.8 V.

Table 13. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Parameter	Symbol	Min	Max	Unit	Note
I/O supply voltage	GV_{DD}	1.71	1.89	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2, 5
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF} + 0.140	GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.140	V	—
Output leakage current	I_{OZ}	–50	50	μA	4
Output high current (V_{OUT} = 1.40 V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.3 V)	I_{OL}	13.4	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.
5. See AN3665, “MPC837xE Design Checklist,” for proper DDR termination.

Table 14 provides the DDR2 capacitance when GV_{DD}(typ) = 1.8 V.

Table 14. DDR2 SDRAM Capacitance for GV_{DD}(typ) = 1.8 V

Parameter	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the recommended operating conditions for the DDR SDRAM component(s) when GV_{DD}(typ) = 2.5 V.

Table 15. DDR SDRAM DC Electrical Characteristics for GV_{DD} (typ) = 2.5 V

Parameter	Symbol	Min	Max	Unit	Note
I/O supply voltage	GV_{DD}	2.375	2.625	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2, 5
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF} + 0.18	GV_{DD} + 0.3	V	—

8.2 MII, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for MII, RGMII, RMII, and RTBI are presented in this section.

8.2.1 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.1.1 MII Transmit AC Timing Specifications

This table provides the MII transmit AC timing specifications.

Table 26. MII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter	Symbol[1]	Min	Typical	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise (20%–80%)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall (80%–20%)	t_{MTXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the MII transmit AC timing diagram.

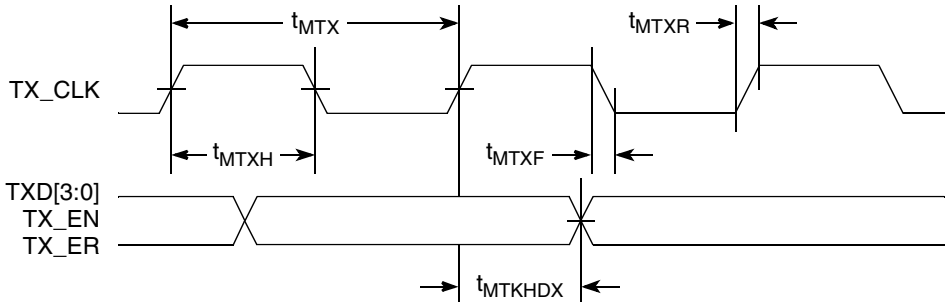

Figure 7. MII Transmit AC Timing Diagram

This figure shows the MII receive AC timing diagram.

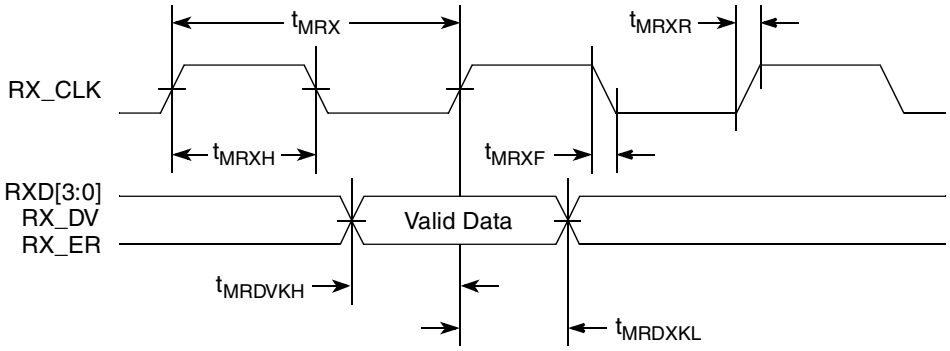

Figure 9. MII Receive AC Timing Diagram

8.2.2 RGMII and RTBI AC Timing Specifications

This table presents the RGMII and RTBI AC timing specifications.

Table 28. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

Parameter	Symbol[1]	Min	Typical	Max	Unit	Note
Data to clock output skew (at transmitter)	t_{SKRGT}	–600	0	600	ps	—
Data to clock input skew (at receiver)	t_{SKRGT}	1.0	—	2.8	ns	2
Clock period	t_{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 1000Base-T	t_{RGTH}/t_{RGT}	45	50	55	%	4
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40	50	60	%	3, 4
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns	—
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns	—
EC_GTX_CLK125 reference clock period	t_{G12}	—	8.0	—	ns	5
EC_GTX_CLK125 reference clock duty cycle measured at $0.5 \times LV_{DD1}$	t_{G125H}/t_{G125}	47	—	53	%	—

Notes:

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between
5. This symbol represents the external EC_GTX_CLK125 and does not follow the original signal naming convention.

This figure provides the AC test load for eTSEC.

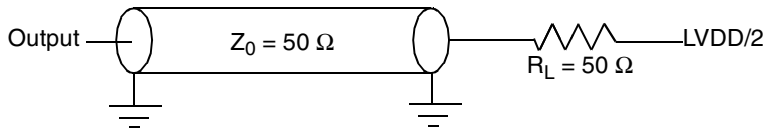

Figure 10. eTSEC AC Test Load

This figure shows the RGMII and RTBI AC timing and multiplexing diagrams.

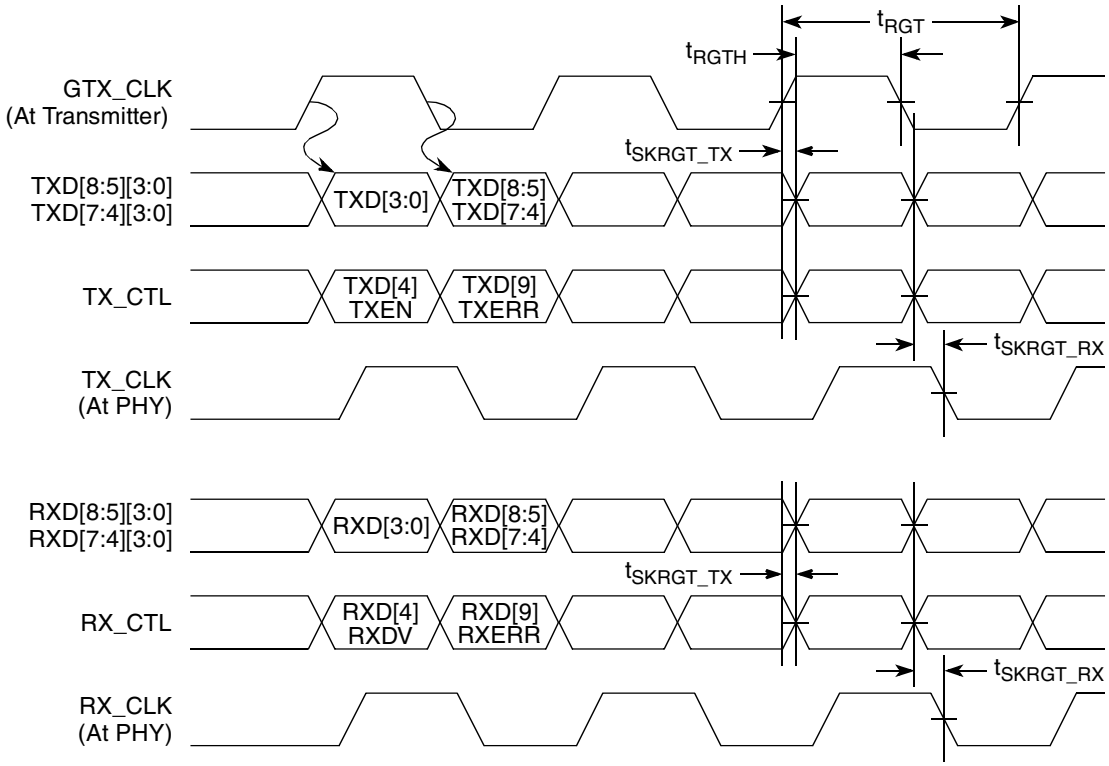

Figure 11. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.2.3 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.3.1 RMII Transmit AC Timing Specifications

This table shows the RMII transmit AC timing specifications.

Table 29. RMII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter	Symbol[1]	Min	Typical	Max	Unit
REF_CLK clock period	t_{RMT}	15.0	20.0	25.0	ns
REF_CLK duty cycle	t_{RMTH}	35	50	65	%
REF_CLK peak-to-peak jitter	t_{RMTJ}	—	—	250	ps
Rise time REF_CLK (20%–80%)	t_{RMTR}	1.0	—	2.0	ns
Fall time REF_CLK (80%–20%)	t_{RMTF}	1.0	—	2.0	ns
REF_CLK to RMII data TXD[1:0], TX_EN delay	t_{RMTDX}	2.0	—	10.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the RMII transmit AC timing diagram.

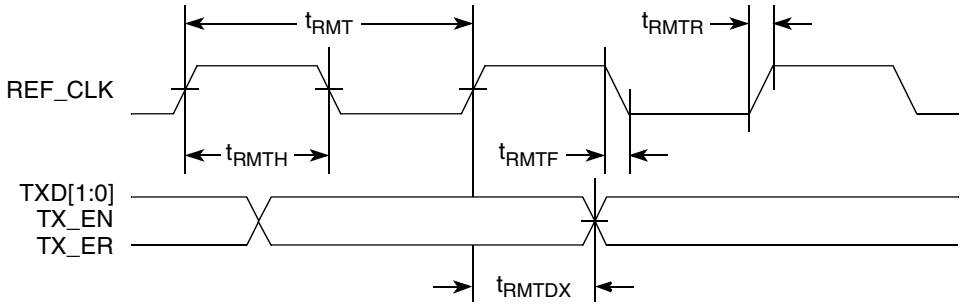

Figure 12. RMII Transmit AC Timing Diagram

Due to the special implementation of the eSDHC, there are constraints regarding the clock and data signals propagation delay on the user board. The constraints are for minimum and maximum delays, as well as skew between the CLK and DAT/CMD signals.

In full speed mode, there is no need to add special delay on the data or clock signals. The user should make sure to meet the timing requirements as described further within this document.

If the system is designed to support both high-speed and full-speed cards, the high-speed constraints should be fulfilled. If the systems is designed to operate up to 25 MHz only, full-speed mode is recommended.

11.1 eSDHC DC Electrical Characteristics

This table provides the DC electrical characteristics for the eSDHC (SD/MMC) interface of the device.

Table 41. eSDHC interface DC Electrical Characteristics

Parameter	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	$0.625 \times OV_{DD}$	$OV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	–0.3	$0.25 \times OV_{DD}$	V
Input current	I_{IN}	—	—	±30	μA
Output high voltage	V_{OH}	I_{OH} = –100 uA, at OV_{DD}(min)	$0.75 \times OV_{DD}$	—	V
Output low voltage	V_{OL}	I_{OL} = +100 uA, at OV_{DD}(min)	—	$0.125 \times OV_{DD}$	V

11.2 eSDHC AC Timing Specifications (Full-Speed Mode)

This section describes the AC electrical specifications for the eSDHC (SD/MMC) interface of the device. This table provides the eSDHC AC timing specifications for full-speed mode as defined in Figure 27 and Figure 28.

Table 42. eSDHC AC Timing Specifications for Full-Speed Mode

At recommended operating conditions OV_{DD} = 3.3 V ± 165 mV.

Parameter	Symbol[1]	Min	Max	Unit	Note
SD_CLK clock frequency—full speed mode	f_{SFSCK}	0	25	MHz	—
SD_CLK clock cycle	t_{SFSCK}	40	—	ns	—
SD_CLK clock frequency—identification mode	f_{SIDCK}	0	400	KHz	—
SD_CLK clock low time	t_{SFSCKL}	15	—	ns	2
SD_CLK clock high time	t_{SFSCKH}	15	—	ns	2
SD_CLK clock rise and fall times	t_{SFSCKR}/ t_{SFSCKF}	—	5	ns	2
Input setup times: SD_CMD, SD_DATx, SD_CD to SD_CLK	$t_{SFSIVKH}$	5	—	ns	2

11.2.1 Full-Speed Output Path (Write)

This figure provides the data and command output timing diagram.

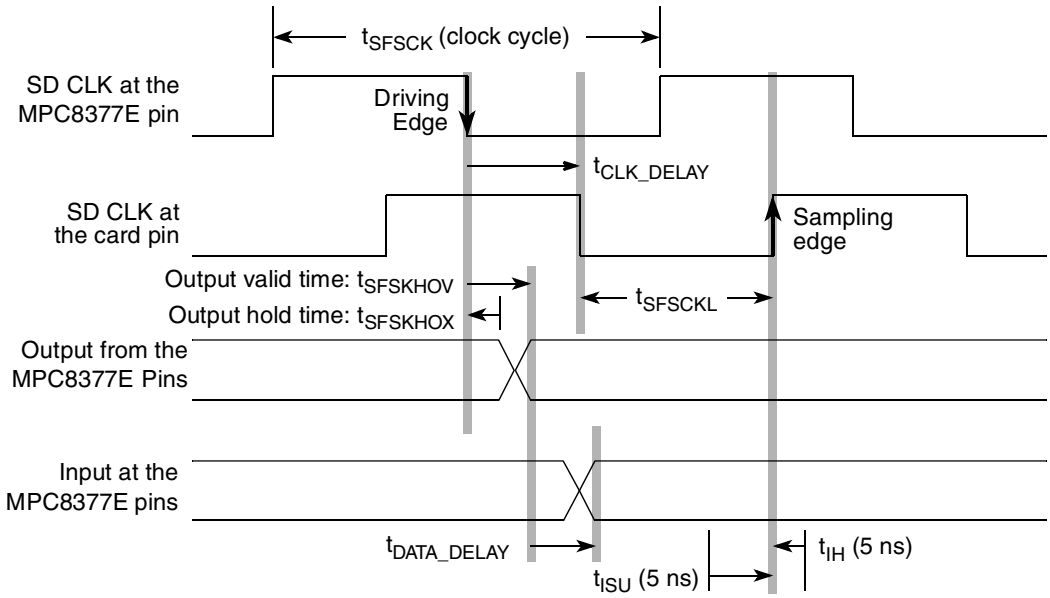

Figure 27. Full Speed Output Path

11.2.1.1 Full-Speed Write Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

No clock delay:

$$t_{SFSKHOV} + t_{DATA\_DELAY} + t_{ISU} < t_{SFSCKL} \quad \textit{Eqn. 1}$$

With clock delay:

$$t_{SFSKHOV} + t_{DATA\_DELAY} + t_{ISU} < t_{SFSCKL} + t_{CLK\_DELAY} \quad \textit{Eqn. 2}$$

$$t_{DATA\_DELAY} + t_{SFSCKL} < t_{SFSCK} + t_{CLK\_DELAY} - t_{ISU} - t_{SFSKHOV} \quad \textit{Eqn. 3}$$

This means that data can be delayed versus clock up to 11 ns in ideal case of t_{SFSCKL} = 20 ns:

$t_{DATA\_DELAY} + 20 < 40 + t_{CLK\_DELAY} - 5 - 4$

$t_{DATA\_DELAY} < 11 + t_{CLK\_DELAY}$

11.2.1.2 Full-Speed Write Meeting Hold (Minimum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

$$t_{CLK\_DELAY} < t_{SFSCKL} + t_{SFSKHOX} + t_{DATA\_DELAY} - t_{IH} \quad \textit{Eqn. 4}$$

14 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the chip.

14.1 PCI DC Electrical Characteristics

This table provides the DC electrical characteristics for the PCI interface of the device. The DC characteristics of the PORESET signal, which can be used as PCI RST in applications where the device is a PCI agent, deviates from the standard PCI levels.

Table 48. PCI DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
High-level input voltage	$V_{OUT} \geq V_{OH}$ (min) or	V_{IH}	2.0	OV_{DD} + 0.5	V
Low-level input voltage	$V_{OUT} \leq V_{OL}$ (max)	V_{IL}	–0.5	$0.3 \times OV_{DD}$	V
High-level output voltage	I_{OH} = –500 µA	V_{OH}	$0.9 \times OV_{DD}$	—	V
Low-level output voltage	I_{OL} = 1500 µA	V_{OL}	—	$0.1 \times OV_{DD}$	V
Input current	$0 V \leq V_{IN} \leq OV_{DD}$	I_{IN}	—	± 30	µA

Note:
- The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 2.

14.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the device. Note that the PCI_CLK/PCI_SYNC_IN or CLKIN signal is used as the PCI input clock depending on whether the chip is configured as a host or agent device. CLKIN is used when the device is in host mode.

This table shows the PCI AC timing specifications at 66 MHz.

Table 49. PCI AC Timing Specifications at 66 MHz

PCI_SYNC_IN clock input levels are with next levels: VIL = $0.1 \times OV_{DD}$, VIH = $0.7 \times OV_{DD}$.

Parameter	Symbol[1]	Min	Max	Unit	Note
Clock to output valid	t_{PCKHOV}	—	6.0	ns	2
Output hold from clock	t_{PCKHOX}	1	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	3.0	—	ns	2, 4

This figure provides the AC test load for PCI.

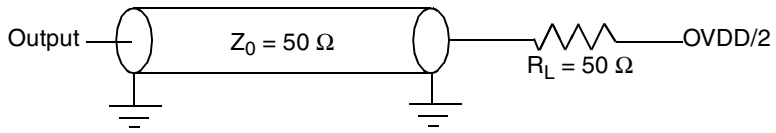

Figure 39. PCI AC Test Load

This figure shows the PCI input AC timing conditions.

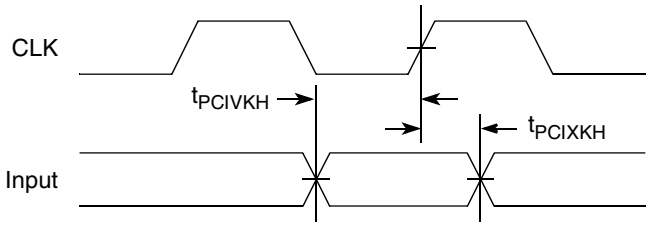

Figure 40. PCI Input AC Timing Measurement Conditions

This figure shows the PCI output AC timing conditions.

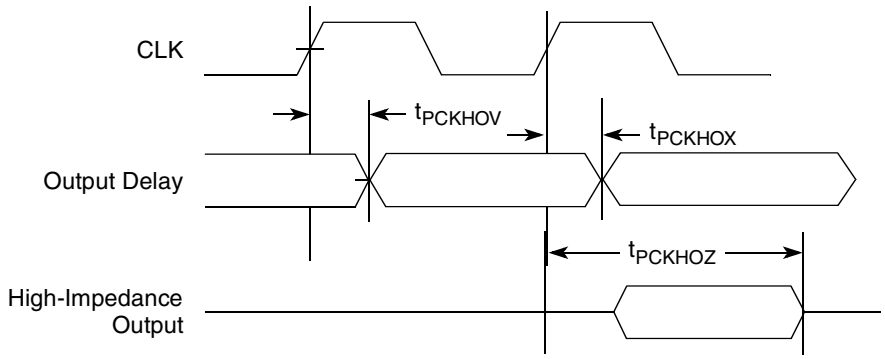

Figure 41. PCI Output AC Timing Measurement Condition

15 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus.

15.1 DC Requirements for PCI Express SD_REF_CLK and SD_REF_CLK

For more information see Section 21, “High-Speed Serial Interfaces (HSSI).”

15.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 44.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D– package pins.

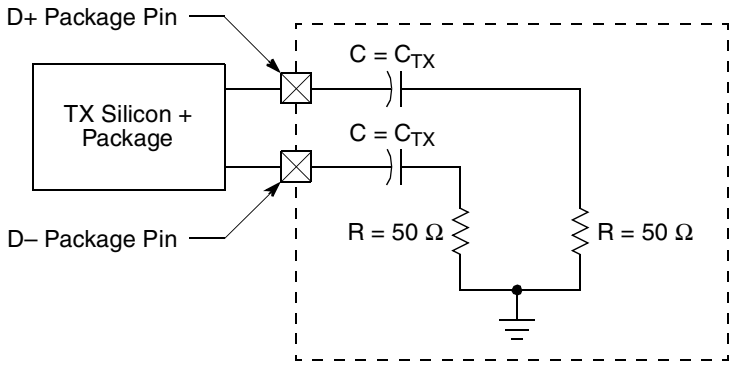

Figure 44. Compliance Test/Measurement Load

16 Serial ATA (SATA)

This section describes the DC and AC electrical specifications for the serial ATA (SATA) of the MPC8377E. Note that the external cabled applications or long backplane applications (Gen1x and Gen2x) are not supported.

16.1 Requirements for SATA REF_CLK

The reference clock is a single ended input clock required for the SATA interface operation. The AC requirements for the SATA reference clock are listed in the Table 54.

Table 54. SATA Reference Clock Input Requirements

Parameter	Condition	Symbol	Min	Typical	Max	Unit	Note
SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ frequency range	—	t_{CLK_REF}	—	100/125/150	—	MHz	1
SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ clock frequency tolerance	—	t_{CLK_TOL}	–350	0	+350	ppm	—
SD_REF_CLK/ $\overline{\text{SD\_REF\_CLK}}$ reference clock duty cycle	Measured at 1.6V	t_{CLK_DUTY}	40	50	60	%	—

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen1i or 1.5 Gbits/s transmission.

Table 56. Gen1i/1.5G Transmitter AC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Note
Channel speed	t_{CH_SPEED}	—	1.5	—	Gbps	—
Unit interval	T_{UI}	666.4333	666.667	670.2333	ps	—
Total jitter, data-data 5 UI	$U_{SATA\_TXTJ5UI}$	—	—	0.355	UI_{p-p}	1
Total jitter, data-data 250 UI	$U_{SATA\_TXTJ250UI}$	—	—	0.47	UI_{p-p}	1
Deterministic jitter, data-data 5 UI	$U_{SATA\_TXDJ5UI}$	—	—	0.175	UI_{p-p}	1
Deterministic jitter, data-data 250 UI	$U_{SATA\_TXDJ250UI}$	—	—	0.22	UI_{p-p}	1

Note:
1. Measured at Tx output pins peak to peak phase variation, random data pattern.

16.2.2 Gen2i/3G Transmitter Specifications

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen2i or 3.0 Gbits/s transmission.

Table 57. Gen 2i/3G Transmitter DC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Note
Tx differential output voltage	V_{SATA_TXDIFF}	400	550	700	mV_{p-p}	1
Tx differential pair impedance	$Z_{SATA\_TXDIFFIM}$	85	100	115	Ω	—

Note:
1. Terminated by 50 Ω load.

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen2i or 3.0 Gbits/s transmission.

Table 58. Gen 2i/3G Transmitter AC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Note
Channel speed	t_{CH_SPEED}	—	3.0	—	Gbps	—
Unit interval	T_{UI}	333.2	333.33	335.11	ps	—
Total jitter $f_{C3dB}=f_{BAUD}/10$	$U_{SATA\_TXTJfB/10}$	—	—	0.3	UI_{p-p}	1
Total jitter $f_{C3dB} = f_{BAUD}/500$	$U_{SATA\_TXTJfB/500}$	—	—	0.37	UI_{p-p}	1

Table 69. SPI DC Electrical Characteristics (continued)

Parameter	Condition	Symbol	Min	Max	Unit
Output low voltage	I_{OL} = 8.0 mA	V_{OL}	—	0.5	V
Output low voltage	I_{OL} = 3.2 mA	V_{OL}	—	0.4	V

20.2 SPI AC Timing Specifications

This table provides the SPI input and output AC timing specifications.

Table 70. SPI AC Timing Specifications

Parameter	Symbol[1]	Min	Max	Unit
SPI outputs—Master mode (internal clock) delay	t_{NIKHOV}	0.5	6	ns
SPI outputs—Slave mode (external clock) delay	t_{NEKHOV}	2	8	ns
SPI inputs—Master mode (internal clock) input setup time	t_{NIIVKH}	4	—	ns
SPI inputs—Master mode (internal clock) input hold time	t_{NIIXKH}	0	—	ns
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).
2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin. The maximum SPICLK input frequency is 66.666 MHz.

This figure provides the AC test load for the SPI.

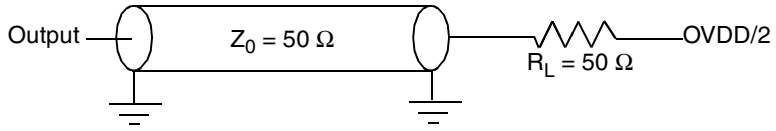

Figure 48. SPI AC Test Load

These figures represent the AC timing from Table 70. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

— The SerDes reference clock input can be either differential or single-ended. Refer to the Differential Mode and Single-ended Mode description below for further detailed requirements.

- The maximum average current requirement that also determines the common mode voltage range
  — When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), since the input is AC-coupled on-chip.
  — This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V ÷ 50 = 8 mA) while the minimum common mode input level is 0.1 V above SGND_SRDS*n* (xcorevss). For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  — If the device driving the SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ inputs cannot drive 50 Ω to SGND_SRDS*n* (xcorevss) DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement
  — This requirement is described in detail in the following sections.

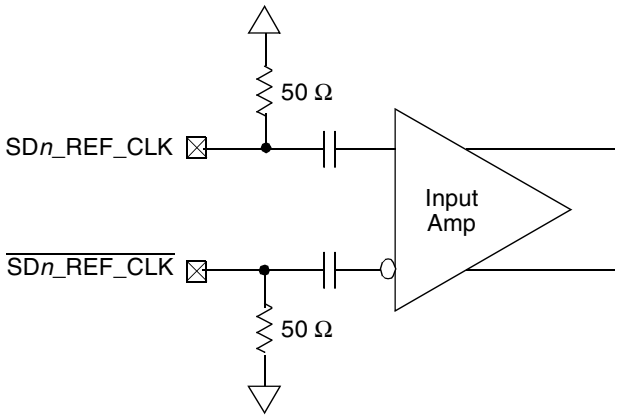

Figure 52. Receiver of SerDes Reference Clocks

21.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the device SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below.

- **Differential Mode**
  — The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing less than 800 mV and

greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.

— For **external DC-coupled** connection, as described in Section 21.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 mV and 400 mV. Figure 53 shows the SerDes reference clock input requirement for DC-coupled connection scheme.

— For **external AC-coupled** connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND_SRDS*n*. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage (SGND_SRDS*n*). Figure 54 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

- **Single-ended Mode**

— The reference clock can also be single-ended. The SD _REF_CLK input amplitude (single-ended swing) must be between 400 mV and 800 mV_{p-p} (from V_{min} to V_{max}) with $\overline{SDn\_REF\_CLK}$ either left unconnected or tied to ground.

— The SD*n*_REF_CLK input average voltage must be between 200 mV and 400 mV. Figure 55 shows the SerDes reference clock input requirement for single-ended signaling mode.

— To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC-coupled externally. For the best noise performance, the reference of the clock could be DC or AC-coupled into the unused phase ($\overline{SDn\_REF\_CLK}$) through the same source impedance as the clock input (SD*n*_REF_CLK) in use.

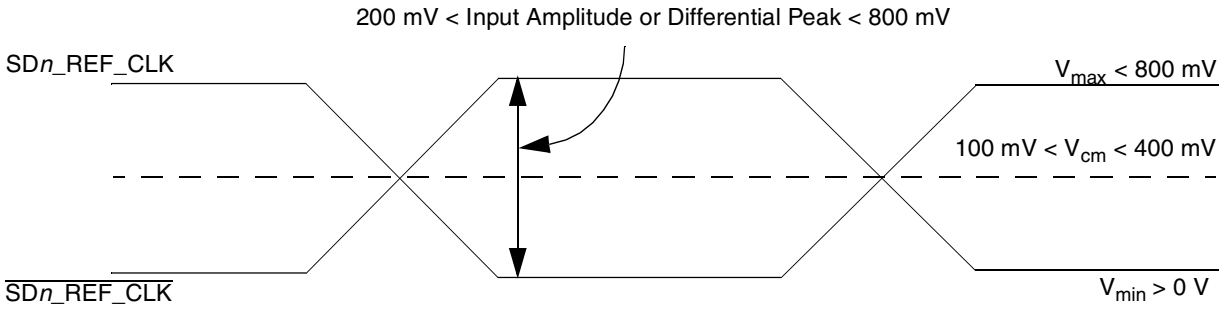

Figure 53. Differential Reference Clock Input DC Requirements (External DC-Coupled)

output driver features a 50-Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.

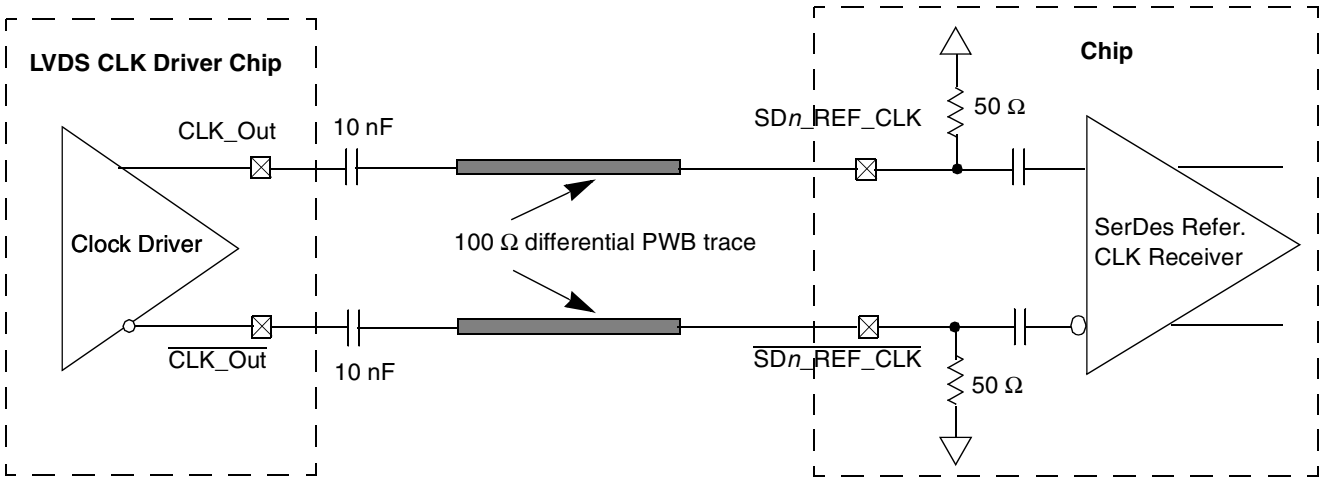

Figure 57. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)

Figure 58 shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Since LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with device SerDes reference clock input's DC requirement, AC-coupling has to be used. Figure 58 assumes that the LVPECL clock driver's output impedance is 50 Ω. R1 is used to DC-bias the LVPECL outputs prior to AC-coupling. Its value could be ranged from 140 Ω to 240 Ω depending on clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50 Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the device SerDes reference clock's differential input amplitude requirement (between 200 mV and 800 mV differential peak). For example, if the LVPECL output's differential peak is 900 mV and the desired SerDes reference clock input amplitude is selected as 600 mV, the attenuation factor is 0.67, which requires R2 = 25 Ω. Consult clock

driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

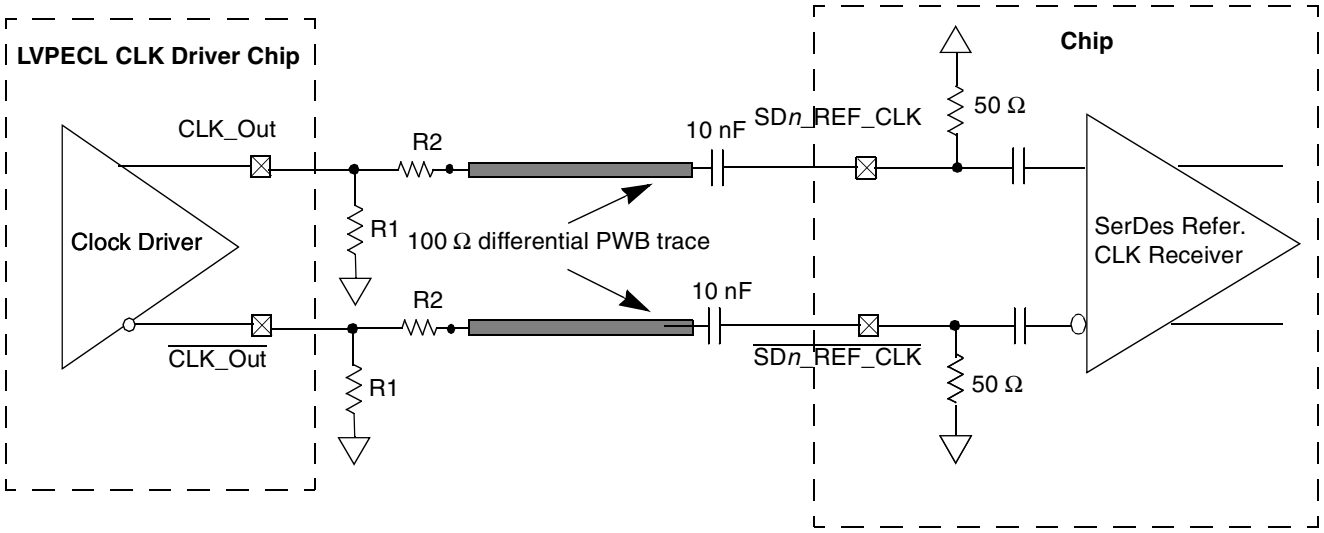

Figure 58. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)

This figure shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with device SerDes reference clock input's DC requirement.

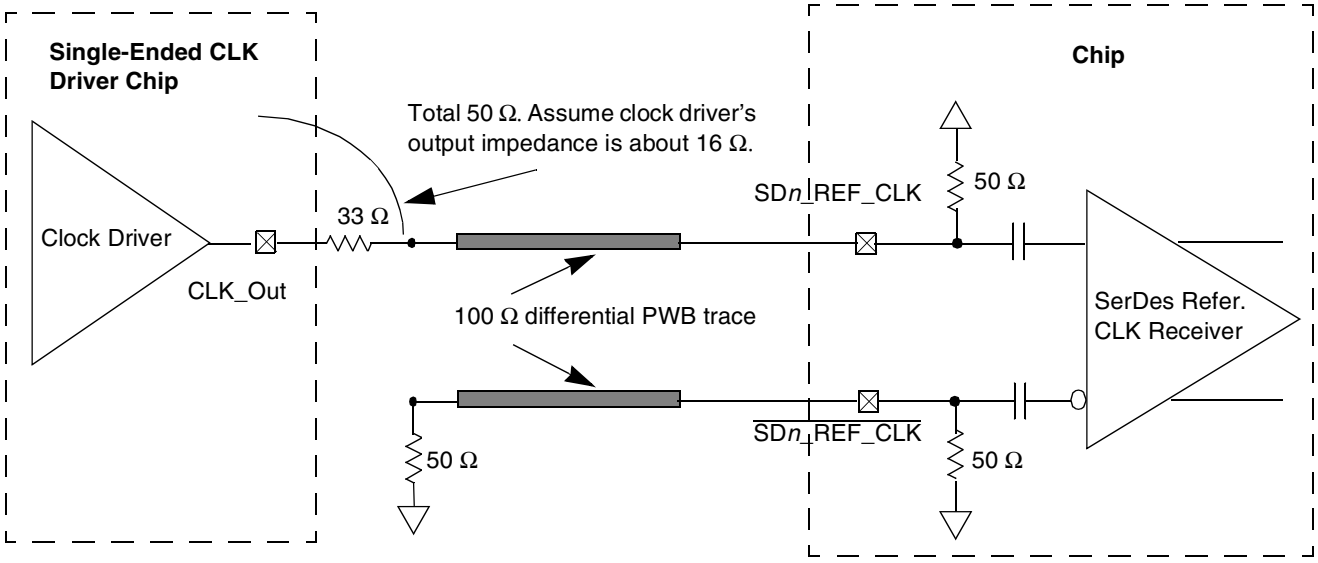

Figure 59. Single-Ended Connection (Reference Only)

21.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100 KHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15 MHz is filtered by the PLL. The most problematic phase noise

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
eTSEC1/GPIO1/GPIO2/CFG_RESET Interface				
TSEC1_COL/GPIO2[20]	AF22	I/O	LVDD1	16
TSEC1_CRS/GPIO2[21]	AE20	I/O	LVDD1	16
TSEC1_GTX_CLK	AJ25	O	LVDD1	16
TSEC1_RX_CLK	AG22	I	LVDD1	16
TSEC1_RX_DV	AD19	I	LVDD1	16
TSEC1_RX_ER/GPIO2[25]	AD20	I/O	LVDD1	16
TSEC1_RXD0	AD22	I	LVDD1	16
TSEC1_RXD1	AE21	I	LVDD1	16
TSEC1_RXD2	AE22	I	LVDD1	16
TSEC1_RXD3	AD21	I	LVDD1	16
TSEC1_TX_CLK	AJ22	I	LVDD1	16
TSEC1_TX_EN	AG23	O	LVDD1	16
TSEC1_TX_ER/CFG_LBMUX	AH22	I/O	LVDD1	16
TSEC1_TXD0/ CFG_RESET_SOURCE[0]	AD23	I/O	LVDD1	16
TSEC1_TXD1/ CFG_RESET_SOURCE[1]	AE23	I/O	LVDD1	16
TSEC1_TXD2/ CFG_RESET_SOURCE[2]	AF23	I/O	LVDD1	16
TSEC1_TXD3/ CFG_RESET_SOURCE[3]	AJ24	I/O	LVDD1	16
EC_GTX_CLK125	AH24	I	LVDD1	16
EC_MDC/CFG_CLKIN_DIV	AJ21	I/O	LVDD1	16
EC_MDIO	AH21	I/O	LVDD1	16
eTSEC2/GPIO1 Interface				
TSEC2_COL/GPIO1[21]/ TSEC1_TMR_TRIG1	AJ27	I/O	LVDD2	16
TSEC2_CRS/GPIO1[22]/ TSEC1_TMR_TRIG2	AG29	I/O	LVDD2	16
TSEC2_GTX_CLK	AF28	O	LVDD2	16
TSEC2_RX_CLK/ TSEC1_TMR_CLK	AF25	I	LVDD2	16
TSEC2_RX_DV/GPIO1[23]	AF26	I/O	LVDD2	16
TSEC2_RX_ER/GPIO1[25]	AG25	I/O	LVDD2	16

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
L1_XCOREVSS	AG14, AG15, AG16, AH16, AG18, AG20	SerDes Core GND	—	—
L1_XPADVDD	AE16, AF16, AD18, AE19, AF19	SerDes I/O Power (1.0 or 1.05 V)	—	—
L1_XPADVSS	AF14, AE17, AF20	SerDes I/O GND	—	—
SerDes2 Interface				
L2_SD_IMP_CAL_RX	C19	I	L2_XPADVDD	—
L2_SD_IMP_CAL_TX	C15	I	L2_XPADVDD	—
L2_SD_REF_CLK	B17	I	L2_XPADVDD	—
L2_SD_REF_CLK_B	A17	I	L2_XPADVDD	—
L2_SD_RXA_N	A19	I	L2_XPADVDD	—
L2_SD_RXA_P	B19	I	L2_XPADVDD	—
L2_SD_RXE_N	A15	I	L2_XPADVDD	—
L2_SD_RXE_P	B15	I	L2_XPADVDD	—
L2_SD_TXA_N	D18	O	L2_XPADVDD	—
L2_SD_TXA_P	E18	O	L2_XPADVDD	—
L2_SD_TXE_N	D15	O	L2_XPADVDD	—
L2_SD_TXE_P	E15	O	L2_XPADVDD	—
L2_SDAVDD_0	A16	SerDes PLL Power (1.0 or 1.05 V)	—	—
L2_SDAVSS_0	C17	SerDes PLL GND	—	—
L2_XCOREVDD	A14, B14, D17, B18, B20	SerDes Core Power (1.0 or 1.05 V)	—	—
L2_XCOREVSS	C14, C16, A18, C18, A20, C20	SerDes Core GND	—	—
L2_XPADVDD	D14, E16, F18, D19, E19	SerDes I/O Power (1.0 or 1.05 V)	—	—
L2_XPADVSS	D16, E17, D20	SerDes I/O GND	—	—
SPI Interface				
SPICLK/SD_CLK	AH9	I/O	OVDD	—

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
SPIMISO/SD_DAT0	AD11	I/O	OVDD	—
SPIMOSI/SD_CMD	AJ9	I/O	OVDD	—
SPISEL_B/SD_CD	AE11	I	OVDD	—
System Control Interface				
SRESET_B	AD12	I/O	OVDD	2
HRESET_B	AE12	I/O	OVDD	1
PORESET_B	AE14	I	OVDD	—
Test Interface				
TEST	E10	I	OVDD	10
TEST_SEL0	D10	I	OVDD	13
TEST_SEL1	D12	I	OVDD	13
Thermal Management				
Reserved	F15	I	—	14
Power Supply Signals				
LVDD1	AC21, AG21, AH23	Power for eTSEC 1 I/O (2.5 V, 3.3 V)	LVDD1	—
LVDD2	AG24, AH27, AH29	Power for eTSEC 2 I/O (2.5 V, 3.3 V)	LVDD2	—
LBVDD	G20, D22, A24, G26, D27, A28	Power for eLBC (3.3, 2.5, or 1.8 V)	LBVDD	—
VDD	K10, L10, M10, N10, P10, R10, T10, U10, V10, W10, Y10, K11, R11, Y11, K12, Y12, K13, Y13, K14, Y14, K15, L15, W15, Y15, K16, Y16, K17, Y17, K18, Y18, K19, R19, Y19, K20, L20, M20, N20, P20, R20, T20, U20, V20, W20, Y20	Power for Core (1.0 V or 1.5 V)	VDD	—