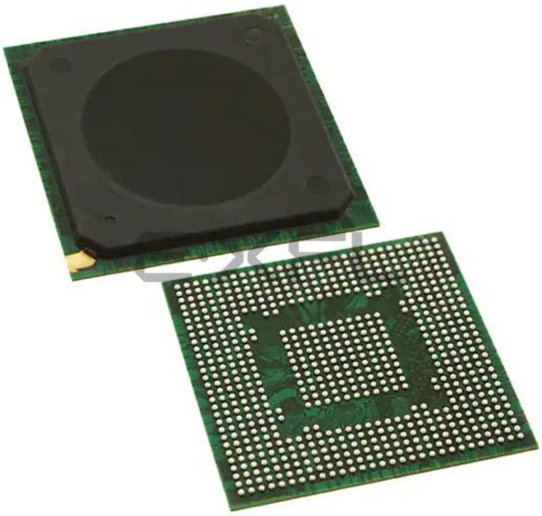

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c4s
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	533MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 125°C (TA)
Security Features	-
Package / Case	689-BBGA Exposed Pad
Supplier Device Package	689-TEPBGA II (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8377cvrajfa

2.1.3 chipOutput Driver Characteristics

This table provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 4. Output Drive Capability

Driver Type[1]	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	45	LBV_{DD} = 2.5 V, 3.3 V
	40	LBV_{DD} = 1.8 V
PCI signals	25	OV_{DD} = 3.3 V
DDR1 signal	18	GV_{DD} = 2.5 V
DDR2 signal	18	GV_{DD} = 1.8 V
eTSEC 10/100/1000 signals	45	LV_{DD} = 2.5 V, 3.3 V
DUART, system control, I^2C, JTAG, SPI, and USB	45	OV_{DD} = 3.3 V
GPIO signals	45	OV_{DD} = 3.3 V

Note:
1. Specialized SerDes output capabilities are described in the relevant sections of these specifications (such as PCI Express and SATA)

2.2 Power Sequencing

The device requires its power rails to be applied in a specific sequence in order to ensure proper device operation. During the power ramp up, before the power supplies are stable and if the I/O voltages are supplied before the core voltage, there may be a period of time that all input and output pins will actively be driven and cause contention and excessive current. To avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltages (V_{DD} and AV_{DD}) before the I/O voltages and assert $\overline{\text{PORESET}}$ before the power supplies fully ramp up. V_{DD} and AV_{DD} must reach 90% of their nominal value before GV_{DD}, LV_{DD}, and OV_{DD} reach 10% of their value, see the following figure. I/O

6.1 DDR1 and DDR2 SDRAM DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR2 SDRAM component(s) of the device when GV_{DD}(typ) = 1.8 V.

Table 13. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Parameter	Symbol	Min	Max	Unit	Note
I/O supply voltage	GV_{DD}	1.71	1.89	V	1
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2, 5
I/O termination voltage	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REF} + 0.140$	$GV_{DD} + 0.3$	V	—
Input low voltage	V_{IL}	–0.3	$MV_{REF} - 0.140$	V	—
Output leakage current	I_{OZ}	–50	50	μA	4
Output high current (V_{OUT} = 1.40 V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.3 V)	I_{OL}	13.4	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, $0 \text{ V} \le V_{OUT} \le GV_{DD}$.
5. See AN3665, "MPC837xE Design Checklist," for proper DDR termination.

Table 14 provides the DDR2 capacitance when GV_{DD}(typ) = 1.8 V.

Table 14. DDR2 SDRAM Capacitance for GV_{DD}(typ) = 1.8 V

Parameter	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the recommended operating conditions for the DDR SDRAM component(s) when GV_{DD}(typ) = 2.5 V.

Table 15. DDR SDRAM DC Electrical Characteristics for GV_{DD} (typ) = 2.5 V

Parameter	Symbol	Min	Max	Unit	Note
I/O supply voltage	GV_{DD}	2.375	2.625	V	1
I/O reference voltage	MV_{REF}	$0.49 \times GV_{DD}$	$0.51 \times GV_{DD}$	V	2, 5
I/O termination voltage	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V	3
Input high voltage	V_{IH}	$MV_{REF} + 0.18$	$GV_{DD} + 0.3$	V	—

Table 15. DDR SDRAM DC Electrical Characteristics for GV_{DD} (typ) = 2.5 V (continued)

Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.18	V	—
Output leakage current	I_{OZ}	–50	50	μA	4
Output high current (V_{OUT} = 1.9 V)	I_{OH}	–15.2	—	mA	—
Output low current (V_{OUT} = 0.38 V)	I_{OL}	15.2	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.
5. See AN3665, "MPC837xE Design Checklist," for proper DDR termination.

Table 16 provides the DDR capacitance when GV_{DD}(typ) = 2.5 V.

Table 16. DDR SDRAM Capacitance for GV_{DD} (typ) = 2.5 V

Parameter	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the current draw characteristics for MV_{REF}.

Table 17. Current Draw Characteristics for MV_{REF}

Parameter	Symbol	Min	Typ	Max	Unit	Note
Current draw for MV_{REF} DDR1 DDR2	I_{MVREF}	 — —	 250 150	 600 400	μA	1, 2

Note:
1. The voltage regulator for MV_{REF} must be able to supply up to the stated maximum current.
2. This current is divided equally between MVREF1 and MVREF2, where half the current flows through each pin.

6.2.2 DDR1 and DDR2 SDRAM Output AC Timing Specifications

This table shows the DDR1 and DDR2 SDRAM output AC timing specifications.

Table 21. DDR1 and DDR2 SDRAM Output AC Timing Specifications

Parameter	Symbol[1]	Min	Max	Unit	Note
MCK*n* cycle time, MCK*n*/$\overline{\text{MCK}n}$ crossing	t_{MCK}	5	10	ns	2
ADDR/CMD output setup with respect to MCK 400 MHz data rate 333 MHz data rate 266 MHz data rate 200 MHz data rate	t_{DDKHAS}	 1.95 2.40 3.15 4.20	 — — — —	ns	3, 7
ADDR/CMD output hold with respect to MCK 400 MHz data rate 333 MHz data rate 266 MHz data rate 200 MHz data rate	t_{DDKHAX}	 1.95 2.40 3.15 4.20	 — — — —	ns	3, 7
$\overline{\text{MCS}n}$ output setup with respect to MCK 400 MHz data rate 333 MHz data rate 266 MHz data rate 200 MHz data rate	t_{DDKHCS}	 1.95 2.40 3.15 4.20	 — — — —	ns	3
$\overline{\text{MCS}n}$ output hold with respect to MCK 400 MHz data rate 333 MHz data rate 266 MHz data rate 200 MHz data rate	t_{DDKHCX}	 1.95 2.40 3.15 4.20	 — — — —	ns	3
MCK to MDQS skew	t_{DDKHMH}	–0.6	0.6	ns	4, 8
MDQ//MDM output setup with respect to MDQS 400 MHz data rate 333 MHz data rate 266 MHz data rate 200 MHz data rate	t_{DDKHDS}, t_{DDKLDS}	 550 800 1100 1200	 — — — —	ps	5, 8
MDQ//MDM output hold with respect to MDQS 400 MHz data rate 333 MHz data rate 266 MHz data rate 200 MHz data rate	t_{DDKHDX}, t_{DDKLDX}	 700 800 1100 1200	 — — — —	ps	5, 8
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6, 8

This figure shows the RMII receive AC timing diagram.

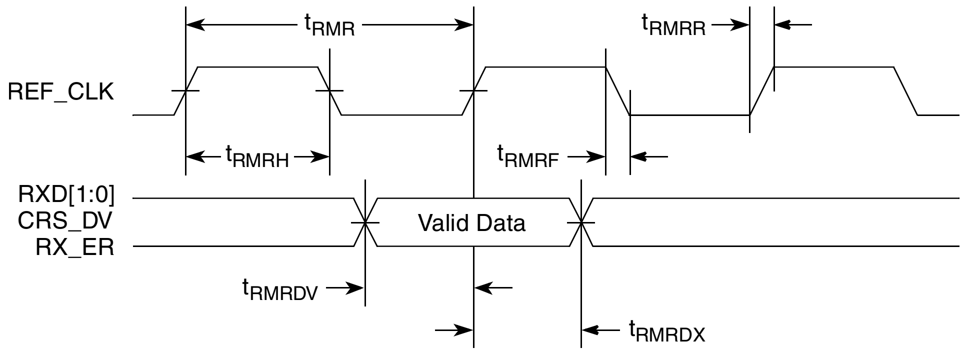

Figure 14. RMII Receive AC Timing Diagram

8.3 Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock).

This figure provides the AC test load for eTSEC.

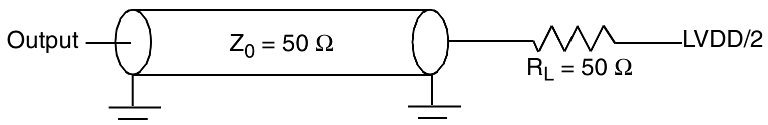

Figure 15. eTSEC AC Test Load

8.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 2.5 V or 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 31 and Table 32.

Table 31. MII Management DC Electrical Characteristics When Powered at 2.5 V

Parameter	Conditions		Symbol	Min	Max	Unit
Supply voltage (2.5 V)	—		LV_{DD1}	2.37	2.63	V
Output high voltage	I_{OH} = –1.0 mA	LV_{DD1} = Min	V_{OH}	2.00	LV_{DD1} + 0.3	V
Output low voltage	I_{OL} = 1.0 mA	LV_{DD1} = Min	V_{OL}	GND – 0.3	0.40	V
Input high voltage	—	LV_{DD1} = Min	V_{IH}	1.7	—	V
Input low voltage	—	LV_{DD1} = Min	V_{IL}	–0.3	0.70	V
Input high current	V_{IN} = LV_{DD1}		I_{IH}	—	20	µA
Input low current	V_{IN} = LV_{DD1}		I_{IL}	–15	—	µA

Table 38. Local Bus DC Electrical Characteristics (LBV_{DD} = 1.8 V)

At recommended operating conditions with LBV_{DD} = 1.8 V.

Parameter	Conditions		Symbol	Min	Max	Unit
Supply voltage 1.8 V	—		LBV_{DD}	1.71	1.89	V
Output high voltage	I_{OH} = –1.0 mA	LBV_{DD} = Min	V_{OH}	LBV_{DD} – 0.45	—	V
Output low voltage	I_{OL} = 1.0 mA	LBV_{DD} = Min	V_{OL}	—	0.45	V
Input high voltage	—	LBV_{DD} = Min	V_{IH}	0.65 × LBV_{DD}	LBV_{DD} + 0.3	V
Input low voltage	—	LBV_{DD} = Min	V_{IL}	–0.3	0.35 × LBV_{DD}	V
Input high current	V_{IN} [1] = LBV_{DD}		I_{IH}	—	10	μA
Input low current	V_{IN} [1] = GND		I_{IL}	–10	—	μA

10.2 Local Bus AC Electrical Specifications

This table describes the general timing parameters of the local bus interface of the device when in PLL enable mode.

Table 39. Local Bus General Timing Parameters—PLL Enable Mode

Parameter	Symbol[1]	Min	Max	Unit	Note
Local bus cycle time	t_{LBK}	7.5	15	ns	2
Input setup to local bus clock (except LUPWAIT/$\overline{\text{LGTA}}$)	t_{LBIVKH}	1.5	—	ns	3, 4
Input hold from local bus clock	t_{LBIXKH}	1.0	—	ns	3, 4
LUPWAIT/$\overline{\text{LGTA}}$ input setup to local bus clock	$t_{LBIVKH1}$	1.5	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7
Local bus clock to LALE rise	t_{LBKHLR}	—	4.5	ns	—
Local bus clock to output valid (except LALE)	t_{LBKHOV}	—	4.5	ns	3

This table describes the general timing parameters of the local bus interface of the device when in PLL bypass mode.

Table 40. Local Bus General Timing Parameters—PLL Bypass Mode

Parameter	Symbol[1]	Min	Max	Unit	Note
Local bus cycle time	t_{LBK}	15	—	ns	2
Input setup to local bus clock	t_{LBIVKH}	7.0	—	ns	3, 4
Input hold from local bus clock	t_{LBIXKH}	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3.0	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7
Local bus clock to LALE rise	t_{LBKHLR}	—	4.5	ns	—
Local bus clock to output valid	t_{LBKHOV}	—	3.0	ns	3
Local bus clock to output high impedance for LAD/LDP	t_{LBKHOZ}	—	4.0	ns	3, 8

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to falling edge of LCLK0 (for all outputs and for $\overline{\text{LGTA}}$ and LUPWAIT inputs) or rising edge of LCLK0 (for all other inputs).
3. All signals are measured from $LBV_{DD}/2$ of the rising/falling edge of LCLK0 to $0.4 \times LBV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. $t_{LBOTOT1}$ should be used when LBCR[AHD] is set and the load on LALE output pin is at least 10pF less than the load on LAD output pins.
6. $t_{LBOTOT2}$ should be used when LBCR[AHD] is not set and the load on LALE output pin is at least 10pF less than the load on LAD output pins.
7. $t_{LBOTOT3}$ should be used when LBCR[AHD] is not set and the load on LALE output pin equals to the load on LAD output pins.
8. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

This figure provides the AC test load for the local bus.

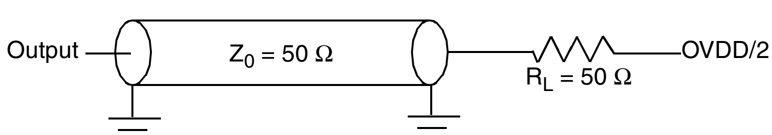

Figure 19. Local Bus AC Test Load

This figures show the local bus signals.

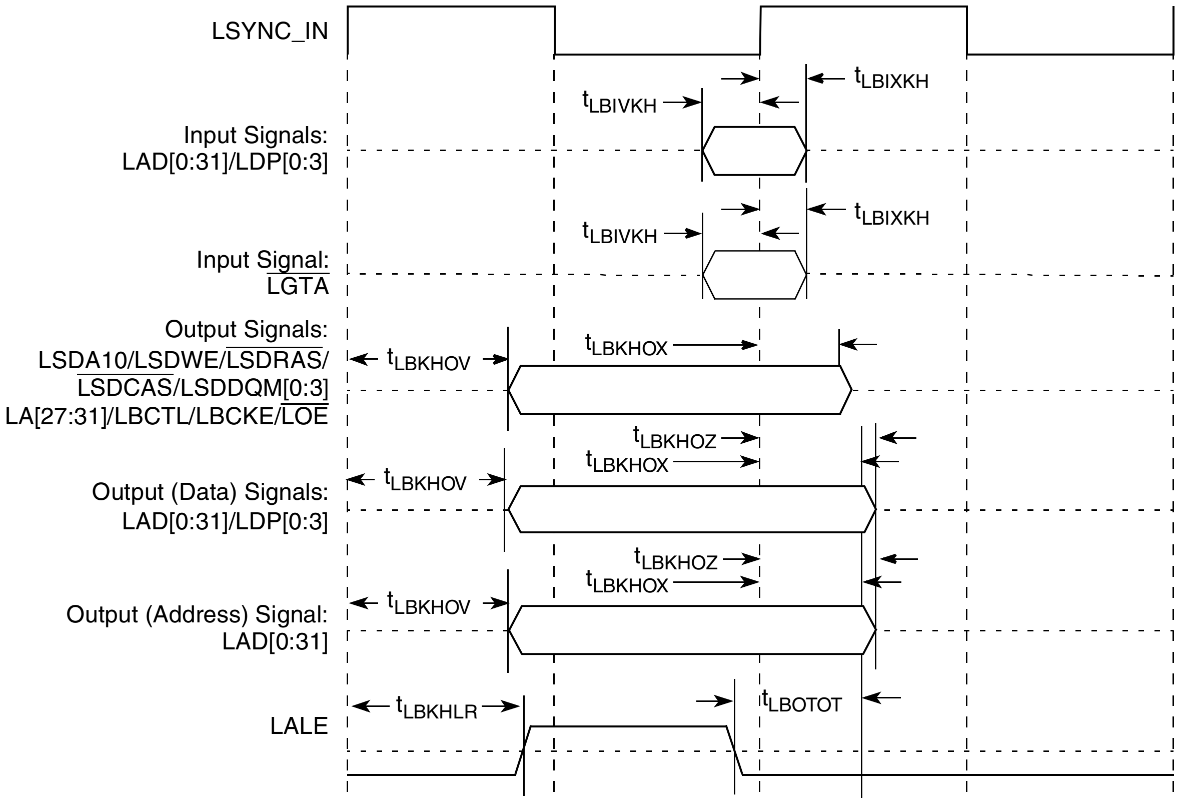

Figure 20. Local Bus Signals, Non-special Signals Only (PLL Enable Mode)

$$t_{CLK\_DELAY} + t_{IH} - t_{SFSKHOX} < t_{SFSCKL} + t_{DATA\_DELAY} \quad \textbf{Eqn. 5}$$

This means that clock can be delayed versus data up to 15 ns (external delay line) in ideal case of $t_{SFSCLKL}$ = 20 ns:

$$t_{CLK\_DELAY} + 5 - 0 < 20 + t_{DATA\_DELAY}$$
$$t_{CLK\_DELAY} < 15 + t_{DATA\_DELAY}$$

11.2.1.3 Full-Speed Write Combined Formula

The following equation is the combined formula to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

$$t_{CLK\_DELAY} + t_{IH} - t_{SFSKHOX} < t_{SFSCKL} + t_{DATA\_DELAY} < t_{SFSCK} + t_{CLK\_DELAY} - t_{ISU} - t_{SFSKHOV} \quad \textbf{Eqn. 6}$$

11.2.2 Full-Speed Input Path (Read)

This figure provides the data and command input timing diagram.

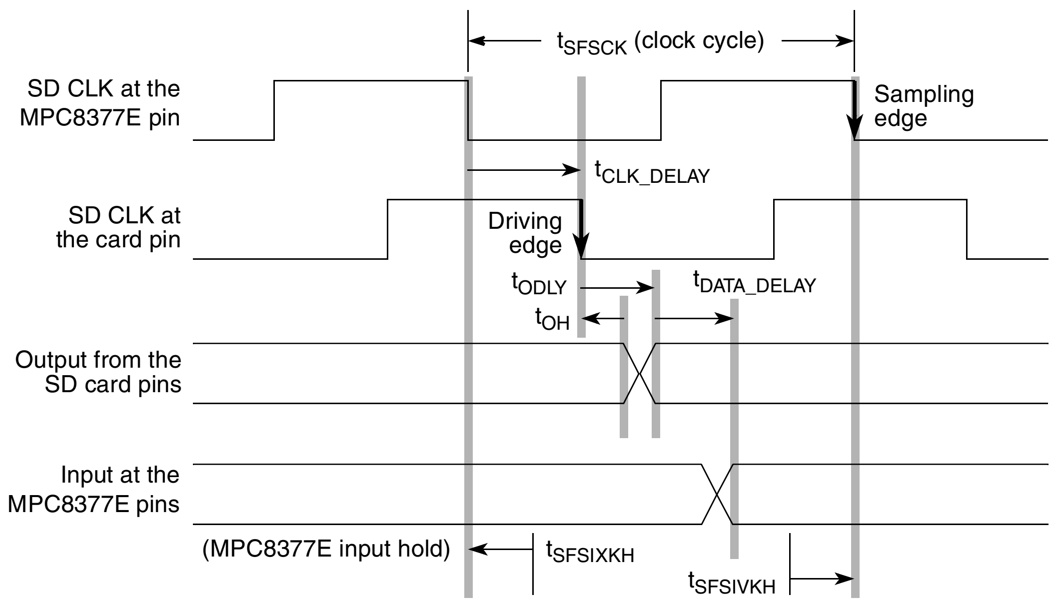

Figure 28. Full Speed Input Path

11.2.2.1 Full-Speed Read Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed combined propagation delay range of the SD_CLK and SD_DAT/CMD signals on the PCB.

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} + t_{ODLY} + t_{SFSIVKH} < t_{SFSCK} \quad \textbf{Eqn. 7}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} < t_{SFSCK} - t_{ODLY} - t_{SFSIVKH} - t_{INT\_CLK\_DLY} \quad \textbf{Eqn. 8}$$

Table 49. PCI AC Timing Specifications at 66 MHz (continued)

PCI_SYNC_IN clock input levels are with next levels: VIL = 0.1 × OV_{DD}, VIH = 0.7 × OV_{DD}.

Parameter	Symbol[1]	Min	Max	Unit	Note
Input hold from cock	t_{PCIXKH}	0.25	—	ns	2, 4, 6
Output clock skew	t_{PCKOSK}	—	0.5	ns	5

Notes:

1. Note that the symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.
5. PCI specifications allows 1 ns skew for 66 MHz but includes the total allowed skew, board, connectors, etc.
6. Value does not comply with the *PCI 2.3 Local Bus Specifications*.

This table shows the PCI AC timing specifications at 33 MHz.

Table 50. PCI AC Timing Specifications at 33 MHz

PCI_SYNC_IN clock input levels are with next levels: VIL = 0.1 × OV_{DD}, V_{IH} = 0.7 × OV_{DD}.

Parameter	Symbol[1]	Min	Max	Unit	Note
Clock to output valid	t_{PCKHOV}	—	11	ns	2
Output hold from clock	t_{PCKHOX}	2	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	3.0	—	ns	2, 4
Input hold from clock	t_{PCIXKH}	0.25	—	ns	2, 4, 6
Output clock skew	t_{PCKOSK}	—	0.5	ns	5

Notes:

1. Note that the symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.
5. PCI specifications allows 2 ns skew for 33 MHz but includes the total allowed skew, board, connectors, etc.
6. Value does not comply with the *PCI 2.3 Local Bus Specifications*.

Table 58. Gen 2i/3G Transmitter AC Specifications (continued)

Parameter	Symbol	Min	Typical	Max	Units	Note
Total jitter $f_{C3dB} = f_{BAUD}/1667$	$U_{SATA\_TXTJfB/1667}$	—	—	0.55	UI_{p-p}	1
Deterministic jitter $f_{C3dB} = f_{BAUD}/10$	$U_{SATA\_TXDJfB/10}$	—	—	0.17	UI_{p-p}	1
Deterministic jitter $f_{C3dB} = f_{BAUD}/500$	$U_{SATA\_TXDJfB/500}$	—	—	0.19	UI_{p-p}	1
Deterministic jitter $f_{C3dB} = f_{BAUD}/1667$	$U_{SATA\_TXDJfB/1667}$	—	—	0.35	UI_{p-p}	1

Note:
1. Measured at Tx output pins peak to peak phase variation, random data pattern.

16.3 Differential Receiver (Rx) Input Characteristics

This section discusses the Gen1i/1.5G and Gen2i/3G differential receiver input AC characteristics.

16.3.1 Gen1i/1.5G Receiver Specifications

This table provides the Gen1i or 1.5 Gbits/s differential receiver input DC characteristics for the SATA interface.

Table 59. Gen1i/1.5G Receiver Input DC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Note
Differential input voltage	V_{SATA_RXDIFF}	240	500	600	mV_{p-p}	1
Differential Rx input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	—

Note:
1. Voltage relative to common of either signal comprising a differential pair.

This table provides the Gen1i or 1.5 Gbits/s differential receiver input AC characteristics for the SATA interface.

Table 60. Gen 1i/1.5G Receiver AC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Note
Unit interval	T_{UI}	666.4333	666.667	670.2333	ps	—
Total jitter, data-data 5 UI	$U_{SATA\_TXTJ5UI}$	—	—	0.43	UI_{p-p}	1
Total jitter, data-data 250 UI	$U_{SATA\_TXTJ250UI}$	—	—	0.60	UI_{p-p}	1
Deterministic jitter, data-data 5 UI	$U_{SATA\_TXDJ5UI}$	—	—	0.25	UI_{p-p}	1

18 GPIO

This section describes the DC and AC electrical specifications for the GPIO of the chip.

18.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for the device GPIO.

Table 65. GPIO DC Electrical Characteristics

This specification applies when operating at 3.3 V ± 165 mV supply.

Parameter	Condition	Symbol	Min	Max	Unit
Output high voltage	I_{OH} = –6.0 mA	V_{OH}	2.4	—	V
Output low voltage	I_{OL} = 6.0 mA	V_{OL}	—	0.5	V
Output low voltage	I_{OL} = 3.2 mA	V_{OL}	—	0.4	V
Input high voltage	—	V_{IH}	2.0	OV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.8	V
Input current	0 V ≤ V_{IN} ≤ OV_{DD}	I_{IN}	—	± 30	μA

18.2 GPIO AC Timing Specifications

This table provides the GPIO input and output AC timing specifications.

Table 66. GPIO Input AC Timing Specifications

Parameter	Symbol	Min	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

This figure provides the AC test load for the GPIO.

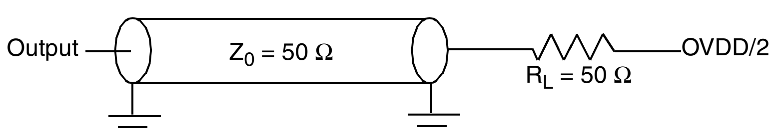

Figure 47. GPIO AC Test Load

19 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins of the chip.

19.1 IPIC DC Electrical Characteristics

This table provides the DC electrical characteristics for the external interrupt pins of the chip.

Table 67. IPIC DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.0	OV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.8	V
Input current	—	I_{IN}	—	±30	μA
Output low voltage	I_{OL} = 6.0 mA	V_{OL}	—	0.5	V
Output low voltage	I_{OL} = 3.2 mA	V_{OL}	—	0.4	V

Note:
1. This table applies for pins $\overline{\text{IRQ}}$[0:7], $\overline{\text{IRQ\_OUT}}$, $\overline{\text{MCP\_OUT}}$.
2. $\overline{\text{IRQ\_OUT}}$ and $\overline{\text{MCP\_OUT}}$ are open drain pins, thus V_{OH} is not relevant for those pins.

19.2 IPIC AC Timing Specifications

This table provides the IPIC input and output AC timing specifications.

Table 68. IPIC Input AC Timing Specifications

Parameter	Symbol	Min	Unit
IPIC inputs—minimum pulse width	t_{PIWID}	20	ns

Note:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.

20 SPI

This section describes the DC and AC electrical specifications for the SPI of the chip.

20.1 SPI DC Electrical Characteristics

This table provides the DC electrical characteristics for the device SPI.

Table 69. SPI DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.0	OV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.8	V
Input current	—	I_{IN}	—	± 30	μA
Output high voltage	I_{OH} = –8.0 mA	V_{OH}	2.4	—	V

21.3 SerDes Transmitter and Receiver Reference Circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.

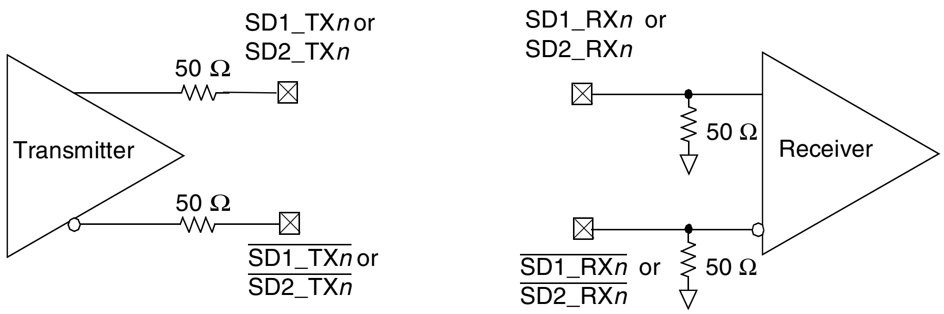

Figure 62. SerDes Transmitter and Receiver Reference Circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below in this document based on the application usage:

- Section 8, "Ethernet: Enhanced Three-Speed Ethernet (eTSEC)"
- Section 15, "PCI Express"
- Section 16, "Serial ATA (SATA)"

Note that an external AC coupling capacitor is required for the above three serial transmission protocols with the capacitor value defined in specification of each protocol section.

22 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions.

22.1 Package Parameters for the MPC8377E TePBGA II

The package parameters are provided in the following list. The package type is 31 mm × 31 mm, 689 plastic ball grid array (TePBGA II).

Package outline	31 mm × 31 mm
Interconnects	689
Pitch	1.00 mm
Module height (typical)	2.0 mm to 2.46 mm (maximum)
Solder Balls	3.5% Ag, 96.5% Sn
Ball diameter (typical)	0.60 mm

This figure shows the mechanical dimensions and bottom surface nomenclature of the TEPBGA II package.

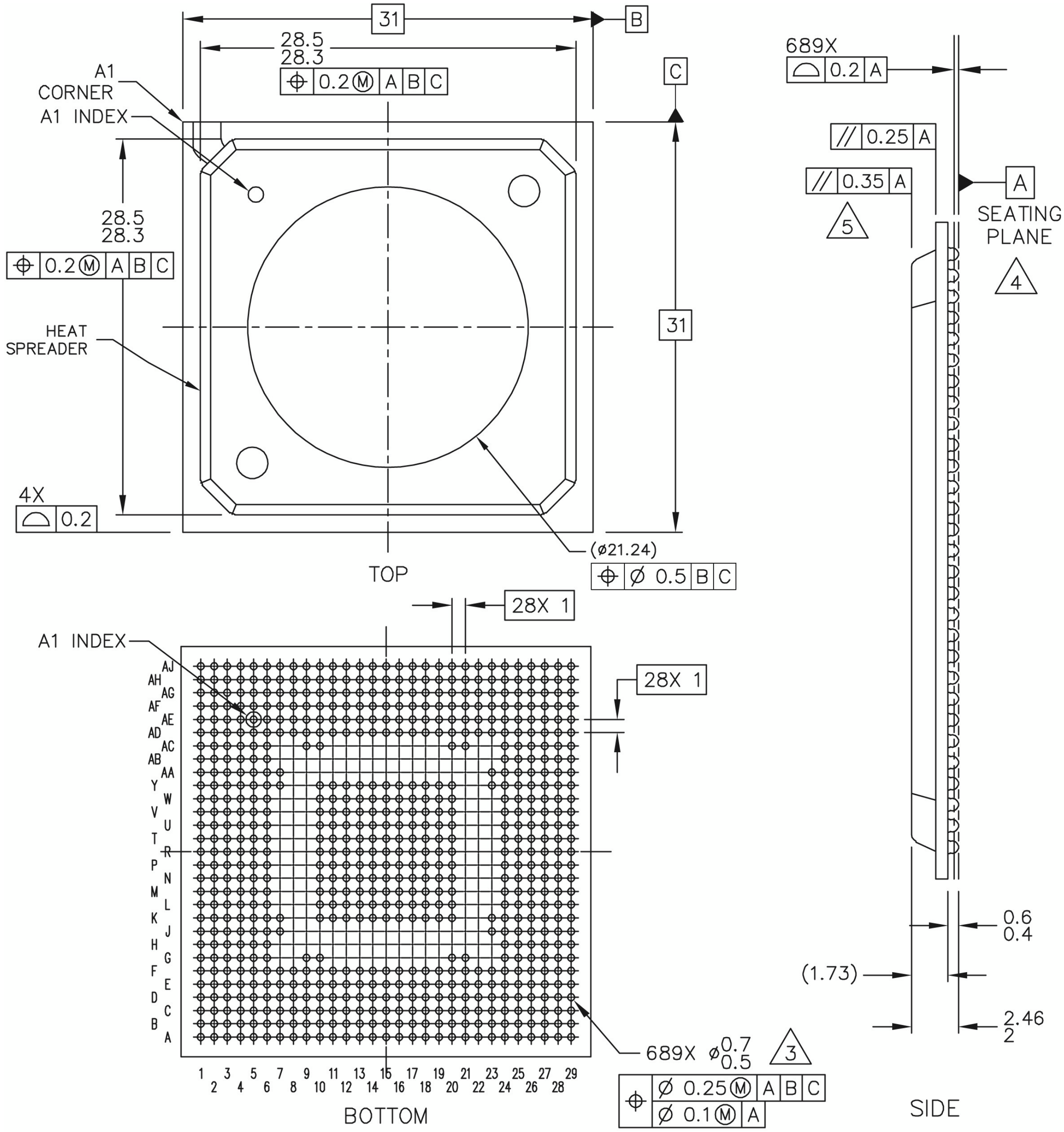

Figure 63. Mechanical Dimensions and Bottom Surface Nomenclature of the TEPBGA II

Note:

1 All dimensions are in millimeters.

2 Dimensioning and tolerancing per ASME Y14. 5M-1994.

3 Maximum solder ball diameter measured parallel to Datum A.

4 Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
MDQS4	AB5	I/O	GVDD	11
MDQS5	AD1	I/O	GVDD	11
MDQS6	AH1	I/O	GVDD	11
MDQS7	AJ3	I/O	GVDD	11
MDQS8	G1	I/O	GVDD	11
MECC0/MSRCID0	J6	I/O	GVDD	—
MECC1/MSRCID1	J3	I/O	GVDD	—
MECC2/MSRCID2	K2	I/O	GVDD	—
MECC3/MSRCID3	K3	I/O	GVDD	—
MECC4/MSRCID4	J5	I/O	GVDD	—
MECC5/MDVAL	J2	I/O	GVDD	—
MECC6	L5	I/O	GVDD	—
MECC7	L2	I/O	GVDD	—
MODT0	N5	O	GVDD	6
MODT1	U6	O	GVDD	6
MODT2	M6	O	GVDD	6
MODT3	P6	O	GVDD	6
MRAS_B	AA3	O	GVDD	—
MVREF1	K4	I	GVDD	11
MVREF2	W4	I	GVDD	11
MWE_B	Y2	O	GVDD	—
DUART Interface				
UART_SIN1/ MSRCID2/LSRCID2	L28	I/O	OVDD	—
UART_SOUT1/ MSRCID0/LSRCID0	L27	O	OVDD	—
UART_CTS_B[1]/ MSRCID4/LSRCID4	K26	I/O	OVDD	—
UART_RTS_B1	N27	O	OVDD	—
UART_SIN2/ MSRCID3/LSRCID3	K27	I/O	OVDD	—
UART_SOUT2/ MSRCID1/LSRCID1	K28	O	OVDD	—
UART_CTS_B[2]/ MDVAL/LDVAL	K29	I/O	OVDD	—

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
UART_RTS_B[2]	L29	O	OVDD	—
Enhanced Local Bus Controller (eLBC) Interface				
LAD0	E24	I/O	LBVDD	—
LAD1	G28	I/O	LBVDD	—
LAD2	H25	I/O	LBVDD	—
LAD3	F26	I/O	LBVDD	—
LAD4	C26	I/O	LBVDD	—
LAD5	J28	I/O	LBVDD	—
LAD6	F21	I/O	LBVDD	—
LAD7	F23	I/O	LBVDD	—
LAD8	E25	I/O	LBVDD	—
LAD9	E26	I/O	LBVDD	—
LAD10	A23	I/O	LBVDD	—
LAD11	F24	I/O	LBVDD	—
LAD12	G24	I/O	LBVDD	—
LAD13	F25	I/O	LBVDD	—
LAD14	H28	I/O	LBVDD	—
LAD15	G25	I/O	LBVDD	—
LA11/LAD16	F27	I/O	LBVDD	—
LA12/LAD17	B21	I/O	LBVDD	—
LA13/LAD18	A25	I/O	LBVDD	—
LA14/LAD19	C28	I/O	LBVDD	—
LA15/LAD20	H24	I/O	LBVDD	—
LA16/LAD21	E23	I/O	LBVDD	—
LA17/LAD22	B28	I/O	LBVDD	—
LA18/LAD23	D28	I/O	LBVDD	—
LA19/LAD24	A27	I/O	LBVDD	—
LA20/LAD25	C25	I/O	LBVDD	—
LA21/LAD26	B27	I/O	LBVDD	—
LA22/LAD27	H27	I/O	LBVDD	—
LA23/LAD28	E21	I/O	LBVDD	—
LA24/LAD29	F20	I/O	LBVDD	—

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
eTSEC1/GPIO1/GPIO2/CFG_RESET Interface				
TSEC1_COL/GPIO2[20]	AF22	I/O	LVDD1	16
TSEC1_CRS/GPIO2[21]	AE20	I/O	LVDD1	16
TSEC1_GTX_CLK	AJ25	O	LVDD1	16
TSEC1_RX_CLK	AG22	I	LVDD1	16
TSEC1_RX_DV	AD19	I	LVDD1	16
TSEC1_RX_ER/GPIO2[25]	AD20	I/O	LVDD1	16
TSEC1_RXD0	AD22	I	LVDD1	16
TSEC1_RXD1	AE21	I	LVDD1	16
TSEC1_RXD2	AE22	I	LVDD1	16
TSEC1_RXD3	AD21	I	LVDD1	16
TSEC1_TX_CLK	AJ22	I	LVDD1	16
TSEC1_TX_EN	AG23	O	LVDD1	16
TSEC1_TX_ER/CFG_LBMUX	AH22	I/O	LVDD1	16
TSEC1_TXD0/ CFG_RESET_SOURCE[0]	AD23	I/O	LVDD1	16
TSEC1_TXD1/ CFG_RESET_SOURCE[1]	AE23	I/O	LVDD1	16
TSEC1_TXD2/ CFG_RESET_SOURCE[2]	AF23	I/O	LVDD1	16
TSEC1_TXD3/ CFG_RESET_SOURCE[3]	AJ24	I/O	LVDD1	16
EC_GTX_CLK125	AH24	I	LVDD1	16
EC_MDC/CFG_CLKIN_DIV	AJ21	I/O	LVDD1	16
EC_MDIO	AH21	I/O	LVDD1	16
eTSEC2/GPIO1 Interface				
TSEC2_COL/GPIO1[21]/ TSEC1_TMR_TRIG1	AJ27	I/O	LVDD2	16
TSEC2_CRS/GPIO1[22]/ TSEC1_TMR_TRIG2	AG29	I/O	LVDD2	16
TSEC2_GTX_CLK	AF28	O	LVDD2	16
TSEC2_RX_CLK/ TSEC1_TMR_CLK	AF25	I	LVDD2	16
TSEC2_RX_DV/GPIO1[23]	AF26	I/O	LVDD2	16
TSEC2_RX_ER/GPIO1[25]	AG25	I/O	LVDD2	16

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
TSEC2_RXD0/GPIO1[16]	AE28	I/O	LVDD2	16
TSEC2_RXD1/GPIO1[15]	AE29	I/O	LVDD2	16
TSEC2_RXD2/GPIO1[14]	AH26	I/O	LVDD2	16
TSEC2_RXD3/GPIO1[13]	AH25	I/O	LVDD2	16
TSEC2_TX_CLK/GPIO2[24]/ TSEC1_TMR_GCLK	AG28	I/O	LVDD2	16
TSEC2_TX_EN/GPIO1[12]/ TSEC1_TMR_ALARM2	AJ26	I/O	LVDD2	16
TSEC2_TX_ER/GPIO1[24]/ TSEC1_TMR_ALARM1	AG26	I/O	LVDD2	16
TSEC2_TXD0/GPIO1[20]	AH28	I/O	LVDD2	16
TSEC2_TXD1/GPIO1[19]/ TSEC1_TMR_PP1	AF27	I/O	LVDD2	16
TSEC2_TXD2/GPIO1[18]/ TSEC1_TMR_PP2	AJ28	I/O	LVDD2	16
TSEC2_TXD3/GPIO1[17]/ TSEC1_TMR_PP3	AF29	I/O	LVDD2	16
GPIO1 Interface				
GPIO1[0]/GTM1_TIN1/ GTM2_TIN2/DREQ0_B	P25	I/O	OVDD	—
GPIO1[1]/GTM1_TGATE1_B/ GTM2_TGATE2_B/DACK0_B	N25	I/O	OVDD	—
GPIO1[2]/GTM1_TOUT1_B/ DDONE0_B	N26	I/O	OVDD	—
GPIO1[3]/GTM1_TIN2/ GTM2_TIN1/DREQ1_B	B9	I/O	OVDD	—
GPIO1[4]/GTM1_TGATE2_B/ GTM2_TGATE1_B/DACK1_B	N29	I/O	OVDD	—
GPIO1[5]/GTM1_TOUT2_B/ GTM2_TOUT1_B/DDONE1_B	M29	I/O	OVDD	—
GPIO1[6]/GTM1_TIN3/ GTM2_TIN4/DREQ2_B	A9	I/O	OVDD	—
GPIO1[7]/GTM1_TGATE3_B/ GTM2_TGATE4_B/DACK2_B	B10	I/O	OVDD	—
GPIO1[8]/GTM1_TOUT3_B/ DDONE2_B	J26	I/O	OVDD	—
GPIO1[9]/GTM1_TIN4/ GTM2_TIN3/DREQ3_B	J24	I/O	OVDD	—

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
SPIMISO/SD_DAT0	AD11	I/O	OVDD	—
SPIMOSI/SD_CMD	AJ9	I/O	OVDD	—
SPISEL_B/SD_CD	AE11	I	OVDD	—
System Control Interface				
SRESET_B	AD12	I/O	OVDD	2
HRESET_B	AE12	I/O	OVDD	1
PORESET_B	AE14	I	OVDD	—
Test Interface				
TEST	E10	I	OVDD	10
TEST_SEL0	D10	I	OVDD	13
TEST_SEL1	D12	I	OVDD	13
Thermal Management				
Reserved	F15	I	—	14
Power Supply Signals				
LVDD1	AC21, AG21, AH23	Power for eTSEC 1 I/O (2.5 V, 3.3 V)	LVDD1	—
LVDD2	AG24, AH27, AH29	Power for eTSEC 2 I/O (2.5 V, 3.3 V)	LVDD2	—
LBVDD	G20, D22, A24, G26, D27, A28	Power for eLBC (3.3, 2.5, or 1.8 V)	LBVDD	—
VDD	K10, L10, M10, N10, P10, R10, T10, U10, V10, W10, Y10, K11, R11, Y11, K12, Y12, K13, Y13, K14, Y14, K15, L15, W15, Y15, K16, Y16, K17, Y17, K18, Y18, K19, R19, Y19, K20, L20, M20, N20, P20, R20, T20, U20, V20, W20, Y20	Power for Core (1.0 V or 1.5 V)	VDD	—