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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	-
Number of Cores/Bus Width	-
Speed	-
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	-
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	-
Operating Temperature	-
Security Features	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8377cvralga

In addition to the security engine, new high-speed interfaces, such as PCI Express and SATA are included. This table compares the differences between MPC837xE derivatives and provides the number of ports available for each interface.

Table 1. High-Speed Interfaces on the MPC8377E, MPC8378E, and MPC8379E

Descriptions	MPC8377E	MPC8378E	MPC8379E
SGMII	0	2	0
PCI Express®	2	2	0
SATA	2	0	4

1.1 DDR Memory Controller

The DDR1/DDR2 memory controller includes the following features:

- Single 32- or 64-bit interface supporting both DDR1 and DDR2 SDRAM
- Support for up to 400-MHz data rate
- Support up to 4 chip selects
- 64-Mbit to 2-Gbit (for DDR1) and to 4-Gbit (for DDR2) devices with ×8/×16/×32 data ports (no direct ×4 support)
- Support for up to 32 simultaneous open pages
- Supports auto refresh
- On-the-fly power management using CKE
- 1.8-/2.5-V SSTL2 compatible I/O

1.2 USB Dual-Role Controller

The USB controller includes the following features:

- Supports USB on-the-go mode, including both device and host functionality, when using an external ULPI (UTMI + low-pin interface) PHY
- Complies with *USB Specification, Rev. 2.0*
- Supports operation as a stand-alone USB device
  - Supports one upstream facing port
  - Supports three programmable USB endpoints
- Supports operation as a stand-alone USB host controller
  - Supports USB root hub with one downstream-facing port
  - Enhanced host controller interface (EHCI) compatible
- Supports high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operation; low-speed operation is supported only in host mode
- Supports UTMI + low pin interface (ULPI)

voltage supplies—GV_{DD}, LV_{DD}, and OV_{DD}—do not have any ordering requirements with respect to one another.

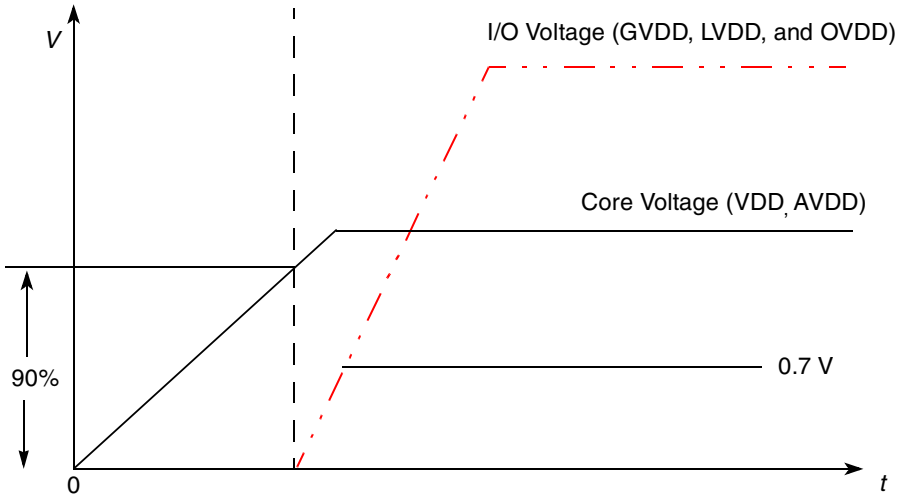

Figure 3. Power-Up Sequencing Example

Note that the SerDes power supply (L[1,2]_$n$$V_{DD}$) should follow the same timing as the core supply (V_{DD}).

The device does not require the core supply voltage and I/O supply voltages to be powered down in any particular order.

3 Power Characteristics

The estimated typical power dissipation for the chip device is shown in this table.

Table 5. Power Dissipation [1]

Core Frequency (MHz)	CSB/DDR Frequency (MHz)	Sleep Power at T_j = 65°C (W) [2]	Typical Application at T_j = 65°C (W) [2]	Typical Application at T_j = 125°C (W) [3]	Max Application at T_j = 125°C (W) [4]
333	333	1.45	1.9	3.2	3.8
	167	1.45	1.8	3.0	3.6
400	400	1.45	2.0	3.3	4.0
	266	1.45	1.9	3.1	3.8
450	300	1.45	2.0	3.2	3.8
	225	1.45	1.9	3.1	3.7
500	333	1.45	2.0	3.3	3.9
	250	1.45	1.9	3.2	3.8
533	355	1.45	2.0	3.3	4.0
	266	1.45	2.0	3.2	3.9

4.3 eTSEC Gigabit Reference Clock Timing

This table provides the eTSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications.

Table 9. EC_GTX_CLK125 AC Timing Specifications

At recommended operating conditions with LV_{DD} = 2.5 ± 0.125 mV/ 3.3 V ± 165 mV

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Note
EC_GTX_CLK125 frequency	t_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC_GTX_CLK rise and fall time LV_{DD} = 2.5 V LV_{DD} = 3.3 V	t_{G125R}/t_{G125F}	—	—	 0.75 1.0	ns	1
EC_GTX_CLK125 duty cycle 1000Base-T for RGMII, RTBI	t_{G125H}/t_{G125}	 47	—	 53	%	2
EC_GTX_CLK125 jitter	—	—	—	±150	ps	2

Notes:

1. Rise and fall times for EC_GTX_CLK125 are measured from 0.5 and 2.0 V for LV_{DD} = 2.5 V and from 0.6 and 2.7 V for LV_{DD} = 3.3 V.
2. EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. The EC_GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 8.2.2, "RGMII and RTBI AC Timing Specifications," for the duty cycle for 10Base-T and 100Base-T reference clock.

5 RESET Initialization

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the chip.

5.1 RESET DC Electrical Characteristics

This table provides the DC electrical characteristics for the RESET pins of the device.

Table 10. RESET Pins DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	± 30	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

Notes:

- This table applies for pins $\overline{\text{PORESET}}$ and $\overline{\text{HRESET}}$. The $\overline{\text{PORESET}}$ is input pin, thus stated output voltages are not relevant.
- $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are open drain pin, thus V_{OH} is not relevant for these pins.

6.1 DDR1 and DDR2 SDRAM DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR2 SDRAM component(s) of the device when GV_{DD}(typ) = 1.8 V.

Table 13. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Parameter	Symbol	Min	Max	Unit	Note
I/O supply voltage	GV_{DD}	1.71	1.89	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2, 5
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF} + 0.140	GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.140	V	—
Output leakage current	I_{OZ}	–50	50	μA	4
Output high current (V_{OUT} = 1.40 V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.3 V)	I_{OL}	13.4	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.
5. See AN3665, “MPC837xE Design Checklist,” for proper DDR termination.

Table 14 provides the DDR2 capacitance when GV_{DD}(typ) = 1.8 V.

Table 14. DDR2 SDRAM Capacitance for GV_{DD}(typ) = 1.8 V

Parameter	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the recommended operating conditions for the DDR SDRAM component(s) when GV_{DD}(typ) = 2.5 V.

Table 15. DDR SDRAM DC Electrical Characteristics for GV_{DD} (typ) = 2.5 V

Parameter	Symbol	Min	Max	Unit	Note
I/O supply voltage	GV_{DD}	2.375	2.625	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2, 5
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF} + 0.18	GV_{DD} + 0.3	V	—

8.1.1 MII, RMII, RGMII, and RTBI DC Electrical Characteristics

MII and RMII drivers and receivers comply with the DC parametric attributes specified in Table 24 and Table 25. The RGMII and RTBI signals in Table 25 are based on a 2.5 V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 24. MII and RMII DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage 3.3 V	LV_{DD1} LV_{DD2}	3.13	3.47	V	1
Output high voltage (LV_{DD1}/LV_{DD2} = Min, I_{OH} = –4.0 mA)	V_{OH}	2.40	LV_{DD1}/LV_{DD2} + 0.3	V	—
Output low voltage (LV_{DD1}/LV_{DD2} = Min, I_{OL} = 4.0 mA)	V_{OL}	GND	0.50	V	—
Input high voltage	V_{IH}	2.0	LV_{DD1}/LV_{DD2} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	0.90	V	—
Input high current (V_{IN} = LV_{DD1}, V_{IN} = LV_{DD2})	I_{IH}	—	30	µA	1
Input low current (V_{IN} = GND)	I_{IL}	–600	—	µA	—

Notes:
1. LV_{DD1} supports eTSEC 1. LV_{DD2} supports eTSEC 2.

Table 25. RGMII and RTBI DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage 2.5 V	LV_{DD1} LV_{DD2}	2.37	2.63	V	1
Output high voltage (LV_{DD1}/LV_{DD2} = Min, IOH = –1.0 mA)	V_{OH}	2.00	LV_{DD1}/LV_{DD2} + 0.3	V	—
Output low voltage (LV_{DD1}/LV_{DD2} = Min, I_{OL} = 1.0 mA)	V_{OL}	GND – 0.3	0.40	V	—
Input high voltage	V_{IH}	1.7	LV_{DD1}/LV_{DD2} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	0.70	V	—
Input high current (V_{IN} = LV_{DD1}, V_{IN} = LV_{DD2})	I_{IH}	—	–20	µA	1
Input low current (V_{IN} = GND)	I_{IL}	–20	—	µA	—

Notes:
1. LV_{DD1} supports eTSEC 1. LV_{DD2} supports eTSEC 2.

10 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the chip.

10.1 Local Bus DC Electrical Characteristics

This tables provide the DC electrical characteristics for the local bus interface.

Table 36. Local Bus DC Electrical Characteristics (LBV_{DD} = 3.3 V)

At recommended operating conditions with LBV_{DD} = 3.3 V.

Parameter	Conditions		Symbol	Min	Max	Unit
Supply voltage 3.3 V	—		LBV_{DD}	3.135	3.465	V
Output high voltage	I_{OH} = –4.0 mA	LBV_{DD} = Min	V_{OH}	2.40	—	V
Output low voltage	I_{OL} = 4.0 mA	LBV_{DD} = Min	V_{OL}	—	0.50	V
Input high voltage	—	—	V_{IH}	2.0	LBV_{DD} + 0.3	V
Input low voltage	—	—	V_{IL}	–0.3	0.90	V
Input high current	V_{IN} [1] = LBV_{DD}		I_{IH}	—	30	μA
Input low current	V_{IN} [1] = GND		I_{IL}	–30	—	μA

Table 37. Local Bus DC Electrical Characteristics (LBV_{DD} = 2.5 V)

At recommended operating conditions with LBV_{DD} = 2.5 V.

Parameter	Conditions		Symbol	Min	Max	Unit
Supply voltage 2.5 V	—		LBV_{DD}	2.37	2.73	V
Output high voltage	I_{OH} = –1.0 mA	LBV_{DD} = Min	V_{OH}	2.00	—	V
Output low voltage	I_{OL} = 1.0 mA	LBV_{DD} = Min	V_{OL}	—	0.40	V
Input high voltage	—	LBV_{DD} = Min	V_{IH}	1.7	LBV_{DD} + 0.3	V
Input low voltage	—	LBV_{DD} = Min	V_{IL}	–0.3	0.70	V
Input high current	V_{IN} [1] = LBV_{DD}		I_{IH}	—	20	μA
Input low current	V_{IN} [1] = GND		I_{IL}	–20	—	μA

Table 38. Local Bus DC Electrical Characteristics (LBV_{DD} = 1.8 V)

At recommended operating conditions with LBV_{DD} = 1.8 V.

Parameter	Conditions		Symbol	Min	Max	Unit
Supply voltage 1.8 V	—		LBV_{DD}	1.71	1.89	V
Output high voltage	I_{OH} = –1.0 mA	LBV_{DD} = Min	V_{OH}	LBV_{DD} – 0.45	—	V
Output low voltage	I_{OL} = 1.0 mA	LBV_{DD} = Min	V_{OL}	—	0.45	V
Input high voltage	—	LBV_{DD} = Min	V_{IH}	0.65 × LBV_{DD}	LBV_{DD} + 0.3	V
Input low voltage	—	LBV_{DD} = Min	V_{IL}	–0.3	0.35 × LBV_{DD}	V
Input high current	V_{IN} [1] = LBV_{DD}		I_{IH}	—	10	μA
Input low current	V_{IN} [1] = GND		I_{IL}	–10	—	μA

10.2 Local Bus AC Electrical Specifications

This table describes the general timing parameters of the local bus interface of the device when in PLL enable mode.

Table 39. Local Bus General Timing Parameters—PLL Enable Mode

Parameter	Symbol[1]	Min	Max	Unit	Note
Local bus cycle time	t_{LBK}	7.5	15	ns	2
Input setup to local bus clock (except LUPWAIT/$\overline{\text{LGTA}}$)	t_{LBIVKH}	1.5	—	ns	3, 4
Input hold from local bus clock	t_{LBIXKH}	1.0	—	ns	3, 4
LUPWAIT/$\overline{\text{LGTA}}$ input setup to local bus clock	$t_{LBIVKH1}$	1.5	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7
Local bus clock to LALE rise	t_{LBKHLR}	—	4.5	ns	—
Local bus clock to output valid (except LALE)	t_{LBKHOV}	—	4.5	ns	3

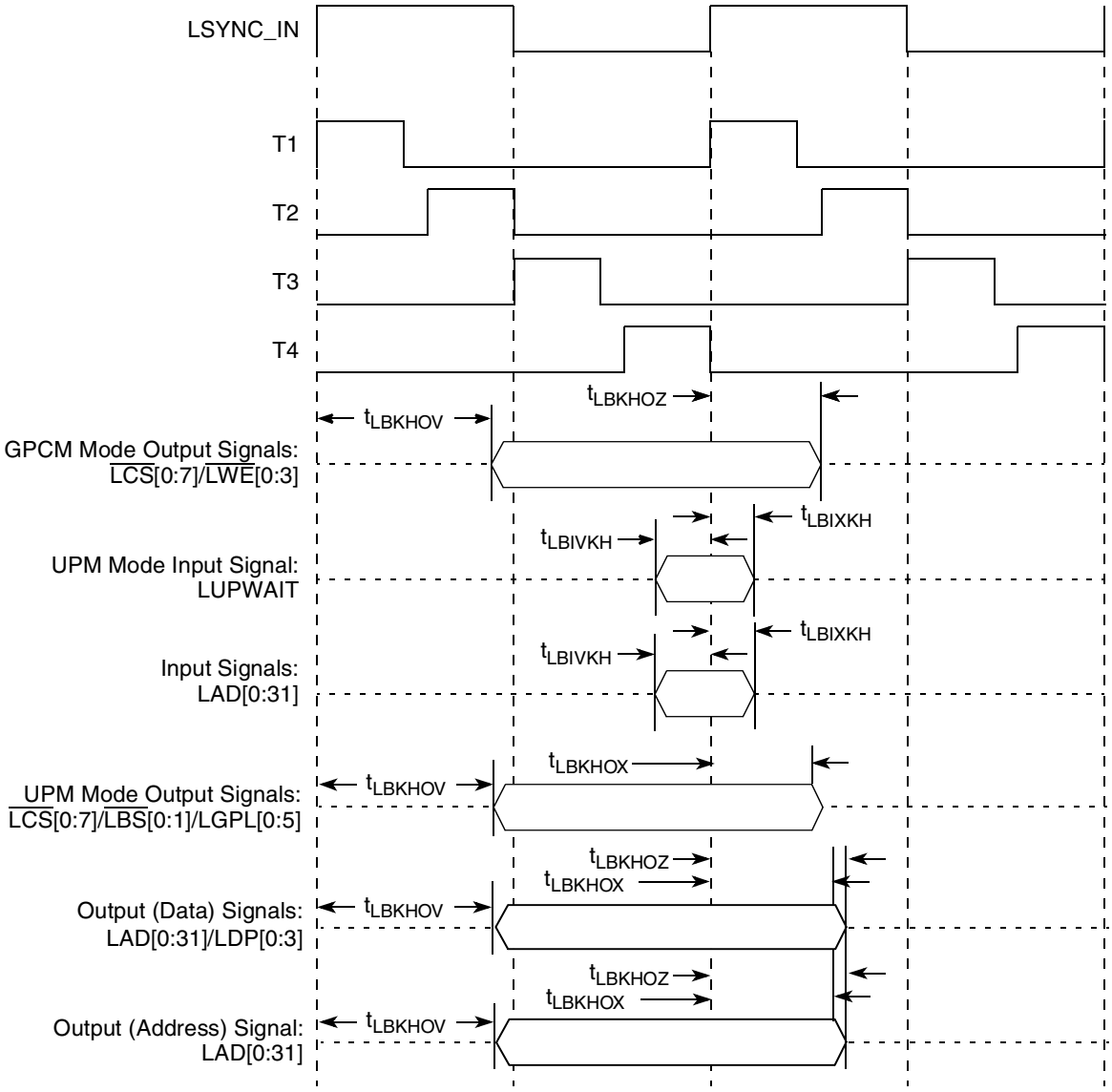

Figure 24. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 (PLL Enable Mode)

11.2.2.2 Full-Speed Read Meeting Hold (Minimum Delay)

There is no minimum delay constraint due to the full clock cycle between the driving and sampling of data.

$$t_{CLK\_DELAY} + t_{OH} + t_{DATA\_DELAY} > t_{SFSIXKH} \quad \textit{Eqn. 9}$$

This means that Data + Clock delay must be greater than –2 ns. This is always fulfilled.

11.3 eSDHC AC Timing Specifications (High-Speed Mode)

This table provides the eSDHC AC timing specifications for high-speed mode as defined in Figure 30 and Figure 31.

Table 43. eSDHC AC Timing Specifications for High-Speed Mode

At recommended operating conditions OV_{DD} = 3.3 V ± 165 mV.

Parameter	Symbol[1]	Min	Max	Unit	Note
SD_CLK clock frequency—high speed mode	f_{SHSCK}	0	50	MHz	—
SD_CLK clock cycle	t_{SHSCK}	20	—	ns	—
SD_CLK clock frequency—identification mode	f_{SIDCK}	0	400	KHz	—
SD_CLK clock low time	t_{SHSCKL}	7	—	ns	2
SD_CLK clock high time	t_{SHSCKH}	7	—	ns	2
SD_CLK clock rise and fall times	t_{SHSCKR}/ t_{SHSCKF}	—	3	ns	2
Input setup times: SD_CMD, SD_DATx, SD_CD to SD_CLK	$t_{SHSIVKH}$	5	—	ns	2
Input hold times: SD_CMD, SD_DATx, SD_CD to SD_CLK	$t_{SHSIXKH}$	0	—	ns	2
Output delay time: SD_CLK to SD_CMD, SD_DATx valid	$t_{SHSKHOV}$	—	4	ns	2
Output Hold time: SD_CLK to SD_CMD, SD_DATx invalid	$t_{SHSKHOX}$	0	—	ns	2
SD_CLK delay within device	$t_{INT\_CLK\_DLY}$	1.5	—	ns	4
SD Card Input Setup	t_{ISU}	6	—	ns	3
SD Card Input Hold	t_{IH}	2	—	ns	3
SD Card Output Valid	t_{ODLY}	—	14	ns	3
SD Card Output Hold	t_{OH}	2.5	—	ns	3

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first three letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{SFSIXKH}$ symbolizes eSDHC full mode speed device timing (SFS) input (I) to go invalid (X) with respect to the clock reference (K) going to high (H). Also $t_{SFSKHOV}$ symbolizes eSDHC full speed timing (SFS) for the clock reference (K) to go high (H), with respect to the output (O) going valid (V) or data output valid time. Note that, in general, the clock reference symbol representation is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Measured at capacitive load of 40 pF.
3. For reference only, according to the SD card specifications.
4. Average, for reference only.

Table 52. Differential Transmitter (Tx) Output Specifications (continued)

Parameter	Conditions	Symbol	Min	Typical	Max	Units	Note
Common mode return loss	Measured over 50 MHz to 1.25 GHz.	RL_{TX-CM}	6	—	—	dB	4
DC differential Tx impedance	Tx DC differential mode low impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	—
Transmitter DC impedance	Required Tx D+ as well as D– DC impedance during all states	Z_{TX-DC}	40	—	—	Ω	—
Lane-to-Lane output skew	Static skew between any two transmitter lanes within a single link	$L_{TX-SKEW}$	—	—	500 + 2 UI	ps	—
AC coupling capacitor	All transmitters should be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.	C_{TX}	75	—	200	nF	—
Crosslink random timeout	This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one downstream and one upstream port.	$T_{crosslink}$	0	—	1	ms	7

Notes:
1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 44 and measured over any 250 consecutive Tx UIs. (Also refer to the transmitter compliance eye diagram shown in Figure 42.)
3. A T_{TX-EYE} = 0.70 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.30 UI for the transmitter collected over any 250 consecutive Tx UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total Tx jitter budget collected over any 250 consecutive Tx UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The transmitter input impedance will result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes, see Figure 44). Note that the series capacitors, C_{TX}, is optional for the return loss measurement.
5. Measured between 20%–80% at transmitter package pins into a test load as shown in Figure 44 for both V_{TX-D+} and V_{TX-D-}.
6. See Section 4.3.1.8 of the *PCI Express Base Specifications*, Rev 1.0a.
7. See Section 4.2.6.3 of the *PCI Express Base Specifications*, Rev 1.0a.

15.4.2 Transmitter Compliance Eye Diagrams

The Tx eye diagram in Figure 42 is specified using the passive compliance/test measurement load (see Figure 44) in place of any real PCI Express interconnect + Rx component. There are two eye diagrams that must be met for the transmitter. Both diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams differ in voltage depending on whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit is always relative to the transition bit.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI.

NOTE

It is recommended that the recovered Tx UI be calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (that is, least squares and median deviation fits).

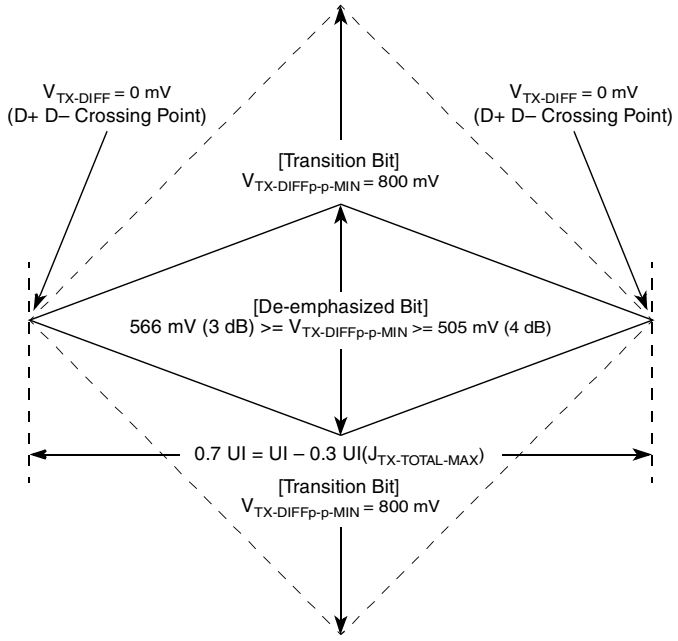

Figure 42. Minimum Transmitter Timing and Voltage Output Compliance Specifications

15.4.3 Differential Receiver (Rx) Input Specifications

This table defines the specifications for the differential input at all receivers. The parameters are specified at the component pins.

Table 53. Differential Receiver (Rx) Input Specifications

Parameter	Comments	Symbol	Min	Typical	Max	Units	Note
Unit interval	Each U_{PERX} is 400 ps ± 300 ppm. U_{PERX} does not account for Spread Spectrum Clock dictated variations.	UI	399.88	400	400.12	ps	1
Differential peak-to-peak output voltage	$V_{PEDPPRX} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$	$V_{RX-DIFFp-p}$	0.175	—	1.200	V	2

Table 60. Gen 1i/1.5G Receiver AC Specifications (continued)

Parameter	Symbol	Min	Typical	Max	Units	Note
Deterministic jitter, data-data 250 UI	$U_{SATA\_TXDJ250UI}$	—	—	0.35	UI_{p-p}	1

Note:
1. Measured at Tx output pins peak to peak phase variation, random data pattern.

16.3.2 Gen2i/3G Receiver (Rx) Specifications

This table provides the Gen2i or 3 Gbits/s differential receiver input DC characteristics for the SATA interface.

Table 61. Gen2i/3G Receiver Input DC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Note
Differential input voltage	V_{SATA_RXDIFF}	275	500	750	mVp-p	1
Differential RX input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	—

Note:
1. Voltage relative to common of either signal comprising a differential pair.

This table provides the differential receiver output AC characteristics for the SATA interface at Gen2i or 3.0 Gbits/s transmission.

Table 62. Gen 2i/3G Receiver AC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Note
Channel Speed	t_{CH_SPEED}	—	3.0	—	Gbps	—
Unit Interval	T_{UI}	333.2	333.33	335.11	ps	—
Total jitter $f_{C3dB} = f_{BAUD}/10$	$U_{SATA\_TXTJfB/10}$	—	—	0.46	UI_{p-p}	1
Total jitter $f_{C3dB} = f_{BAUD}/500$	$U_{SATA\_TXTJfB/500}$	—	—	0.60	UI_{p-p}	1
Total jitter $f_{C3dB} = f_{BAUD}/1667$	$U_{SATA\_TXTJfB/1667}$	—	—	0.65	UI_{p-p}	1
Deterministic jitter $f_{C3dB} = f_{BAUD}/10$	$U_{SATA\_TXDJfB/10}$	—	—	0.35	UI_{p-p}	1
Deterministic jitter $f_{C3dB} = f_{BAUD}/500$	$U_{SATA\_TXDJfB/500}$	—	—	0.42	UI_{p-p}	1
Deterministic jitter $f_{C3dB} = f_{BAUD}/1667$	$U_{SATA\_TXDJfB/1667}$	—	—	0.35	UI_{p-p}	1

Note:
1. Measured at Tx output pins peak to peak phase variation, random data pattern.

19.1 IPIC DC Electrical Characteristics

This table provides the DC electrical characteristics for the external interrupt pins of the chip.

Table 67. IPIC DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.0	OV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.8	V
Input current	—	I_{IN}	—	±30	μA
Output low voltage	I_{OL} = 6.0 mA	V_{OL}	—	0.5	V
Output low voltage	I_{OL} = 3.2 mA	V_{OL}	—	0.4	V

Note:
1. This table applies for pins $\overline{\text{IRQ}}$[0:7], $\overline{\text{IRQ\_OUT}}$, $\overline{\text{MCP\_OUT}}$.
2. $\overline{\text{IRQ\_OUT}}$ and $\overline{\text{MCP\_OUT}}$ are open drain pins, thus V_{OH} is not relevant for those pins.

19.2 IPIC AC Timing Specifications

This table provides the IPIC input and output AC timing specifications.

Table 68. IPIC Input AC Timing Specifications

Parameter	Symbol	Min	Unit
IPIC inputs—minimum pulse width	t_{PIWID}	20	ns

Note:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.

20 SPI

This section describes the DC and AC electrical specifications for the SPI of the chip.

20.1 SPI DC Electrical Characteristics

This table provides the DC electrical characteristics for the device SPI.

Table 69. SPI DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.0	OV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.8	V
Input current	—	I_{IN}	—	± 30	μA
Output high voltage	I_{OH} = –8.0 mA	V_{OH}	2.4	—	V

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
UART_RTS_B[2]	L29	O	OVDD	—
Enhanced Local Bus Controller (eLBC) Interface				
LAD0	E24	I/O	LBVDD	—
LAD1	G28	I/O	LBVDD	—
LAD2	H25	I/O	LBVDD	—
LAD3	F26	I/O	LBVDD	—
LAD4	C26	I/O	LBVDD	—
LAD5	J28	I/O	LBVDD	—
LAD6	F21	I/O	LBVDD	—
LAD7	F23	I/O	LBVDD	—
LAD8	E25	I/O	LBVDD	—
LAD9	E26	I/O	LBVDD	—
LAD10	A23	I/O	LBVDD	—
LAD11	F24	I/O	LBVDD	—
LAD12	G24	I/O	LBVDD	—
LAD13	F25	I/O	LBVDD	—
LAD14	H28	I/O	LBVDD	—
LAD15	G25	I/O	LBVDD	—
LA11/LAD16	F27	I/O	LBVDD	—
LA12/LAD17	B21	I/O	LBVDD	—
LA13/LAD18	A25	I/O	LBVDD	—
LA14/LAD19	C28	I/O	LBVDD	—
LA15/LAD20	H24	I/O	LBVDD	—
LA16/LAD21	E23	I/O	LBVDD	—
LA17/LAD22	B28	I/O	LBVDD	—
LA18/LAD23	D28	I/O	LBVDD	—
LA19/LAD24	A27	I/O	LBVDD	—
LA20/LAD25	C25	I/O	LBVDD	—
LA21/LAD26	B27	I/O	LBVDD	—
LA22/LAD27	H27	I/O	LBVDD	—
LA23/LAD28	E21	I/O	LBVDD	—
LA24/LAD29	F20	I/O	LBVDD	—

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
L1_XCOREVSS	AG14, AG15, AG16, AH16, AG18, AG20	SerDes Core GND	—	—
L1_XPADVDD	AE16, AF16, AD18, AE19, AF19	SerDes I/O Power (1.0 or 1.05 V)	—	—
L1_XPADVSS	AF14, AE17, AF20	SerDes I/O GND	—	—
SerDes2 Interface				
L2_SD_IMP_CAL_RX	C19	I	L2_XPADVDD	—
L2_SD_IMP_CAL_TX	C15	I	L2_XPADVDD	—
L2_SD_REF_CLK	B17	I	L2_XPADVDD	—
L2_SD_REF_CLK_B	A17	I	L2_XPADVDD	—
L2_SD_RXA_N	A19	I	L2_XPADVDD	—
L2_SD_RXA_P	B19	I	L2_XPADVDD	—
L2_SD_RXE_N	A15	I	L2_XPADVDD	—
L2_SD_RXE_P	B15	I	L2_XPADVDD	—
L2_SD_TXA_N	D18	O	L2_XPADVDD	—
L2_SD_TXA_P	E18	O	L2_XPADVDD	—
L2_SD_TXE_N	D15	O	L2_XPADVDD	—
L2_SD_TXE_P	E15	O	L2_XPADVDD	—
L2_SDAVDD_0	A16	SerDes PLL Power (1.0 or 1.05 V)	—	—
L2_SDAVSS_0	C17	SerDes PLL GND	—	—
L2_XCOREVDD	A14, B14, D17, B18, B20	SerDes Core Power (1.0 or 1.05 V)	—	—
L2_XCOREVSS	C14, C16, A18, C18, A20, C20	SerDes Core GND	—	—
L2_XPADVDD	D14, E16, F18, D19, E19	SerDes I/O Power (1.0 or 1.05 V)	—	—
L2_XPADVSS	D16, E17, D20	SerDes I/O GND	—	—
SPI Interface				
SPICLK/SD_CLK	AH9	I/O	OVDD	—

As shown in Figure 64, the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create the coherent system bus clock (*csb_clk*), the internal clock for the DDR controller (*ddr_clk*), and the internal clock for the local bus interface unit (*lbiu_clk*).

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb\_clk = \{PCI\_SYNC\_IN \times (1 + CFG\_CLKIN\_DIV)\} \times SPMF \qquad \text{Eqn. 20}$$

In PCI host mode, PCI_SYNC_IN × (1 + CFG_CLKIN_DIV) is the CLKIN frequency.

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the e300 core multiplies up the *csb_clk* frequency to create the internal clock for the e300 core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low register (RCWLR) which is loaded at power-on reset or by one of the hard-coded reset options. See Chapter 4, "Reset, Clocking, and Initialization," in the *MPC8379E Reference Manual* for more information on the clock subsystem.

The internal *ddr_clk* frequency is determined by the following equation:

$$ddr\_clk = csb\_clk \times (1 + RCWLR[DDRCM]) \qquad \text{Eqn. 21}$$

Note that *ddr_clk* is not the external memory bus frequency; *ddr_clk* passes through the DDR clock divider (÷2) to create the differential DDR memory bus clock outputs (MCK and $\overline{\text{MCK}}$). However, the data rate is the same frequency as *ddr_clk*.

The internal *lbiu_clk* frequency is determined by the following equation:

$$lbiu\_clk = csb\_clk \times (1 + RCWLR[LBCM]) \qquad \text{Eqn. 22}$$

Note that *lbiu_clk* is not the external local bus frequency; *lbiu_clk* passes through the LBIU clock divider to create the external local bus clock outputs (LCLK[0:2]). The eLBC clock divider ratio is controlled by LCRR[CLKDIV].

Some of the internal units may be required to be shut off or operate at lower frequency than the *csb_clk* frequency. Those units have a default clock ratio that can be configured by a memory mapped register after the device comes out of reset. Table 73 specifies which units have a configurable clock frequency.

Table 73. Configurable Clock Units

Unit	Default Frequency	Options
eTSEC1, eTSEC2	csb_clk/3	Off, *csb_clk, csb_clk/2, csb_clk/3*
eSDHC and I^2C1[1]	csb_clk/3	Off, *csb_clk, csb_clk/2, csb_clk/3*
Security block	csb_clk/3	Off, *csb_clk, csb_clk/2, csb_clk/3*
USB DR	csb_clk/3	Off, *csb_clk, csb_clk/2, csb_clk/3*
PCI and DMA complex	csb_clk	Off, *csb_clk*

Table 81. Package Thermal Characteristics for TePBGA II (continued)

Parameter	Symbol	Value	Unit	Note
Junction-to-package natural convection on top	ψ_{JT}	6	°C/W	6

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

24.2 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$ where $P_{I/O}$ is the power dissipation of the I/O drivers.

24.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Generally, the value obtained on a single layer board is appropriate for a tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

24.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

NOTE

The heat sink cannot be mounted on the package.

Tyco Electronics
Chip Coolers™
www.chipcoolers.com

Wakefield Engineering
www.wakefield.com

Interface material vendors include the following:

Chomerics, Inc.
www.chomerics.com

Dow-Corning Corporation
Dow-Corning Electronic Materials
www.dowcorning.com

Shin-Etsu MicroSi, Inc.
www.microsi.com

The Bergquist Company
www.bergquistcompany.com

24.3 Heat Sink Attachment

The device requires the use of heat sinks. When heat sinks are attached, an interface material is required, preferably thermal grease and a spring clip. The spring clip should connect to the printed circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces that can lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. The recommended maximum compressive force on the top of the package is 10 lb force (4.5 kg force). Any adhesive attachment should attach to painted or plastic surfaces, and its performance should be verified under the application requirements.

24.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When a heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimize the size of the clearance to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction to case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

where:

T_J = junction temperature (°C)

T_C = case temperature of the package (°C)

Table 87. Document Revision History (continued)

Revision	Date	Substantive Change(s)
6	07/2011	In Section 2.2, "Power Sequencing," updated power down sequencing information.
5	07/2011	• In Table 2, "Absolute Maximum Ratings[1]," removed footnote 5 from LB_{IN} to OV_{IN}. Also, corrected footnote 5. • In Table 3, "Recommended Operating Conditions," added footnote 2 to AV_{DD}. • In Figure 2, "Overshoot/Undershoot Voltage for $GV_{DD}/LV_{DD}/OV_{DD}/LBV_{DD}$," added LBV_{DD}. • In Table 13, "DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V," updated I_{OZ} min/max to –50/50. • In Figure 11, "RGMII and RTBI AC Timing and Multiplexing Diagrams," added distinction between t_{SKRGT_RX} and t_{SKRGT_TX} signals. • In Table 33, "MII Management AC Timing Specifications," updated MDC frequency—removed Min and Max values, added Typical value. Also, updated footnote 2 and removed footnote 3. • In Table 48, "PCI DC Electrical Characteristics," updated V_{IH} min value to 2.0. • In Table 72, "TePBGA II Pinout Listing," added Note to LGPL4/LFRB_B/LGTA_B/LUPWAIT/LPBSE (to be consistent with AN3665, "MPC837xE Design Checklist." • In Table 74, "Operating Frequencies for TePBGA II," added Minimum Operating Frequency for eTSEC, and corrected DDR2 Minimum and Maximum Operating Frequency values.
4	11/2010	• In Table 25, "RGMII and RTBI DC Electrical Characteristics," updated V_{IH} min value to 1.7. • In Table 40, "Local Bus General Timing Parameters—PLL Bypass Mode," added row for t_{LBKHLR}. • In Section 10.2, "Local Bus AC Electrical Specifications," and in Section 23, "Clocking," updated LCCR to LCRR. • In Table 72, "TePBGA II Pinout Listing," added SD_WP to pin C9. Also clarified TEST_SEL0 and TEST_SEL1 pins—no change in functionality.
3	03/2010	• Added Section 4.3, "eTSEC Gigabit Reference Clock Timing." • In Table 34, "USB DC Electrical Characteristics," and Table 35, "USB General Timing Parameters (ULPI Mode Only)," added table footnotes . • In Table 39, "Local Bus General Timing Parameters—PLL Enable Mode," and Table 40, "Local Bus General Timing Parameters—PLL Bypass Mode," corrected footnotes for $t_{LBOTOT1}$, $t_{LBOTOT2}$, $t_{LBOTOT3}$. • In Figure 22, "Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (PLL Enable Mode)," and Figure 24, "Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 (PLL Enable Mode)," shifted "Input Signals: LAD[0:31]/LDP[0:3]" from the falling edge to the rising edge of LSYNC_IN. • In Figure 63, "Mechanical Dimensions and Bottom Surface Nomenclature of the TEPBGA II," added heat spreader. • In Section 25.6, "Pull-Up Resistor Requirements," removed "Ethernet Management MDIO pin" from list of open drain type pins. • In Table 72, "TePBGA II Pinout Listing," updated the Pin Type column for AVDD_C, AVDD_L, and AVDD_P pins. • in Table 72, "TePBGA II Pinout Listing," added Note 16 to eTSEC pins. • In Table 77, "CSB Frequency Options for Host Mode," and Table 78, "CSB Frequency Options for Agent Mode," updated *csb_clk* frequencies available. • In Table 84, "Part Numbering Nomenclature," removed footnote to "e300 core Frequency."

Table 87. Document Revision History (continued)

Revision	Date	Substantive Change(s)
2	10/2009	• In Table 3, “Recommended Operating Conditions,” added “Operating temperature range” values. • In Table 5, “Power Dissipation [1],” corrected maximal application for 800/400 MHz to 4.3 W. • In Table 5, “Power Dissipation [1],” added a column for “Typical Application at T_j = 65°C (W)”. • In Table 5, “Power Dissipation [1],” added a column for “Sleep Power at T_j = 65°C (W)”. • In Table 11, removed overbar from CFG_CLKIN_DIV. • In Table 17, “Current Draw Characteristics for MV_{REF},” updated I_{MVREF} maximum value for both DDR1 and DDR2 to 600 and 400 µA, respectively. Also, updated Note 1 and added Note 2. • In Table 20, “DDR1 and DDR2 SDRAM Input AC Timing Specifications,” column headings renamed to “Min” and “Max”. Footnote 2 updated to state “T is the MCK clock period”. • In Table 20, “DDR1 and DDR2 SDRAM Input AC Timing Specifications,” and Table 21, “DDR1 and DDR2 SDRAM Output AC Timing Specifications,” clarified that the frequency parameters are data rates. • In Table 29, “RMII Transmit AC Timing Specifications,” updated t_{RMTDX}I to 2.0 ns. • In Table 60, Gen 1i/1.5G Transmitter AC Specifications,” and Table 62, Gen 2i/3G Transmitter AC Specifications,” corrected titles from “Transmitter” to “Receiver”. • In Table 72, “TePBGA II Pinout Listing,” removed pin THERM0; it is now Reserved. Also added 1.05 V to VDD pin. • In Table 74, “Operating Frequencies for TePBGA II,” corrected “DDR2 memory bus frequency (MCK)” range to 125–200. • In Table 79, “e300 Core PLL Configuration,” added 3.5:1 and 4:1 core_clk: csb_clk ratio options. • In Table 80, “Example Clock Frequency Combinations,” updated column heading to “DDR data rate” . • In Section 20.2, “SPI AC Timing Specifications,” corrected t_{NIKHOX} and t_{NEKHOX} to t_{NIKHOV} and t_{NEKHOV}, respectively.
1	02/2009	• In Table 3, “Recommended Operating Conditions,” added two new rows for 800 MHz, and created two rows for SerDes. In addition, changed 666 to 667 MHz. • In Table 5, “Power Dissipation [1],” added Notes 4 and 5. In addition, changed 666 to 667 MHz. • In Table 13, “DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V,” Table 21, “DDR1 and DDR2 SDRAM Output AC Timing Specifications,” and Table 72, “TePBGA II Pinout Listing,” added footnote to references to MVREF, MDQ, and MDQS, referencing AN3665, *MPC837xE Design Checklist*. • In Table 21, updated t_{DDKHCX} minimum value for 333 MHz to 2.40. • In Table 72, “TePBGA II Pinout Listing,” added footnote to USBDR_STP_SUSPEND and modified footnote 10 and added footnote 14. • In Table 74, “Operating Frequencies for TePBGA II,” changed 667 to 800 MHz for *core_clk*. • In Table 80, “Example Clock Frequency Combinations,” added 800 MHz cells for e300 core. • Updated part numbering information in AF column in Table 84, “Part Numbering Nomenclature.” In addition, modified extended temperature information in notes 1 and 4. • In Table 85, “Available Parts (Core/DDR Data Rate),” added new row for 800/400 MHz.
0	12/2008	Initial public release.