E·XFL



Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300c4s
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 125°C (TA)
Security Features	-
Package / Case	689-BBGA Exposed Pad
Supplier Device Package	689-TEPBGA II (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8377cvranga

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

controller, dual I²C controllers, a 4-channel DMA controller, an enhanced secured digital host controller, and a general-purpose I/O port. This figure shows the block diagram of the chip.



Figure 1. MPC8377E Block Diagram and Features

The following features are supported in the chip:

- e300c4s core built on Power Architecture® technology with 32 KB instruction cache and 32 KB data cache, a floating point unit, and two integer units
- DDR1/DDR2 memory controller supporting a 32/64-bit interface
- Peripheral interfaces, such as a 32-bit PCI interface with up to 66-MHz operation
- 32-bit local bus interface running up to 133-MHz
- USB 2.0 (full/high speed) support
- Power management controller for low-power consumption
- High degree of software compatibility with previous-generation PowerQUICC processor-based designs for backward compatibility and easier software migration
- Optional security engine provides acceleration for control and data plane security protocols

The optional security engine (SEC 3.0) is noted with the extension "E" at the end. It allows CPU-intensive cryptographic operations to be offloaded from the main CPU core. The security-processing accelerator provides hardware acceleration for the DES, 3DES, AES, SHA-1, and MD-5 algorithms.

1.10 PCI Express Controller

The PCI Express controller includes the following features:

- PCI Express 1.0a compatible
- Two $\times 1$ links or one $\times 2$ link width
- Auto-detection of number of connected lanes
- Selectable operation as root complex or endpoint
- Both 32- and 64-bit addressing
- 128-byte maximum payload size
- Support for MSI and INTx interrupt messages
- Virtual channel 0 only
- Selectable Traffic Class
- Full 64-bit decode with 32-bit wide windows
- Dedicated four channel descriptor-based DMA engine per interface

1.11 Serial ATA (SATA) Controllers

The serial ATA (SATA) controllers have the following features:

- Supports Serial ATA Rev 2.5 Specification
- Spread spectrum clocking on receive
- Asynchronous notification
- Hot Plug including asynchronous signal recovery
- Link power management
- Native command queuing
- Staggered spin-up and port multiplier support
- Port multiplier support
- SATA 1.5 and 3.0 Gb/s operation
- Interrupt driven
- Power management support
- Error handling and diagnostic features
 - Far end/near end loopback
 - Failed CRC error reporting
 - Increased ALIGN insertion rates
- Scrambling and CONT override

8.2.1.2 MII Receive AC Timing Specifications

This table provides the MII receive AC timing specifications.

Table 27. MII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V \pm 5%.

Parameter	Symbol ¹	Min	Typical	Мах	Unit
Input low voltage	V _{IL}	_	—	0.7	V
Input high voltage	V _{IH}	1.9	—	—	V
RX_CLK clock period 10 Mbps	t _{MRX}	_	400	—	ns
RX_CLK clock period 100 Mbps	t _{MRX}	_	40	—	ns
RX_CLK duty cycle	t _{MRXH} /t _{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t _{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t _{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise time (20%–80%)	t _{MRXR}	1.0	—	4.0	ns
RX_CLK clock fall time (80%-20%)	t _{MRXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state)}

(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure provides the AC test load for eTSEC.



Figure 8. eTSEC AC Test Load

This figure shows the MII receive AC timing diagram.



Figure 9. MII Receive AC Timing Diagram

8.2.2 RGMII and RTBI AC Timing Specifications

This table presents the RGMII and RTBI AC timing specifications.

Table 28. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV $_{DD}$ of 2.5 V \pm 5%.

Parameter	Symbol ¹	Min	Typical	Max	Unit	Note
Data to clock output skew (at transmitter)	^t SKRGT	-600	0	600	ps	_
Data to clock input skew (at receiver)	t _{SKRGT}	1.0	_	2.8	ns	2
Clock period	t _{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 1000Base-T	t _{RGTH} /t _{RGT}	45	50	55	%	4
Duty cycle for 10BASE-T and 100BASE-TX	t _{RGTH} /t _{RGT}	40	50	60	%	3, 4
Rise time (20%–80%)	t _{RGTR}	—	_	0.75	ns	_
Fall time (20%-80%)	t _{RGTF}	—	_	0.75	ns	_
EC_GTX_CLK125 reference clock period	t _{G12}	—	8.0	_	ns	5
EC_GTX_CLK125 reference clock duty cycle measured at 0.5 \times LV $_{DD1}$	t _{G125H} /t _{G125}	47	—	53	%	_

Notes:

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).

- 2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
- 3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns \pm 40 ns and 40 ns \pm 4 ns, respectively.
- 4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between
- 5. This symbol represents the external EC_GTX_CLK125 and does not follow the original signal naming convention.

This figure provides the AC test load for eTSEC.



This figure shows the RGMII and RTBI AC timing and multiplexing diagrams.



Figure 11. RGMII and RTBI AC Timing and Multiplexing Diagrams

9.2 USB AC Electrical Specifications

This table describes the general timing parameters of the USB interface of the device.

Parameter	Symbol ¹	Min	Max	Unit	Note
USB clock cycle time	t _{USCK}	15	_	ns	2, 3, 4, 5
Input setup to USB clock—all inputs	t _{USIVKH}	4	_	ns	2, 3, 4, 5
Input hold to USB clock—all inputs	t _{USIXKH}	1	_	ns	2, 3, 4, 5
USB clock to output valid—all outputs	t _{USKHOV}		7	ns	2, 3, 4, 5
Output hold from USB clock—all outputs	t _{USKHOX}	2	—	ns	2, 3, 4, 5

Table 35. USB General Timing Parameters (ULPI Mode Only)

Notes:

 The symbols for timing specifications follow the pattern of t<sub>(First two letters of functional block)(signal)(state) (reference)(state) for inputs and t_{(First two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{USIXKH} symbolizes USB timing (US) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, t_{USKHOX} symbolizes USB timing (US) for the USB clock reference (K) to go high (H) with respect to the output (O) going invalid (X) or output hold time.
</sub>

- 2. All timings are in reference to the USB clock, USBDR_CLK.
- 3. All signals are measured from $OV_{DD}/2$ of the rising edge of the USB clock to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V signaling levels.
- 4. Input timings are measured at the pin.
- 5. For active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.

These two figures provide the AC test load and signals for the USB, respectively.



Due to the special implementation of the eSDHC, there are constraints regarding the clock and data signals propagation delay on the user board. The constraints are for minimum and maximum delays, as well as skew between the CLK and DAT/CMD signals.

In full speed mode, there is no need to add special delay on the data or clock signals. The user should make sure to meet the timing requirements as described further within this document.

If the system is designed to support both high-speed and full-speed cards, the high-speed constraints should be fulfilled. If the systems is designed to operate up to 25 MHz only, full-speed mode is recommended.

11.1 eSDHC DC Electrical Characteristics

This table provides the DC electrical characteristics for the eSDHC (SD/MMC) interface of the device.

Parameter	Symbol	Condition	Min	Мах	Unit
Input high voltage	V _{IH}	—	$0.625 \times \text{OV}_{\text{DD}}$	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	-0.3	$0.25 \times OV_{DD}$	V
Input current	I _{IN}	—	—	±30	μA
Output high voltage	V _{OH}	I _{OH} = −100 uA, at OV _{DD} (min)	$0.75 \times OV_{DD}$	—	V
Output low voltage	V _{OL}	I _{OL} = +100 uA, at OV _{DD} (min)	—	$0.125 \times OV_{DD}$	V

Table 41. eSDHC interface DC Electrical Characteristics

11.2 eSDHC AC Timing Specifications (Full-Speed Mode)

This section describes the AC electrical specifications for the eSDHC (SD/MMC) interface of the device. This table provides the eSDHC AC timing specifications for full-speed mode as defined in Figure 27 and Figure 28.

Table 42. eSDHC AC Timing Specifications for Full-Speed Mode

At recommended operating conditions $OV_{DD} = 3.3 \text{ V} \pm 165 \text{ mV}$.

Parameter	Symbol ¹	Min	Max	Unit	Note
SD_CLK clock frequency—full speed mode	f _{SFSCK}	0	25	MHz	_
SD_CLK clock cycle	t _{SFSCK}	40	_	ns	
SD_CLK clock frequency—identification mode	f _{SIDCK}	0	400	KHz	
SD_CLK clock low time	t _{SFSCKL}	15	_	ns	2
SD_CLK clock high time	t _{SFSCKH}	15	_	ns	2
SD_CLK clock rise and fall times	t _{SFSCKR} / t _{SFSCKF}	—	5	ns	2
Input setup times: SD_CMD, SD_DATx, SD_CD to SD_CLK	t _{SFSIVKH}	5	_	ns	2

This figure provides the boundary-scan timing diagram.



Figure 35. Boundary-Scan Timing Diagram

This figure provides the test access port timing diagram.



VM = Midpoint Voltage (OVDD/2)



13 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the chip.

13.1 I²C DC Electrical Characteristics

This table provides the DC electrical characteristics for the I^2C interface of the chip.

Table 46. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V \pm 165 mV.

Parameter	Symbol	Min	Мах	Unit	Note
Input high voltage level	V _{IH}	$0.7 \times OV_{DD}$	OV _{DD} + 0.3	V	—
Input low voltage level	V _{IL}	-0.3	$0.3 imes OV_{DD}$	V	—
Low level output voltage	V _{OL}	0	$0.2\times\text{OV}_\text{DD}$	V	1
Output fall time from $V_{IH}(\text{min})$ to $V_{IL}(\text{max})$ with a bus capacitance from 10 to 400 pF	t _{I2KLKV}	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t _{I2KHKL}	0	50	ns	3
Capacitance for each I/O pin	CI	—	10	pF	—
Input current (0 V \leq V _{IN} \leq OV _{DD})	I _{IN}	_	± 30	μA	4

Notes:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.

2. C_B = capacitance of one bus line in pF.

3. Refer to the MPC8379E PowerQUICC II Pro Integrated Host Processor Reference Manual for information on the digital filter used.

4. I/O pins will obstruct the SDA and SCL lines if OV_DD is switched off.

13.2 I²C AC Electrical Specifications

This table provides the AC timing parameters for the I^2C interface of the device.

Table 47. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 46).

Parameter	Symbol ¹	Min	Max	Unit	Note
SCL clock frequency	f _{I2C}	0	400	kHz	—
Low period of the SCL clock	t _{I2CL}	1.3	—	μs	—
High period of the SCL clock	t _{I2CH}	0.6	—	μs	—
Setup time for a repeated START condition	t _{I2SVKH}	0.6	—	μs	—
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t _{I2SXKL}	0.6	_	μs	—
Data setup time	t _{I2DVKH}	100	—	ns	—

Parameter	Comments	Symbol	Min	Typical	Max	Units	Note
Unexpected Electrical Idle Enter Detect Threshold Integration Time	An unexpected electrical idle (Vrx-diffp-p < Vrx-idle-det-diffp-p) must be recognized no longer than Trx-idle-det-diff-entertime to signal an unexpected idle condition.	T _{RX-IDLE-DET-DIFF-} ENTERTIME			10	ms	_
Total Skew	Skew across all lanes on a link. This includes variation in the length of SKP ordered set (e.g. COM and one to five SKP Symbols) at the Rx as well as any delay differences arising from the interconnect itself.	L _{RX-SKEW}			20	ns	_

Table 53. Differential Receiver (Rx) Input Specifications (continued)

Notes:

- 1. No test load is necessarily associated with this value.
- 2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 44 should be used as the Rx device when taking measurements (also refer to the receiver compliance eye diagram shown in Figure 43). If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
- 3. A T_{Rx-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The TRx-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive Tx UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
- 4. The receiver input impedance will result in a differential return loss greater than or equal to 10 dB with the D+ line biased to 300 mV and the D- line biased to -300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the D+ and D- line (that is, as measured by a vector network analyzer with 50- Ω probes, see Figure 44). Note that the series capacitors, C_{Tx}, is optional for the return loss measurement.
- 5. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
- 6. The Rx DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the Rx ground.
- 7. It is recommended that the recovered Tx UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

15.5 Receiver Compliance Eye Diagrams

The Rx eye diagram in Figure 43 is specified using the passive compliance/test measurement load (see Figure 44) in place of any real PCI Express Rx component. In general, the minimum receiver eye diagram measured with the compliance/test measurement load (see Figure 44) is larger than the minimum receiver eye diagram measured over a range of systems at the input receiver of any real PCI Express component. The degraded eye diagram at the input receiver is due to traces internal to the package as well as silicon parasitic characteristics that cause the real PCI Express component to vary in impedance from the

output driver features a 50- Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.



Figure 57. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)

Figure 58 shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Since LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with device SerDes reference clock input's DC requirement, AC-coupling has to be used. Figure 58 assumes that the LVPECL clock driver's output impedance is 50 Ω . R1 is used to DC-bias the LVPECL outputs prior to AC-coupling. Its value could be ranged from 140 Ω to 240 Ω depending on clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50 Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the device SerDes reference clock's differential input amplitude requirement (between 200 mV and 800 mV differential peak). For example, if the LVPECL output's differential peak is 900 mV and the desired SerDes reference clock input amplitude is selected as 600 mV, the attenuation factor is 0.67, which requires R2 = 25 Ω . Consult clock

21.3 SerDes Transmitter and Receiver Reference Circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.



Figure 62. SerDes Transmitter and Receiver Reference Circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below in this document based on the application usage:

- Section 8, "Ethernet: Enhanced Three-Speed Ethernet (eTSEC)"
- Section 15, "PCI Express"
- Section 16, "Serial ATA (SATA)"

Note that an external AC coupling capacitor is required for the above three serial transmission protocols with the capacitor value defined in specification of each protocol section.

22 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions.

22.1 Package Parameters for the MPC8377E TePBGA II

The package parameters are provided in the following list. The package type is $31 \text{ mm} \times 31 \text{ mm}$, 689 plastic ball grid array (TePBGA II).

Package outline	$31 \text{ mm} \times 31 \text{ mm}$
Interconnects	689
Pitch	1.00 mm
Module height (typical)	2.0 mm to 2.46 mm (maximum)
Solder Balls	3.5% Ag, 96.5% Sn
Ball diameter (typical)	0.60 mm
Pitch Module height (typical) Solder Balls Ball diameter (typical)	1.00 mm 2.0 mm to 2.46 mm (maximum) 3.5% Ag, 96.5% Sn 0.60 mm

Signal	Package Pin Number	Pin Type	Power Supply	Note
MDQ35	AE1	I/O	GVDD	11
MDQ36	V6	I/O	GVDD	11
MDQ37	Y5	I/O	GVDD	11
MDQ38	AA4	I/O	GVDD	11
MDQ39	AB6	I/O	GVDD	11
MDQ40	AD3	I/O	GVDD	11
MDQ41	AC4	I/O	GVDD	11
MDQ42	AD4	I/O	GVDD	11
MDQ43	AF1	I/O	GVDD	11
MDQ44	AE4	I/O	GVDD	11
MDQ45	AC5	I/O	GVDD	11
MDQ46	AE2	I/O	GVDD	11
MDQ47	AE3	I/O	GVDD	11
MDQ48	AG1	I/O	GVDD	11
MDQ49	AG2	I/O	GVDD	11
MDQ50	AG3	I/O	GVDD	11
MDQ51	AF5	I/O	GVDD	11
MDQ52	AE5	I/O	GVDD	11
MDQ53	AD7	I/O	GVDD	11
MDQ54	AH2	I/O	GVDD	11
MDQ55	AG4	I/O	GVDD	11
MDQ56	AH3	I/O	GVDD	11
MDQ57	AG5	I/O	GVDD	11
MDQ58	AF8	I/O	GVDD	11
MDQ59	AJ5	I/O	GVDD	11
MDQ60	AF6	I/O	GVDD	11
MDQ61	AF7	I/O	GVDD	11
MDQ62	AH6	I/O	GVDD	11
MDQ63	AH7	I/O	GVDD	11
MDQS0	C8	I/O	GVDD	11
MDQS1	C4	I/O	GVDD	11
MDQS2	E3	I/O	GVDD	11
MDQS3	G2	I/O	GVDD	11

Signal	Package Pin Number	Pin Type	Power Supply	Note
MDQS4	AB5	I/O	GVDD	11
MDQS5	AD1	I/O	GVDD	11
MDQS6	AH1	I/O	GVDD	11
MDQS7	AJ3	I/O	GVDD	11
MDQS8	G1	I/O	GVDD	11
MECC0/MSRCID0	J6	I/O	GVDD	_
MECC1/MSRCID1	J3	I/O	GVDD	
MECC2/MSRCID2	K2	I/O	GVDD	
MECC3/MSRCID3	К3	I/O	GVDD	
MECC4/MSRCID4	J5	I/O	GVDD	
MECC5/MDVAL	J2	I/O	GVDD	
MECC6	L5	I/O	GVDD	
MECC7	L2	I/O	GVDD	
MODT0	N5	0	GVDD	6
MODT1	U6	0	GVDD	6
MODT2	M6	0	GVDD	6
MODT3	P6	0	GVDD	6
MRAS_B	AA3	0	GVDD	
MVREF1	К4	I	GVDD	11
MVREF2	W4	I	GVDD	11
MWE_B	Y2	0	GVDD	_
	DUART Interface			
UART_SIN1/ MSRCID2/LSRCID2	L28	I/O	OVDD	
UART_SOUT1/ MSRCID0/LSRCID0	L27	0	OVDD	—
UART_CTS_B[1]/ MSRCID4/LSRCID4	K26	I/O	OVDD	_
UART_RTS_B1	N27	0	OVDD	_
UART_SIN2/ MSRCID3/LSRCID3	K27	I/O	OVDD	—
UART_SOUT2/ MSRCID1/LSRCID1	K28	0	OVDD	_
UART_CTS_B[2]/ MDVAL/LDVAL	K29	I/O	OVDD	—

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
PCI_AD27	AA29	I/O	OVDD	
PCI_AD28	AC24	I/O	OVDD	
PCI_AD29	AC25	I/O	OVDD	_
PCI_AD30	AB28	I/O	OVDD	
PCI_AD31	AE24	I/O	OVDD	
PCI_C_BE_B0	T26	I/O	OVDD	_
PCI_C_BE_B1	T28	I/O	OVDD	
PCI_C_BE_B2	V29	I/O	OVDD	
PCI_C_BE_B3	Y29	I/O	OVDD	_
PCI_DEVSEL_B	U28	I/O	OVDD	5
PCI_FRAME_B	V27	I/O	OVDD	_
PCI_GNT_B0	AE27	I/O	OVDD	_
PCI_GNT_B[1]/ CPCI_HS_LED	AC28	0	OVDD	_
PCI_GNT_B[2]/ CPCI_HS_ENUM	AD27	0	OVDD	—
PCI_GNT_B[3]/PCI_PME	AC27	0	OVDD	—
PCI_GNT_B[4]	AE25	0	OVDD	—
PCI_IDSEL	W28	I	OVDD	5
PCI_INTA_B/IRQ_OUT_B	AD29	0	OVDD	2
PCI_IRDY_B	U29	I/O	OVDD	5
PCI_PAR	V25	I/O	OVDD	—
PCI_PERR_B	Y25	I/O	OVDD	5
PCI_REQ_B0	AE26	I/O	OVDD	—
PCI_REQ_B[1]/CPCI_HS_ES	AC29	I	OVDD	_
PCI_REQ_B2	AB29	I	OVDD	_
PCI_REQ_B3	AD26	I	OVDD	
PCI_REQ_B4	W27	I	OVDD	
PCI_RESET_OUT_B	AD28	0	OVDD	_
PCI_SERR_B	V26	I/O	OVDD	5
PCI_STOP_B	W26	I/O	OVDD	5
PCI_TRDY_B	Y24	I/O	OVDD	5
M66EN	AD15	I	OVDD	

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note			
Programmable Interrupt Controller (PIC) Interface							
MCP_OUT_B	AD14	0	OVDD	2			
IRQ_B0/MCP_IN_B/GPIO2[12]	F9	I/O	OVDD				
IRQ_B1/GPIO2[13]	E9	I/O	OVDD				
IRQ_B2/GPIO2[14]	F10	I/O	OVDD				
IRQ_B3/GPIO2[15]	D9	I/O	OVDD	_			
IRQ_B4/GPIO2[16]/SD_WP	C9	I/O	OVDD	_			
IRQ_B5/GPIO2[17]/ USBDR_PWRFAULT	AE10	I/O	OVDD	_			
IRQ_B6/GPIO2[18]	AD10	I/O	OVDD	_			
IRQ_B7/GPIO2[19]	AD9	I/O	OVDD	_			
	PMC Interface						
QUIESCE_B	D13	0	OVDD				
	SerDes1 Interface						
L1_SD_IMP_CAL_RX	AJ14	I	L1_XPADVDD				
L1_SD_IMP_CAL_TX	AG19	I	L1_XPADVDD	_			
L1_SD_REF_CLK	AJ17	I	L1_XPADVDD	_			
L1_SD_REF_CLK_B	AH17	I	L1_XPADVDD	_			
L1_SD_RXA_N	AJ15	I	L1_XPADVDD	_			
L1_SD_RXA_P	AH15	I	L1_XPADVDD	_			
L1_SD_RXE_N	AJ19	I	L1_XPADVDD	_			
L1_SD_RXE_P	AH19	I	L1_XPADVDD				
L1_SD_TXA_N	AF15	0	L1_XPADVDD	_			
L1_SD_TXA_P	AE15	0	L1_XPADVDD				
L1_SD_TXE_N	AF18	0	L1_XPADVDD				
L1_SD_TXE_P	AE18	0	L1_XPADVDD				
L1_SDAVDD_0	AJ18	SerDes PLL Power (1.0 or 1.05 V)	—				
L1_SDAVSS_0	AG17	SerDes PLL GND	—				
L1_XCOREVDD	AH14, AJ16, AF17, AH20, AJ20	SerDes Core Power (1.0 or 1.05 V)	_	—			

Table 72. TePBGA II Pinout Listing (continued)

As shown in Figure 64, the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create the coherent system bus clock (csb_clk), the internal clock for the DDR controller (ddr_clk), and the internal clock for the local bus interface unit ($lbiu_clk$).

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

csb_clk = {PCI_SYNC_IN × (1 + CFG_CLKIN_DIV)} × SPMF Eqn. 20

In PCI host mode, PCI_SYNC_IN \times (1 + CFG_CLKIN_DIV) is the CLKIN frequency.

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the e300 core multiplies up the *csb_clk* frequency to create the internal clock for the e300 core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low register (RCWLR) which is loaded at power-on reset or by one of the hard-coded reset options. See Chapter 4, "Reset, Clocking, and Initialization," in the *MPC8379E Reference Manual* for more information on the clock subsystem.

The internal *ddr_clk* frequency is determined by the following equation:

Note that ddr_clk is not the external memory bus frequency; ddr_clk passes through the DDR clock divider (÷2) to create the differential DDR memory bus clock outputs (MCK and $\overline{\text{MCK}}$). However, the data rate is the same frequency as ddr_clk .

The internal *lbiu_clk* frequency is determined by the following equation:

Note that *lbiu_clk* is not the external local bus frequency; *lbiu_clk* passes through the LBIU clock divider to create the external local bus clock outputs (LCLK[0:2]). The eLBC clock divider ratio is controlled by LCRR[CLKDIV].

Some of the internal units may be required to be shut off or operate at lower frequency than the *csb_clk* frequency. Those units have a default clock ratio that can be configured by a memory mapped register after the device comes out of reset. Table 73 specifies which units have a configurable clock frequency.

Table	73.	Configurable	Clock	Units
-------	-----	--------------	-------	-------

Unit	Default Frequency	Options
eTSEC1, eTSEC2	csb_clk/3	Off, csb_clk, csb_clk/2, csb_clk/3
eSDHC and I ² C1 ¹	csb_clk/3	Off, csb_clk, csb_clk/2, csb_clk/3
Security block	csb_clk/3	Off, csb_clk, csb_clk/2, csb_clk/3
USB DR	csb_clk/3	Off, csb_clk, csb_clk/2, csb_clk/3
PCI and DMA complex	csb_clk	Off, csb_clk

MPC8377E PowerQUICC II Pro Processor Hardware Specifications, Rev. 8

Eqn. 22

			Input Clock Frequency (MHz) ²		
CFG_CLKIN_DIV at Reset ¹	SPMF	<i>csb_clk</i> : Input Clock Ratio ¹	25	33.33	66.67
			csb_	<i>clk</i> Frequency (MHz)
High	0010	2 : 1			133
High	0011	3 : 1			200
High	0100	4 : 1		133	267
High	0101	5 : 1		167	333
High	0110	6 : 1	150	200	400
High	0111	7 : 1	175	233	
High	1000	8 : 1	200	267	
High	1001	9 : 1	225	300	
High	1010	10 : 1	250	333	
High	1011	11 : 1	275	367	
High	1100	12 : 1	300	400	
High	1101	13 : 1	325		
High	1110	14 : 1	350		
High	1111	15 : 1	375		

Table 77. CSB Frequency Options for Host Mode

Notes:

1. CFG_CLKIN_DIV select the ratio between CLKIN and PCI_SYNC_OUT.

2. CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

Table 78	CSB	Frequenc	v Ontions	for A	aont l	ApoM
Table 10	. СЭР	riequenc	y options	IOI A	genti	vioue

			Input C	(MHz) ²	
CFG_CLKIN_DIV at reset ¹	SPMF	<i>csb_clk</i> : Input Clock Ratio ¹	25	33.33	66.67
			csb_clk Frequency (MHz)		MHz)
Low	0010	2 : 1			133
Low	0011	3 : 1			200
Low	0100	4 : 1		133	267
Low	0101	5 : 1		167	333
Low	0110	6 : 1	150	200	400

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term} . The measured voltage is $V_2 = (1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

This table summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD} , nominal OV_{DD} , 105°C.

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI Signals (not including PCI output clocks)	PCI Output Clocks (including PCI_SYNC_OUT)	DDR DRAM	Symbol	Unit
R _N	42 Target	25 Target	42 Target	20 Target	Z ₀	W
R _P	42 Target	25 Target	42 Target	20 Target	Z ₀	W
Differential	NA	NA	NA	NA	Z _{DIFF}	W

Table 83. Impedance Characteristics

Note: Nominal supply voltages. See Table 2, $T_i = 105^{\circ}C$.

25.5 Configuration Pin Muxing

The device provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 k Ω on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While HRESET is asserted however, these pins are treated as inputs. The value presented on these pins while HRESET is asserted, is latched when PORESET deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

25.6 Pull-Up Resistor Requirements

The device requires high resistance pull-up resistors (10 k Ω is recommended) on open drain type pins including I²C pins and IPIC interrupt pins.

For more information on required pull-up resistors and the connections required for the JTAG interface, see AN3665, "MPC837xE Design Checklist."

26 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 26.1, "Part Numbers Fully Addressed by This Document."

How to Reach Us:

Home Page: www.freescale.com

Web Support: http://www.freescale.com/support

USA/Europe or Locations Not Listed:

Freescale Semiconductor, Inc. Technical Information Center, EL516 2100 East Elliot Road Tempe, Arizona 85284 1-800-521-6274 or +1-480-768-2130 www.freescale.com/support

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH Technical Information Center Schatzbogen 7 81829 Muenchen, Germany +44 1296 380 456 (English) +46 8 52200080 (English) +49 89 92103 559 (German) +33 1 69 35 48 48 (French) www.freescale.com/support

Japan:

Freescale Semiconductor Japan Ltd. Headquarters ARCO Tower 15F 1-8-1, Shimo-Meguro, Meguro-ku Tokyo 153-0064 Japan 0120 191014 or +81 3 5437 9125 support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor China Ltd. Exchange Building 23F No. 118 Jianguo Road Chaoyang District Beijing 100022 China +86 10 5879 8000 support.asia@freescale.com Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale, the Freescale logo, CodeWarrior, ColdFire, PowerQUICC, QorlQ, StarCore, and Symphony are trademarks of Freescale Semiconductor, Inc., Reg. U.S. Pat. & Tm. Off. CoreNet, QorlQ Qonverge, QUICC Engine, and VortiQa are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org.

© 2008-2012 Freescale Semiconductor, Inc.

Document Number: MPC8377EEC Rev. 8 05/2012



