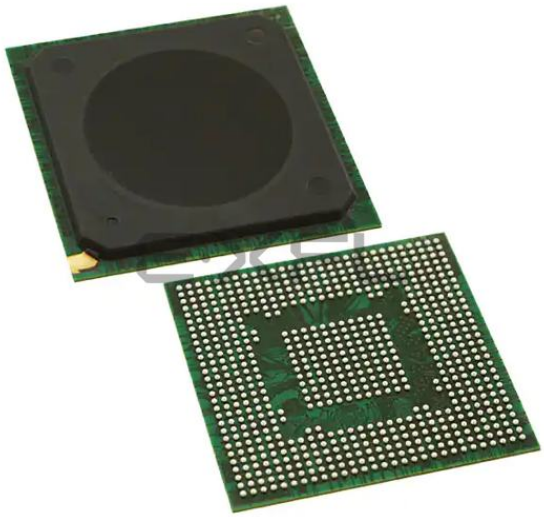

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e300c4s |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 533MHz |
| Co-Processors/DSP | Security; SEC 3.0 |
| RAM Controllers | DDR, DDR2 |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (2) |
| SATA | SATA 3Gbps (2) |
| USB | USB 2.0 + PHY (1) |
| Voltage - I/O | 1.8V, 2.5V, 3.3V |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Security Features | Cryptography, Random Number Generator |
| Package / Case | 689-BBGA Exposed Pad |
| Supplier Device Package | 689-TEPBGA II (31x31) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8377ecvrajf |

**Table 2. Absolute Maximum Ratings[1] (continued)**

| Characteristic | | Symbol | Max Value | Unit | Note |
|---|---|---|---|---|---|
| Input voltage | DDR DRAM signals | $MV_{IN}$ | –0.3 to ($GV_{DD}$ + 0.3) | V | 2, 4 |
| | DDR DRAM reference | $MV_{REF}$ | –0.3 to ($GV_{DD}$ + 0.3) | V | 2, 4 |
| | Three-speed Ethernet signals | $LV_{IN}$ | –0.3 to ($LV_{DD}$ + 0.3) | V | — |
| | PCI, DUART, CLKIN, system control and power management, $I^2C$, and JTAG signals | $OV_{IN}$ | –0.3 to ($OV_{DD}$ + 0.3) | V | 3, 4, 5 |
| | Local Bus | $LB_{IN}$ | –0.3 to ($LBV_{DD}$ + 0.3) | V | — |
| Storage temperature range | | $T_{STG}$ | –55 to 150 | °C | — |

**Notes:**
1. Functional and tested operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** $MV_{IN}$ must not exceed $GV_{DD}$ by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** $OV_{IN}$ must not exceed $OV_{DD}$ by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. (M,O)$V_{IN}$ and $MV_{REF}$ may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
5. Overshoot/undershoot by $OV_{IN}$ on the PCI interface does not comply to the *PCI Electrical Specification* for 3.3-V operation, as shown in Figure 2.
6. L[1,2]_$n$$V_{DD}$ includes $SDAV_{DD\_0}$, $XCOREV_{DD}$, and $XPADV_{DD}$ power inputs.

## 2.1.2 Power Supply Voltage Specification

This table provides recommended operating conditions for the device. Note that the values in this table are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

**Table 3. Recommended Operating Conditions**

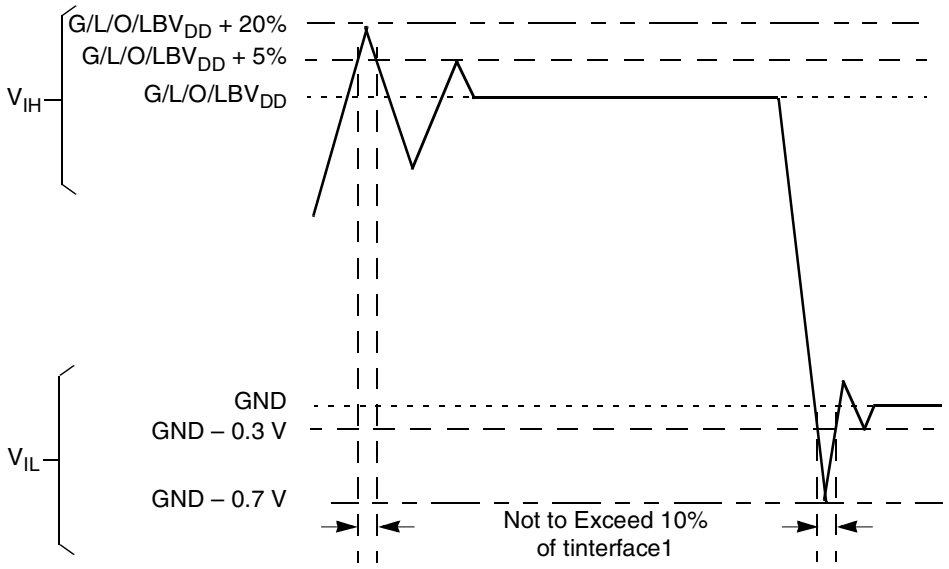
| Characteristic | | Symbol | Recommended Value | Unit | Note |
|---|---|---|---|---|---|
| Core supply voltage | up to 667 MHz | $V_{DD}$ | 1.0 ± 50 mV | V | 1 |
| | 800 MHz | | 1.05 ± 50 mV | V | 1 |
| PLL supply voltage (e300 core, eLBC and system) | up to 667 MHz | $AV_{DD}$ | 1.0 ± 50 mV | V | 1, 2 |
| | 800 MHz | | 1.05 ± 50 mV | V | 1, 2 |
| DDR1 and DDR2 DRAM I/O voltage | | $GV_{DD}$ | 2.5 V ± 125 mV<br>1.8 V ± 90 mV | V | 1 |
| Three-speed Ethernet I/O, MII management voltage | | $LV_{DD}$[1,2] | 3.3 V ± 165 mV<br>2.5 V ± 125 mV | V | — |
| PCI, local bus, DUART, system control and power management, $I^2C$, and JTAG I/O voltage | | $OV_{DD}$ | 3.3 V ± 165 mV | V | 1 |
| Local Bus | | $LBV_{DD}$ | 1.8 V ± 90 mV<br>2.5 V ± 125 mV<br>3.3 V ± 165 mV | V | — |

**Table 3. Recommended Operating Conditions (continued)**

| Characteristic | | Symbol | Recommended Value | Unit | Note |
|---|---|---|---|---|---|
| SerDes | up to 667 MHz | L[1,2]_$nV_{DD}$ | 1.0 ± 50 mV | V | 1, 3 |
| | 800 MHz | | 1.05 V ± 50 mV | V | 1, 3 |
| Operating temperature range | commerical | $T_a$<br>$T_j$ | $T_a$=0 (min)—<br>$T_j$=125 (max) | °C | — |
| | extended temperature | $T_a$<br>$T_j$ | $T_a$=–40 (min)—<br>$T_j$=125 (max) | °C | — |

**Notes:**
1. $GV_{DD}$, $OV_{DD}$, $AV_{DD}$, and $V_{DD}$ must track each other and must vary in the same direction—either in the positive or negative direction.
2. $AV_{DD}$ is the input to the filter discussed in Section 25.1, "PLL Power Supply Filtering," and is not necessarily the voltage at the AVDD pin.
3. L[1,2]_$nV_{DD}$, $SDAV_{DD\_0}$, $XCOREV_{DD}$, and $XPADV_{DD}$ power inputs.

This figure shows the undershoot and overshoot voltages at the interfaces of the device.




**Note:**
1. Note that $t_{interface}$ refers to the clock period associated with the bus clock interface.
2. Note that with the PCI overshoot allowed (as specified above), the device does not fully comply with the maximum AC ratings and device protection guideline outlined in the *PCI Rev. 2.3 Specification* (Section 4.2.2.3).

**Figure 2. Overshoot/Undershoot Voltage for $GV_{DD}$/$LV_{DD}$/$OV_{DD}$/$LBV_{DD}$**

**Table 5. Power Dissipation [1] (continued)**

| Core Frequency (MHz) | CSB/DDR Frequency (MHz) | Sleep Power at $T_j$ = 65°C (W) [2] | Typical Application at $T_j$ = 65°C (W) [2] | Typical Application at $T_j$ = 125°C (W) [3] | Max Application at $T_j$ = 125°C (W) [4] |
|---|---|---|---|---|---|
| **600** | 400 | 1.45 | 2.1 | 3.4 | 4.1 |
| | 300 | 1.45 | 2.0 | 3.3 | 4.0 |
| **667** | 333 | 1.45 | 2.1 | 3.3 | 4.1 |
| | 266 | 1.45 | 2.0 | 3.3 | 3.9 |
| **800** | 400 | 1.45 | 2.5 | 3.8 | 4.3 |

**Notes:**
1. The values do not include I/O supply power ($OV_{DD}$, $LV_{DD}$, $GV_{DD}$) or $AV_{DD}$. For I/O power values, see Table 6.
2. Typical power is based on a voltage of $V_{DD}$ = 1.0 V for core frequencies ≤ 667 MHz or $V_{DD}$ = 1.05 V for core frequencies of 800 MHz, and running a Dhrystone benchmark application.
3. Typical power is based on a voltage of $V_{DD}$ = 1.0 V for core frequencies ≤ 667 MHz or $V_{DD}$ = 1.05 V for core frequencies of 800 MHz, and running a Dhrystone benchmark application.
4. Maximum power is based on a voltage of $V_{DD}$ = 1.0 V for core frequencies ≤ 667 MHz or $V_{DD}$ = 1.05 V for core frequencies of 800 MHz, worst case process, and running an artificial smoke test.

This table shows the estimated typical I/O power dissipation for the device.

**Table 6. Typical I/O Power Dissipation**

| Interface | Parameter | $GV_{DD}$ (1.8 V) | $GV_{DD}$/$LBV_{DD}$ (2.5 V) | $OV_{DD}$ (3.3 V) | $LV_{DD}$ (3.3 V) | $LV_{DD}$ (2.5 V) | L[1,2]_$n$$V_{DD}$ (1.0 V) | Unit | Comments |
|---|---|---|---|---|---|---|---|---|---|
| DDR I/O 65% utilization 2 pair of clocks | 200 MHz data rate, 32-bit | 0.28 | 0.35 | — | — | — | — | W | — |
| | 200 MHz data rate, 64-bit | 0.41 | 0.49 | — | — | — | — | W | |
| | 266 MHz data rate, 32-bit | 0.31 | 0.4 | — | — | — | — | W | |
| | 266 MHz data rate, 64-bit | 0.46 | 0.56 | — | — | — | — | W | |
| | 300 MHz data rate, 32-bit | 0.33 | 0.43 | — | — | — | — | W | |
| | 300 MHz data rate, 64-bit | 0.48 | 0.6 | — | — | — | — | W | |
| | 333 MHz data rate, 32-bit | 0.35 | 0.45 | — | — | — | — | W | |
| | 333 MHz data rate, 64-bit | 0.51 | 0.64 | — | — | — | — | W | |
| | 400 MHz data rate, 32-bit | 0.38 | — | — | — | — | — | W | |
| | 400 MHz data rate, 64-bit | 0.56 | — | — | — | — | — | W | |

**Table 21. DDR1 and DDR2 SDRAM Output AC Timing Specifications (continued)**

| Parameter | Symbol[1] | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| MDQS epilogue end | $t_{DDKHME}$ | –0.6 | 0.6 | ns | 6, 8 |

**Notes:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, $t_{DDKHAS}$ symbolizes DDR timing (DD) for the time $t_{MCK}$ memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, $t_{DDKLDX}$ symbolizes DDR timing (DD) for the time $t_{MCK}$ memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ//MDM/MDQS.
4. Note that $t_{DDKHMH}$ follows the symbol conventions described in Note 1. For example, $t_{DDKHMH}$ describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). $t_{DDKHMH}$ can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8379E PowerQUICC II Pro Host Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data MDQ, ECC, or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK*n* at the pins of the microprocessor. Note that $t_{DDKHMP}$ follows the symbol conventions described in Note 1.
7. Clock Control register is set to adjust the memory clocks by 1/2 the applied cycle.
8. See AN3665, “MPC837xE Design Checklist,” for proper DDR termination.

The minimum frequency for DDR2 is 250 MHz data rate (125 MHz clock), 167 MHz data rate (83 MHz clock) for DDR1. This figure shows the DDR1 and DDR2 SDRAM output timing for the MCK to MDQS skew measurement ($t_{DDKHMH}$).

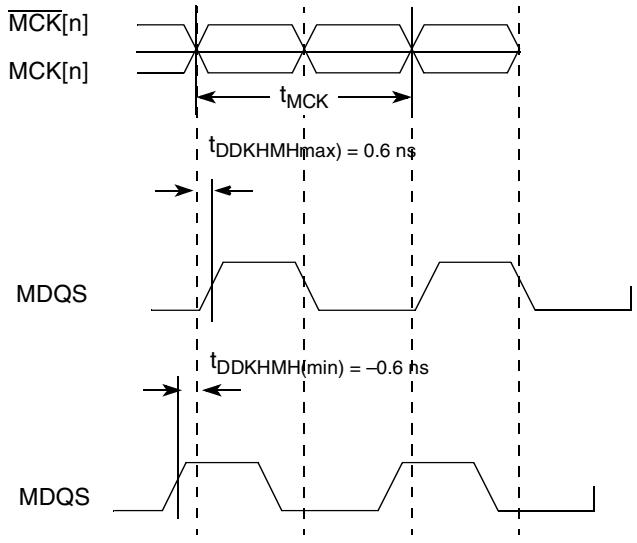



**Figure 4. DDR Timing Diagram for $t_{DDKHMH}$**

This figure shows the DDR1 and DDR2 SDRAM output timing diagram.

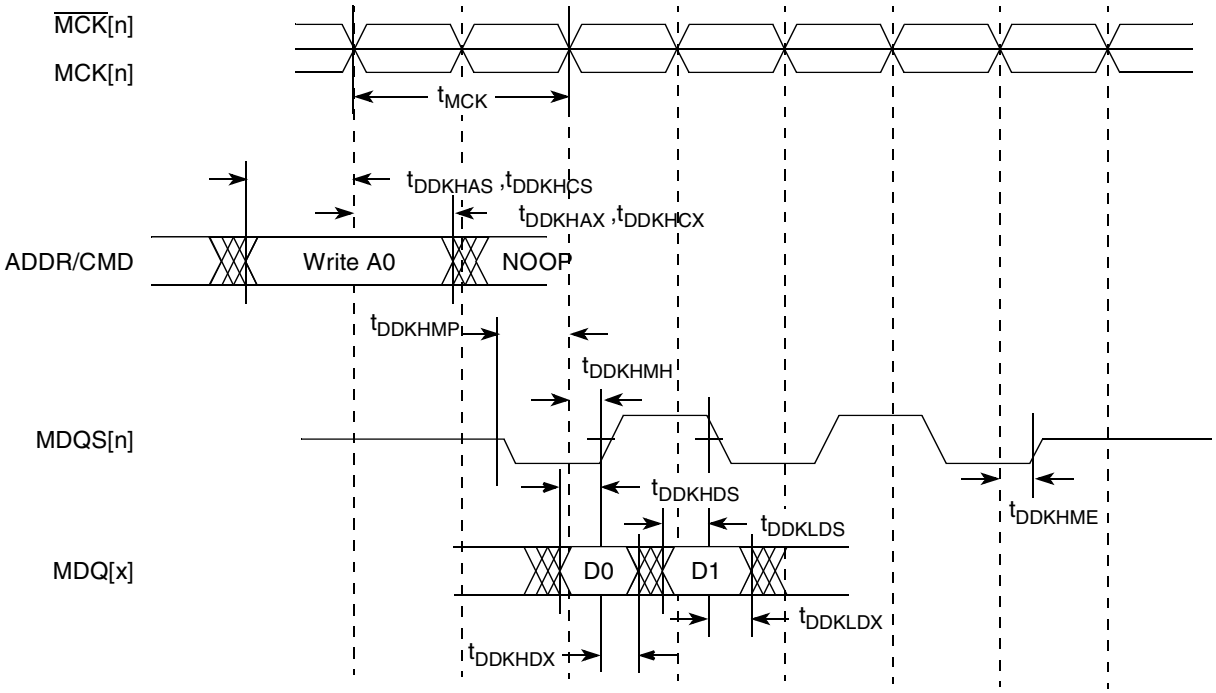



**Figure 5. DDR1 and DDR2 SDRAM Output Timing Diagram**

This figure provides AC test load for the DDR bus.

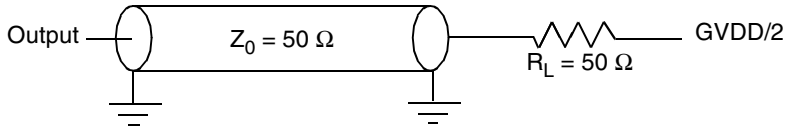



**Figure 6. DDR AC Test Load**

# 7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the chip.

## 7.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface of the device.

**Table 22. DUART DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | $OV_{DD}$ + 0.3 | V |
| Low-level input voltage $OV_{DD}$ | $V_{IL}$ | –0.3 | 0.8 | V |
| High-level output voltage, $I_{OH}$ = –100 μA | $V_{OH}$ | $OV_{DD}$ – 0.2 | — | V |

Due to the special implementation of the eSDHC, there are constraints regarding the clock and data signals propagation delay on the user board. The constraints are for minimum and maximum delays, as well as skew between the CLK and DAT/CMD signals.

In full speed mode, there is no need to add special delay on the data or clock signals. The user should make sure to meet the timing requirements as described further within this document.

If the system is designed to support both high-speed and full-speed cards, the high-speed constraints should be fulfilled. If the systems is designed to operate up to 25 MHz only, full-speed mode is recommended.

## 11.1 eSDHC DC Electrical Characteristics

This table provides the DC electrical characteristics for the eSDHC (SD/MMC) interface of the device.

**Table 41. eSDHC interface DC Electrical Characteristics**

| Parameter | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | — | $0.625 \times OV_{DD}$ | $OV_{DD} + 0.3$ | V |
| Input low voltage | $V_{IL}$ | — | –0.3 | $0.25 \times OV_{DD}$ | V |
| Input current | $I_{IN}$ | — | — | ±30 | μA |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –100 uA, at $OV_{DD}$(min) | $0.75 \times OV_{DD}$ | — | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = +100 uA, at $OV_{DD}$(min) | — | $0.125 \times OV_{DD}$ | V |

## 11.2 eSDHC AC Timing Specifications (Full-Speed Mode)

This section describes the AC electrical specifications for the eSDHC (SD/MMC) interface of the device. This table provides the eSDHC AC timing specifications for full-speed mode as defined in Figure 27 and Figure 28.

**Table 42. eSDHC AC Timing Specifications for Full-Speed Mode**

At recommended operating conditions $OV_{DD}$ = 3.3 V ± 165 mV.

| Parameter | Symbol[1] | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| SD_CLK clock frequency—full speed mode | $f_{SFSCK}$ | 0 | 25 | MHz | — |
| SD_CLK clock cycle | $t_{SFSCK}$ | 40 | — | ns | — |
| SD_CLK clock frequency—identification mode | $f_{SIDCK}$ | 0 | 400 | KHz | — |
| SD_CLK clock low time | $t_{SFSCKL}$ | 15 | — | ns | 2 |
| SD_CLK clock high time | $t_{SFSCKH}$ | 15 | — | ns | 2 |
| SD_CLK clock rise and fall times | $t_{SFSCKR}$/ $t_{SFSCKF}$ | — | 5 | ns | 2 |
| Input setup times: SD_CMD, SD_DATx, SD_CD to SD_CLK | $t_{SFSIVKH}$ | 5 | — | ns | 2 |

### 11.2.1 Full-Speed Output Path (Write)

This figure provides the data and command output timing diagram.

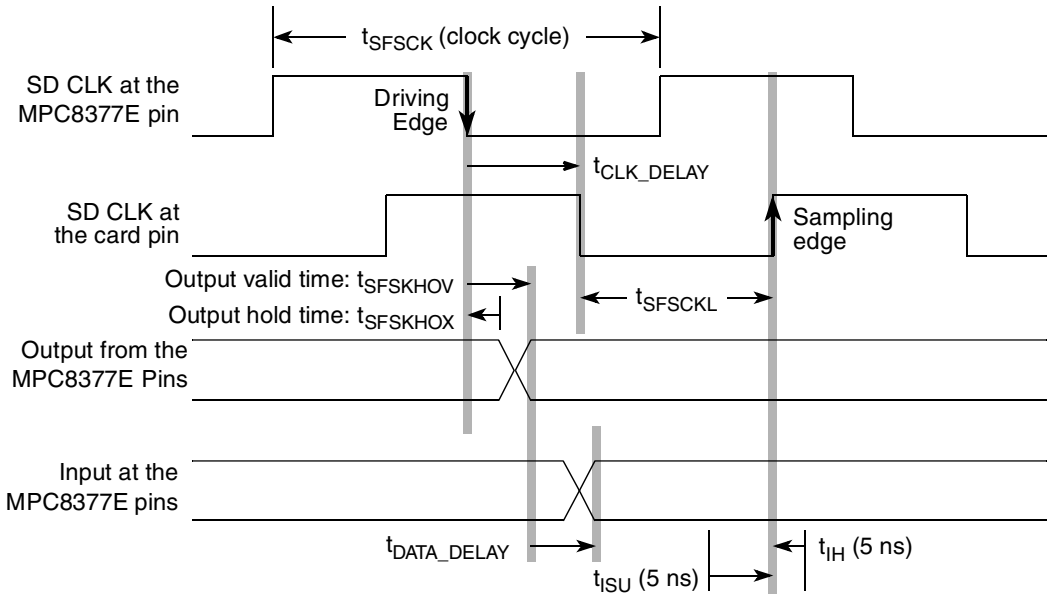



**Figure 27. Full Speed Output Path**

#### 11.2.1.1 Full-Speed Write Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

No clock delay:

$$t_{SFSKHOV} + t_{DATA\_DELAY} + t_{ISU} < t_{SFSCKL} \quad \textit{Eqn. 1}$$

With clock delay:

$$t_{SFSKHOV} + t_{DATA\_DELAY} + t_{ISU} < t_{SFSCKL} + t_{CLK\_DELAY} \quad \textit{Eqn. 2}$$

$$t_{DATA\_DELAY} + t_{SFSCKL} < t_{SFSCK} + t_{CLK\_DELAY} - t_{ISU} - t_{SFSKHOV} \quad \textit{Eqn. 3}$$

This means that data can be delayed versus clock up to 11 ns in ideal case of $t_{SFSCKL}$ = 20 ns:

$t_{DATA\_DELAY} + 20 < 40 + t_{CLK\_DELAY} - 5 - 4$

$t_{DATA\_DELAY} < 11 + t_{CLK\_DELAY}$

#### 11.2.1.2 Full-Speed Write Meeting Hold (Minimum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

$$t_{CLK\_DELAY} < t_{SFSCKL} + t_{SFSKHOX} + t_{DATA\_DELAY} - t_{IH} \quad \textit{Eqn. 4}$$

This figure provides the AC test load for PCI.

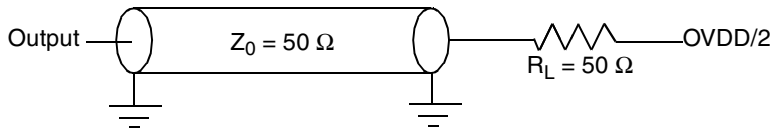



**Figure 39. PCI AC Test Load**

This figure shows the PCI input AC timing conditions.

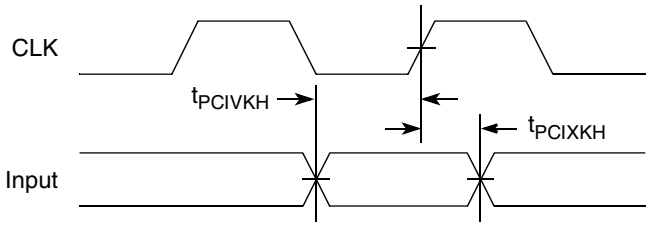



**Figure 40. PCI Input AC Timing Measurement Conditions**

This figure shows the PCI output AC timing conditions.

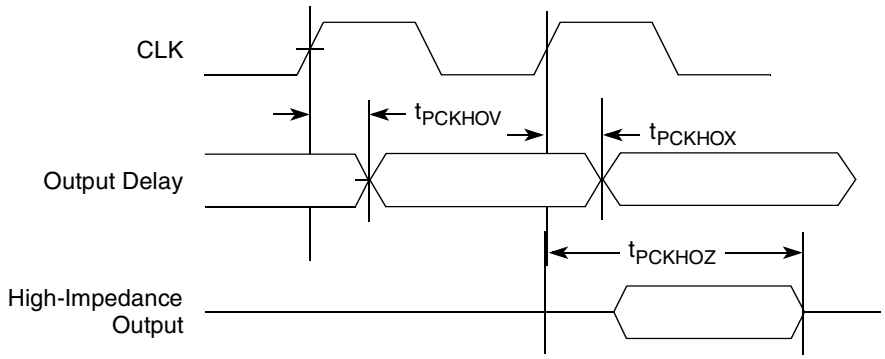



**Figure 41. PCI Output AC Timing Measurement Condition**

# 15 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus.

## 15.1 DC Requirements for PCI Express SD_REF_CLK and SD_REF_CLK

For more information see Section 21, “High-Speed Serial Interfaces (HSSI).”

**Table 52. Differential Transmitter (Tx) Output Specifications (continued)**

| Parameter | Conditions | Symbol | Min | Typical | Max | Units | Note |
|---|---|---|---|---|---|---|---|
| Common mode return loss | Measured over 50 MHz to 1.25 GHz. | $RL_{TX-CM}$ | 6 | — | — | dB | 4 |
| DC differential Tx impedance | Tx DC differential mode low impedance | $Z_{TX-DIFF-DC}$ | 80 | 100 | 120 | Ω | — |
| Transmitter DC impedance | Required Tx D+ as well as D– DC impedance during all states | $Z_{TX-DC}$ | 40 | — | — | Ω | — |
| Lane-to-Lane output skew | Static skew between any two transmitter lanes within a single link | $L_{TX-SKEW}$ | — | — | 500 + 2 UI | ps | — |
| AC coupling capacitor | All transmitters should be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. | $C_{TX}$ | 75 | — | 200 | nF | — |
| Crosslink random timeout | This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one downstream and one upstream port. | $T_{crosslink}$ | 0 | — | 1 | ms | 7 |

**Notes:**
1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 44 and measured over any 250 consecutive Tx UIs. (Also refer to the transmitter compliance eye diagram shown in Figure 42.)
3. A $T_{TX-EYE}$ = 0.70 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.30 UI for the transmitter collected over any 250 consecutive Tx UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total Tx jitter budget collected over any 250 consecutive Tx UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The transmitter input impedance will result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes, see Figure 44). Note that the series capacitors, $C_{TX}$, is optional for the return loss measurement.
5. Measured between 20%–80% at transmitter package pins into a test load as shown in Figure 44 for both $V_{TX-D+}$ and $V_{TX-D-}$.
6. See Section 4.3.1.8 of the *PCI Express Base Specifications*, Rev 1.0a.
7. See Section 4.2.6.3 of the *PCI Express Base Specifications*, Rev 1.0a.

## 15.4.2 Transmitter Compliance Eye Diagrams

The Tx eye diagram in Figure 42 is specified using the passive compliance/test measurement load (see Figure 44) in place of any real PCI Express interconnect + Rx component. There are two eye diagrams that must be met for the transmitter. Both diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams differ in voltage depending on whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit is always relative to the transition bit.

**Table 53. Differential Receiver (Rx) Input Specifications (continued)**

| Parameter | Comments | Symbol | Min | Typical | Max | Units | Note |
|---|---|---|---|---|---|---|---|
| Unexpected Electrical Idle Enter Detect Threshold Integration Time | An unexpected electrical idle (Vrx-diffp-p < Vrx-idle-det-diffp-p) must be recognized no longer than Trx-idle-det-diff-entertime to signal an unexpected idle condition. | $T_{RX-IDLE-DET-DIFF-ENTERTIME}$ | — | — | 10 | ms | — |
| Total Skew | Skew across all lanes on a link. This includes variation in the length of SKP ordered set (e.g. COM and one to five SKP Symbols) at the Rx as well as any delay differences arising from the interconnect itself. | $L_{RX-SKEW}$ | — | — | 20 | ns | — |

**Notes:**
1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 44 should be used as the Rx device when taking measurements (also refer to the receiver compliance eye diagram shown in Figure 43). If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A $T_{Rx-EYE}$ = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The TRx-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive Tx UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. The receiver input impedance will result in a differential return loss greater than or equal to 10 dB with the D+ line biased to 300 mV and the D– line biased to –300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes, see Figure 44). Note that the series capacitors, $C_{Tx}$, is optional for the return loss measurement.
5. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
6. The Rx DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the Rx ground.
7. It is recommended that the recovered Tx UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

## 15.5 Receiver Compliance Eye Diagrams

The Rx eye diagram in Figure 43 is specified using the passive compliance/test measurement load (see Figure 44) in place of any real PCI Express Rx component. In general, the minimum receiver eye diagram measured with the compliance/test measurement load (see Figure 44) is larger than the minimum receiver eye diagram measured over a range of systems at the input receiver of any real PCI Express component. The degraded eye diagram at the input receiver is due to traces internal to the package as well as silicon parasitic characteristics that cause the real PCI Express component to vary in impedance from the

## 19.1 IPIC DC Electrical Characteristics

This table provides the DC electrical characteristics for the external interrupt pins of the chip.

**Table 67. IPIC DC Electrical Characteristics**

| Parameter | Condition | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| Input high voltage | — | $V_{IH}$ | 2.0 | $OV_{DD}$ + 0.3 | V |
| Input low voltage | — | $V_{IL}$ | –0.3 | 0.8 | V |
| Input current | — | $I_{IN}$ | — | ±30 | μA |
| Output low voltage | $I_{OL}$ = 6.0 mA | $V_{OL}$ | — | 0.5 | V |
| Output low voltage | $I_{OL}$ = 3.2 mA | $V_{OL}$ | — | 0.4 | V |

**Note:**
1. This table applies for pins $\overline{\text{IRQ}}$[0:7], $\overline{\text{IRQ\_OUT}}$, $\overline{\text{MCP\_OUT}}$.
2. $\overline{\text{IRQ\_OUT}}$ and $\overline{\text{MCP\_OUT}}$ are open drain pins, thus $V_{OH}$ is not relevant for those pins.

## 19.2 IPIC AC Timing Specifications

This table provides the IPIC input and output AC timing specifications.

**Table 68. IPIC Input AC Timing Specifications**

| Parameter | Symbol | Min | Unit |
|---|---|---|---|
| IPIC inputs—minimum pulse width | $t_{PIWID}$ | 20 | ns |

**Note:**
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least $t_{PIWID}$ ns to ensure proper operation when working in edge triggered mode.

# 20 SPI

This section describes the DC and AC electrical specifications for the SPI of the chip.

## 20.1 SPI DC Electrical Characteristics

This table provides the DC electrical characteristics for the device SPI.

**Table 69. SPI DC Electrical Characteristics**

| Parameter | Condition | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| Input high voltage | — | $V_{IH}$ | 2.0 | $OV_{DD}$ + 0.3 | V |
| Input low voltage | — | $V_{IL}$ | –0.3 | 0.8 | V |
| Input current | — | $I_{IN}$ | — | ± 30 | μA |
| Output high voltage | $I_{OH}$ = –8.0 mA | $V_{OH}$ | 2.4 | — | V |

**Table 69. SPI DC Electrical Characteristics (continued)**

| Parameter | Condition | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| Output low voltage | $I_{OL}$ = 8.0 mA | $V_{OL}$ | — | 0.5 | V |
| Output low voltage | $I_{OL}$ = 3.2 mA | $V_{OL}$ | — | 0.4 | V |

## 20.2 SPI AC Timing Specifications

This table provides the SPI input and output AC timing specifications.

**Table 70. SPI AC Timing Specifications**

| Parameter | Symbol[1] | Min | Max | Unit |
|---|---|---|---|---|
| SPI outputs—Master mode (internal clock) delay | $t_{NIKHOV}$ | 0.5 | 6 | ns |
| SPI outputs—Slave mode (external clock) delay | $t_{NEKHOV}$ | 2 | 8 | ns |
| SPI inputs—Master mode (internal clock) input setup time | $t_{NIIVKH}$ | 4 | — | ns |
| SPI inputs—Master mode (internal clock) input hold time | $t_{NIIXKH}$ | 0 | — | ns |
| SPI inputs—Slave mode (external clock) input setup time | $t_{NEIVKH}$ | 4 | — | ns |
| SPI inputs—Slave mode (external clock) input hold time | $t_{NEIXKH}$ | 2 | — | ns |

**Notes:**
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{NIKHOV}$ symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).
2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin. The maximum SPICLK input frequency is 66.666 MHz.

This figure provides the AC test load for the SPI.

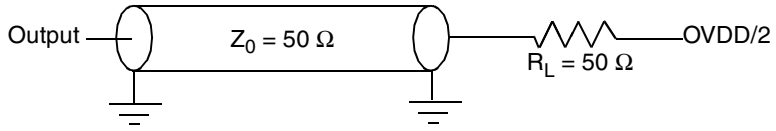



**Figure 48. SPI AC Test Load**

These figures represent the AC timing from Table 70. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

- **Single-Ended Swing**

  The transmitter output signals and the receiver input signals SD*n*_TX, $\overline{\text{SD}n\text{\_TX}}$, SD*n*_RX and $\overline{\text{SD}n\text{\_RX}}$ each have a peak-to-peak swing of A – B volts. This is also referred as each signal wire's single-ended swing.

- **Differential Output Voltage, $V_{OD}$** (or **Differential Output Swing**):

  The differential output voltage (or swing) of the transmitter, $V_{OD}$, is defined as the difference of the two complimentary output voltages: $V_{SDn\_TX} - V_{\overline{SDn\_TX}}$. The $V_{OD}$ value can be either positive or negative.

- **Differential Input Voltage, $V_{ID}$** (or **Differential Input Swing**):

  The differential input voltage (or swing) of the receiver, $V_{ID}$, is defined as the difference of the two complimentary input voltages: $V_{SDn\_RX} - V_{\overline{SDn\_RX}}$. The $V_{ID}$ value can be either positive or negative.

- **Differential Peak Voltage**, $V_{DIFFp}$

  The peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak voltage, $V_{DIFFp} = |A - B|$ volts.

- **Differential Peak-to-Peak**, $V_{DIFFp-p}$

  Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2 \times V_{DIFFp} = 2 \times |(A - B)|$ volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2 \times |V_{OD}|$.

- **Differential Waveform**

  The differential waveform is constructed by subtracting the inverting signal ($\overline{\text{SD}n\text{\_TX}}$, for example) from the non-inverting signal (SD*n*_TX, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 60 as an example for differential waveform.

- **Common Mode Voltage, $V_{cm}$**

  The common mode voltage is equal to one half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm\_out} = (V_{SDn\_TX} + V_{\overline{SDn\_TX}}) \div 2 = (A + B) \div 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes it may be even different between the receiver input and driver output circuits within the same component. It is also referred as the DC offset in some occasion.

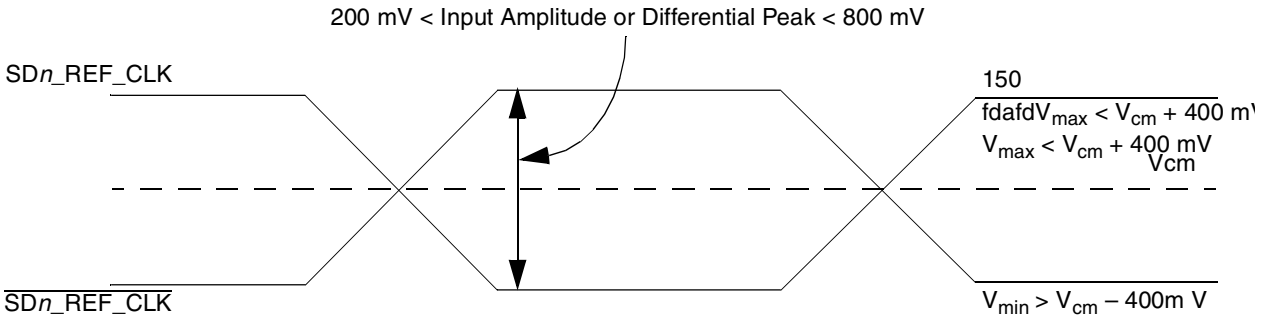



**Figure 54. Differential Reference Clock Input DC Requirements (External AC-Coupled)**

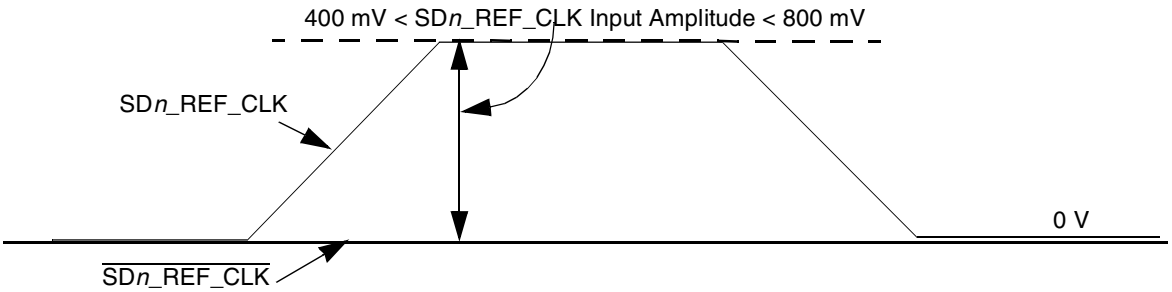



**Figure 55. Single-Ended Reference Clock Input DC Requirements**

## 21.2.3 Interfacing With Other Differential Signaling Levels

The following list provides information about interfacing with other differential signaling levels.

- With on-chip termination to SGND_SRDS*n* (xcorevss), the differential reference clocks inputs are HCSL (high-speed current steering logic) compatible DC-coupled.
- Many other low voltage differential type outputs like LVDS (low voltage differential signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 mV to 400 mV) for DC-coupled connection.
- LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

**Table 72. TePBGA II Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| MDQ2 | C7 | I/O | GVDD | 11 |
| MDQ3 | D8 | I/O | GVDD | 11 |
| MDQ4 | A7 | I/O | GVDD | 11 |
| MDQ5 | A5 | I/O | GVDD | 11 |
| MDQ6 | A3 | I/O | GVDD | 11 |
| MDQ7 | C6 | I/O | GVDD | 11 |
| MDQ8 | D7 | I/O | GVDD | 11 |
| MDQ9 | E8 | I/O | GVDD | 11 |
| MDQ10 | B1 | I/O | GVDD | 11 |
| MDQ11 | D5 | I/O | GVDD | 11 |
| MDQ12 | B3 | I/O | GVDD | 11 |
| MDQ13 | D6 | I/O | GVDD | 11 |
| MDQ14 | C3 | I/O | GVDD | 11 |
| MDQ15 | C2 | I/O | GVDD | 11 |
| MDQ16 | D4 | I/O | GVDD | 11 |
| MDQ17 | E6 | I/O | GVDD | 11 |
| MDQ18 | F6 | I/O | GVDD | 11 |
| MDQ19 | G4 | I/O | GVDD | 11 |
| MDQ20 | F8 | I/O | GVDD | 11 |
| MDQ21 | E4 | I/O | GVDD | 11 |
| MDQ22 | C1 | I/O | GVDD | 11 |
| MDQ23 | G6 | I/O | GVDD | 11 |
| MDQ24 | F2 | I/O | GVDD | 11 |
| MDQ25 | G5 | I/O | GVDD | 11 |
| MDQ26 | H6 | I/O | GVDD | 11 |
| MDQ27 | H4 | I/O | GVDD | 11 |
| MDQ28 | D1 | I/O | GVDD | 11 |
| MDQ29 | G3 | I/O | GVDD | 11 |
| MDQ30 | H5 | I/O | GVDD | 11 |
| MDQ31 | F1 | I/O | GVDD | 11 |
| MDQ32 | W6 | I/O | GVDD | 11 |
| MDQ33 | AC1 | I/O | GVDD | 11 |
| MDQ34 | AC3 | I/O | GVDD | 11 |

**Table 72. TePBGA II Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---|---|---|---|---|
| **Programmable Interrupt Controller (PIC) Interface** | | | | |
| MCP_OUT_B | AD14 | O | OVDD | 2 |
| IRQ_B0/MCP_IN_B/GPIO2[12] | F9 | I/O | OVDD | — |
| IRQ_B1/GPIO2[13] | E9 | I/O | OVDD | — |
| IRQ_B2/GPIO2[14] | F10 | I/O | OVDD | — |
| IRQ_B3/GPIO2[15] | D9 | I/O | OVDD | — |
| IRQ_B4/GPIO2[16]/SD_WP | C9 | I/O | OVDD | — |
| IRQ_B5/GPIO2[17]/ USBDR_PWRFAULT | AE10 | I/O | OVDD | — |
| IRQ_B6/GPIO2[18] | AD10 | I/O | OVDD | — |
| IRQ_B7/GPIO2[19] | AD9 | I/O | OVDD | — |
| **PMC Interface** | | | | |
| QUIESCE_B | D13 | O | OVDD | — |
| **SerDes1 Interface** | | | | |
| L1_SD_IMP_CAL_RX | AJ14 | I | L1_XPADVDD | — |
| L1_SD_IMP_CAL_TX | AG19 | I | L1_XPADVDD | — |
| L1_SD_REF_CLK | AJ17 | I | L1_XPADVDD | — |
| L1_SD_REF_CLK_B | AH17 | I | L1_XPADVDD | — |
| L1_SD_RXA_N | AJ15 | I | L1_XPADVDD | — |
| L1_SD_RXA_P | AH15 | I | L1_XPADVDD | — |
| L1_SD_RXE_N | AJ19 | I | L1_XPADVDD | — |
| L1_SD_RXE_P | AH19 | I | L1_XPADVDD | — |
| L1_SD_TXA_N | AF15 | O | L1_XPADVDD | — |
| L1_SD_TXA_P | AE15 | O | L1_XPADVDD | — |
| L1_SD_TXE_N | AF18 | O | L1_XPADVDD | — |
| L1_SD_TXE_P | AE18 | O | L1_XPADVDD | — |
| L1_SDAVDD_0 | AJ18 | SerDes PLL Power (1.0 or 1.05 V) | — | — |
| L1_SDAVSS_0 | AG17 | SerDes PLL GND | — | — |
| L1_XCOREVDD | AH14, AJ16, AF17, AH20, AJ20 | SerDes Core Power (1.0 or 1.05 V) | — | — |

**Table 79. e300 Core PLL Configuration (continued)**

| RCWLR[COREPLL] | | | *core_clk* : *csb_clk* Ratio | VCO Divider [1] |
|---|---|---|---|---|
| 0–1 | 2–5 | 6 | | |
| **01** | **0001** | 1 | 1.5:1 | 4 |
| **10** | **0001** | 1 | 1.5:1 | 8 |
| **00** | **0010** | 0 | 2:1 | 2 |
| **01** | **0010** | 0 | 2:1 | 4 |
| **10** | **0010** | 0 | 2:1 | 8 |
| **00** | **0010** | 1 | 2.5:1 | 2 |
| **01** | **0010** | 1 | 2.5:1 | 4 |
| **10** | **0010** | 1 | 2.5:1 | 8 |
| **00** | **0011** | 0 | 3:1 | 2 |
| **01** | **0011** | 0 | 3:1 | 4 |
| **10** | **0011** | 0 | 3:1 | 8 |
| **00** | **0011** | 1 | 3.5:1 | 2 |
| **01** | **0011** | 1 | 3.5:1 | 4 |
| **10** | **0011** | 1 | 3.5:1 | 8 |
| **00** | **0100** | 0 | 4:1 | 2 |
| **01** | **0100** | 0 | 4:1 | 4 |
| **10** | **0100** | 0 | 4:1 | 8 |

**Notes:**
1. Core VCO frequency = Core frequency × VCO divider. Note that VCO divider has to be set properly so that the core VCO frequency is in the range of 800–1600 MHz.

## 23.3 Suggested PLL Configurations

This table shows suggested PLL configurations for different input clocks (LBCM = 0).

**Table 80. Example Clock Frequency Combinations**

| | | | | | | | | eLBC [1] | | | e300 Core [1] | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Ref [1]** | **LBCM** | **DDRCM** | **SVCOD** | **SPMF** | **Sys VCO[1,2]** | **CSB[1,3]** | **DDR data rate[1,4]** | **/2** | **/4** | **/8** | **× 1** | **× 1.5** | **× 2** | **× 2.5** | **× 3** |
| 25.0 | 0 | 1 | 2 | 5 | 500 | 125 | 250 | 62.5 | 31.3 | 15.6 | — | — | — | — | 375 |
| 25.0 | 0 | 1 | 2 | 6 | 600 | 150 | 300 | 75 [6] | 37.5 | 18.8 | — | — | — | 375 | 450 |
| 33.3 | 0 | 1 | 2 | 5 | 667 | 167 | 333 | 83.3 [6] | 41.6 | 20.8 | — | — | 333 | 416 | 500 |
| 33.3 | 0 | 1 | 2 | 4 | 533 | 133 | 267 | 66.7 | 33.3 | 16.7 | — | — | — | 333 | 400 |

**Table 80. Example Clock Frequency Combinations (continued)**

| | | | | | | | | eLBC [1] | | | e300 Core [1] | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Ref [1] | LBCM | DDRCM | SVCOD | SPMF | Sys VCO[1,2] | CSB[1,3] | DDR data rate[1,4] | /2 | /4 | /8 | × 1 | × 1.5 | × 2 | × 2.5 | × 3 |
| 48.0 | 0 | 1 | 2 | 3 | 576 | 144 | 288 | 72 [6] | 36 | 18 | — | — | — | 360 | 432 |
| 66.7 | 0 | 1 | 2 | 2 | 533 | 133 | 266 | 66.7 | 33.3 | 16.7 | — | — | — | 333 | 400 |
| 25.0 | 0 | 0 | 4 | 8 | 800 | 200 | 200 | 100 [6] | 50 | 25 | — | — | 400 | 500 | 600 |
| 33.3 | 0 | 0 | 2 | 8 | 533 | 266.7 | 267 | 133 [6] | 66.7 | 33.3 | — | 400 | 533 | 667 | 800 |
| 50.0 | 0 | 0 | 4 | 4 | 800 | 200 | 200 | 100 [6] | 50 | 25 | — | — | 400 | 500 | 600 |
| 50.0 | 0 | 0 | 2 | 8 | 800 | 400 | 400 [5] | — | 100 [6] | 50 | — | 600 | 800 | — | — |
| 66.7 | 0 | 0 | 2 | 4 | 533 | 266.7 | 267 | 133 [6] | 66.7 | 33.3 | — | 400 | 533 | 667 | 800 |
| 66.7 | 0 | 0 | 2 | 5 | 667 | 333 | 333 | — | 83.3 [6] | 41.6 | 333 | 500 | 667 | — | — |
| 66.7 | 0 | 0 | 2 | 6 | 800 | 400 | 400 [5] | — | 100 [6] | 50 | 400 | 600 | 800 | — | — |

**Notes:**
1. Values in MHz.
2. System PLL VCO range: 400–800 MHz.
3. CSB frequencies less than 133 MHz will not support Gigabit Ethernet rates.
4. Minimum data rate for DDR2 is 250 MHz and for DDR1 is 167 MHz.
5. Applies to DDR2 only.
6. Applies to eLBC PLL-enabled mode only.

# 24 Thermal

This section describes the thermal specifications of this chip.

## 24.1 Thermal Characteristics

This table provides the package thermal characteristics for the 689 31 × 31mm TePBGA II package.

**Table 81. Package Thermal Characteristics for TePBGA II**

| Parameter | Symbol | Value | Unit | Note |
|---|---|---|---|---|
| Junction-to-ambient natural convection on single layer board (1s) | $R_{\theta JA}$ | 21 | °C/W | 1, 2 |
| Junction-to-ambient natural convection on four layer board (2s2p) | $R_{\theta JA}$ | 15 | °C/W | 1, 2, 3 |
| Junction-to-ambient (at 200 ft/min) on single layer board (1s) | $R_{\theta JMA}$ | 16 | °C/W | 1, 3 |
| Junction-to-ambient (at 200 ft/min) on four layer board (2s2p) | $R_{\theta JMA}$ | 12 | °C/W | 1, 3 |
| Junction-to-board thermal | $R_{\theta JB}$ | 8 | °C/W | 4 |
| Junction-to-case thermal | $R_{\theta JC}$ | 6 | °C/W | 5 |

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the VDD, OVDD, GVDD, and LVDD planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

## 25.3 Connection Recommendations

To ensure reliable operation, it is highly recommended that unused inputs be connected to an appropriate signal level. Unused active low inputs should be tied to OVDD, GVDD, or LVDD as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external VDD, GVDD, LVDD, OVDD, and GND pins of the device.

## 25.4 Output Buffer DC Impedance

The device drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for $I^2C$).

To measure $Z_0$ for the single-ended drivers, an external resistor is connected from the chip pad to OVDD or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 66). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and $R_P$ is trimmed until the voltage at the pad equals $OV_{DD}/2$. $R_P$ then becomes the resistance of the pull-up devices. $R_P$ and $R_N$ are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

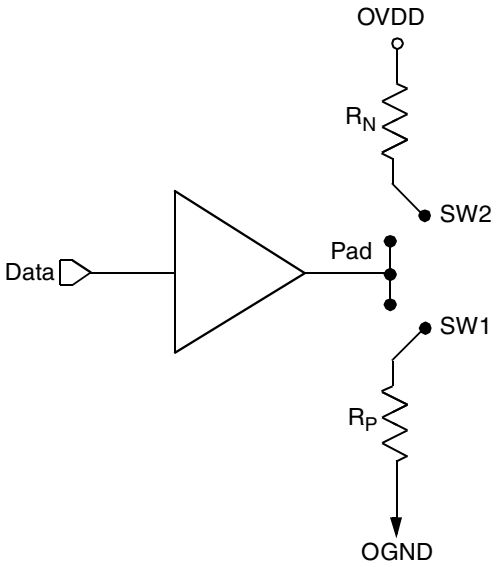



**Figure 66. Driver Impedance Measurement**

**Table 87. Document Revision History (continued)**

| Revision | Date | Substantive Change(s) |
|---|---|---|
| 6 | 07/2011 | In Section 2.2, "Power Sequencing," updated power down sequencing information. |
| 5 | 07/2011 | • In Table 2, "Absolute Maximum Ratings[1]," removed footnote 5 from $LB_{IN}$ to $OV_{IN}$. Also, corrected footnote 5.<br>• In Table 3, "Recommended Operating Conditions," added footnote 2 to $AV_{DD}$.<br>• In Figure 2, "Overshoot/Undershoot Voltage for $GV_{DD}/LV_{DD}/OV_{DD}/LBV_{DD}$," added $LBV_{DD}$.<br>• In Table 13, "DDR2 SDRAM DC Electrical Characteristics for $GV_{DD}$(typ) = 1.8 V," updated $I_{OZ}$ min/max to –50/50.<br>• In Figure 11, "RGMII and RTBI AC Timing and Multiplexing Diagrams," added distinction between $t_{SKRGT\_RX}$ and $t_{SKRGT\_TX}$ signals.<br>• In Table 33, "MII Management AC Timing Specifications," updated MDC frequency—removed Min and Max values, added Typical value. Also, updated footnote 2 and removed footnote 3.<br>• In Table 48, "PCI DC Electrical Characteristics," updated $V_{IH}$ min value to 2.0.<br>• In Table 72, "TePBGA II Pinout Listing," added Note to LGPL4/LFRB_B/LGTA_B/LUPWAIT/LPBSE (to be consistent with AN3665, "MPC837xE Design Checklist."<br>• In Table 74, "Operating Frequencies for TePBGA II," added Minimum Operating Frequency for eTSEC, and corrected DDR2 Minimum and Maximum Operating Frequency values. |
| 4 | 11/2010 | • In Table 25, "RGMII and RTBI DC Electrical Characteristics," updated $V_{IH}$ min value to 1.7.<br>• In Table 40, "Local Bus General Timing Parameters—PLL Bypass Mode," added row for $t_{LBKHLR}$.<br>• In Section 10.2, "Local Bus AC Electrical Specifications," and in Section 23, "Clocking," updated LCCR to LCRR.<br>• In Table 72, "TePBGA II Pinout Listing," added SD_WP to pin C9. Also clarified TEST_SEL0 and TEST_SEL1 pins—no change in functionality. |
| 3 | 03/2010 | • Added Section 4.3, "eTSEC Gigabit Reference Clock Timing."<br>• In Table 34, "USB DC Electrical Characteristics," and Table 35, "USB General Timing Parameters (ULPI Mode Only)," added table footnotes .<br>• In Table 39, "Local Bus General Timing Parameters—PLL Enable Mode," and Table 40, "Local Bus General Timing Parameters—PLL Bypass Mode," corrected footnotes for $t_{LBOTOT1}$, $t_{LBOTOT2}$, $t_{LBOTOT3}$.<br>• In Figure 22, "Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (PLL Enable Mode)," and Figure 24, "Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 (PLL Enable Mode)," shifted "Input Signals: LAD[0:31]/LDP[0:3]" from the falling edge to the rising edge of LSYNC_IN.<br>• In Figure 63, "Mechanical Dimensions and Bottom Surface Nomenclature of the TEPBGA II," added heat spreader.<br>• In Section 25.6, "Pull-Up Resistor Requirements," removed "Ethernet Management MDIO pin" from list of open drain type pins.<br>• In Table 72, "TePBGA II Pinout Listing," updated the Pin Type column for AVDD_C, AVDD_L, and AVDD_P pins.<br>• in Table 72, "TePBGA II Pinout Listing," added Note 16 to eTSEC pins.<br>• In Table 77, "CSB Frequency Options for Host Mode," and Table 78, "CSB Frequency Options for Agent Mode," updated *csb_clk* frequencies available.<br>• In Table 84, "Part Numbering Nomenclature," removed footnote to "e300 core Frequency." |