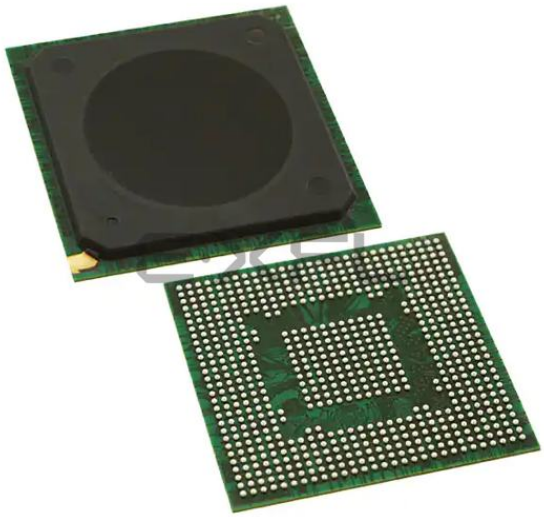

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300c4s
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	533MHz
Co-Processors/DSP	Security; SEC 3.0
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 125°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	689-BBGA Exposed Pad
Supplier Device Package	689-TEPBGA II (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8377ecvrajfa

There are two I^2C controllers. These synchronous, multi-master buses can be connected to additional devices for expansion and system development.

The DUART supports full-duplex operation and is compatible with the PC16450 and PC16550 programming models. 16-byte FIFOs are supported for both the transmitter and the receiver.

The main component of the enhanced local bus controller (eLBC) is its memory controller, which provides a seamless interface to many types of memory devices and peripherals. The memory controller is responsible for controlling eight memory banks shared by a NAND Flash control machine (FCM), a general-purpose chip-select machine (GPCM), and up to three user-programmable machines (UPMs). As such, it supports a minimal glue logic interface to SRAM, EPROM, NOR Flash EPROM, NAND Flash, EPROM, burstable RAM, regular DRAM devices, extended data output DRAM devices, and other peripherals. The eLBC external address latch enable (LALE) signal allows multiplexing of addresses with data signals to reduce the device pin count.

The enhanced local bus controller also includes a number of data checking and protection features, such as data parity generation and checking, write protection, and a bus monitor to ensure that each bus cycle is terminated within a user-specified period. The local bus can operate at up to 133 MHz.

The system timers include the following features: periodic interrupt timer, real time clock, software watchdog timer, and two general-purpose timer blocks.

1.8 Security Engine

The optional security engine is optimized to handle all the algorithms associated with IPSec, IEEE 802.11i, and iSCSI. The security engine contains one crypto-channel, a controller, and a set of crypto execution units (EUs). The execution units are as follows:

- Data encryption standard execution unit (DEU), supporting DES and 3DES
- Advanced encryption standard unit (AESU), supporting AES
- Message digest execution unit (MDEU), supporting MD5, SHA1, SHA-256, and HMAC with any algorithm
- One crypto-channel supporting multi-command descriptor chains

1.9 PCI Controller

The PCI controller includes the following features:

- *PCI Specification Revision 2.3* compatible
- Single 32-bit data PCI interface operates at up to 66 MHz
- PCI 3.3-V compatible (not 5-V compatible)
- Support for host and agent modes
- On-chip arbitration, supporting 5 external masters on PCI
- Selectable hardware-enforced coherency

voltage supplies—GV_{DD}, LV_{DD}, and OV_{DD}—do not have any ordering requirements with respect to one another.

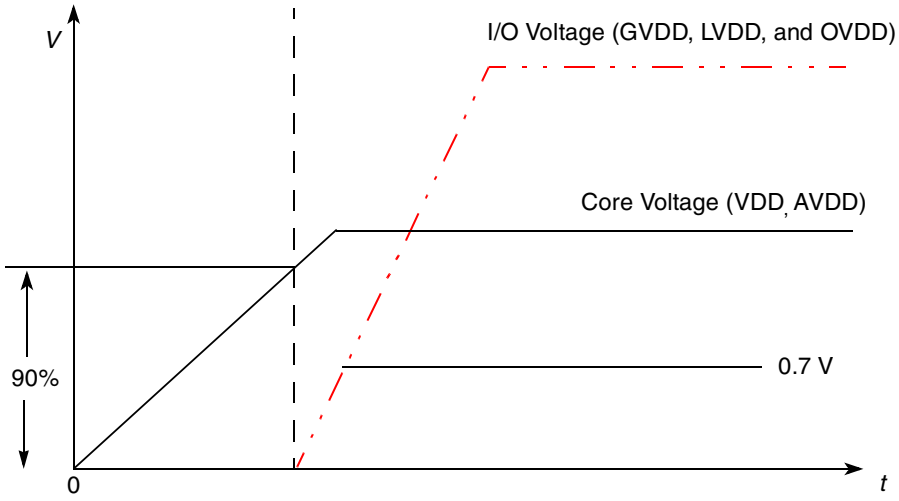

Figure 3. Power-Up Sequencing Example

Note that the SerDes power supply (L[1,2]_$n$$V_{DD}$) should follow the same timing as the core supply (V_{DD}).

The device does not require the core supply voltage and I/O supply voltages to be powered down in any particular order.

3 Power Characteristics

The estimated typical power dissipation for the chip device is shown in this table.

Table 5. Power Dissipation [1]

Core Frequency (MHz)	CSB/DDR Frequency (MHz)	Sleep Power at T_j = 65°C (W) [2]	Typical Application at T_j = 65°C (W) [2]	Typical Application at T_j = 125°C (W) [3]	Max Application at T_j = 125°C (W) [4]
333	333	1.45	1.9	3.2	3.8
	167	1.45	1.8	3.0	3.6
400	400	1.45	2.0	3.3	4.0
	266	1.45	1.9	3.1	3.8
450	300	1.45	2.0	3.2	3.8
	225	1.45	1.9	3.1	3.7
500	333	1.45	2.0	3.3	3.9
	250	1.45	1.9	3.2	3.8
533	355	1.45	2.0	3.3	4.0
	266	1.45	2.0	3.2	3.9

Table 5. Power Dissipation [1] (continued)

Core Frequency (MHz)	CSB/DDR Frequency (MHz)	Sleep Power at T_j = 65°C (W) [2]	Typical Application at T_j = 65°C (W) [2]	Typical Application at T_j = 125°C (W) [3]	Max Application at T_j = 125°C (W) [4]
600	400	1.45	2.1	3.4	4.1
	300	1.45	2.0	3.3	4.0
667	333	1.45	2.1	3.3	4.1
	266	1.45	2.0	3.3	3.9
800	400	1.45	2.5	3.8	4.3

Notes:
1. The values do not include I/O supply power (OV_{DD}, LV_{DD}, GV_{DD}) or AV_{DD}. For I/O power values, see Table 6.
2. Typical power is based on a voltage of V_{DD} = 1.0 V for core frequencies ≤ 667 MHz or V_{DD} = 1.05 V for core frequencies of 800 MHz, and running a Dhrystone benchmark application.
3. Typical power is based on a voltage of V_{DD} = 1.0 V for core frequencies ≤ 667 MHz or V_{DD} = 1.05 V for core frequencies of 800 MHz, and running a Dhrystone benchmark application.
4. Maximum power is based on a voltage of V_{DD} = 1.0 V for core frequencies ≤ 667 MHz or V_{DD} = 1.05 V for core frequencies of 800 MHz, worst case process, and running an artificial smoke test.

This table shows the estimated typical I/O power dissipation for the device.

Table 6. Typical I/O Power Dissipation

Interface	Parameter	GV_{DD} (1.8 V)	GV_{DD}/LBV_{DD} (2.5 V)	OV_{DD} (3.3 V)	LV_{DD} (3.3 V)	LV_{DD} (2.5 V)	L[1,2]_$n$$V_{DD}$ (1.0 V)	Unit	Comments
DDR I/O 65% utilization 2 pair of clocks	200 MHz data rate, 32-bit	0.28	0.35	—	—	—	—	W	—
	200 MHz data rate, 64-bit	0.41	0.49	—	—	—	—	W	
	266 MHz data rate, 32-bit	0.31	0.4	—	—	—	—	W	
	266 MHz data rate, 64-bit	0.46	0.56	—	—	—	—	W	
	300 MHz data rate, 32-bit	0.33	0.43	—	—	—	—	W	
	300 MHz data rate, 64-bit	0.48	0.6	—	—	—	—	W	
	333 MHz data rate, 32-bit	0.35	0.45	—	—	—	—	W	
	333 MHz data rate, 64-bit	0.51	0.64	—	—	—	—	W	
	400 MHz data rate, 32-bit	0.38	—	—	—	—	—	W	
	400 MHz data rate, 64-bit	0.56	—	—	—	—	—	W	

4.1 DC Electrical Characteristics

This table provides the clock input (CLKIN/PCI_CLK) DC timing specifications for the device.

Table 7. CLKIN DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit	Note
Input high voltage	—	V_{IH}	2.7	OV_{DD} + 0.3	V	1
Input low voltage	—	V_{IL}	–0.3	0.4	V	1
CLKIN Input current	0 V ≤ V_{IN} ≤ OV_{DD}	I_{IN}	—	± 10	μA	—
PCI_CLK Input current	0 V ≤ V_{IN} ≤ 0.5 V or OV_{DD} – 0.5 V ≤ V_{IN} ≤ OV_{DD}	I_{IN}	—	± 30	μA	—

Note:
1. In PCI agent mode, this specification does not comply with *PCI 2.3 Specification*.

4.2 AC Electrical Characteristics

The primary clock source for the device can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. This table provides the clock input (CLKIN/PCI_CLK) AC timing specifications for the device.

Table 8. CLKIN AC Timing Specifications

Parameter	Symbol	Min	Typical	Max	Unit	Note
CLKIN/PCI_CLK frequency	f_{CLKIN}	25	—	66.666	MHz	1, 6
CLKIN/PCI_CLK cycle time	t_{CLKIN}	15	—	40	ns	—
CLKIN/PCI_CLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	2.3	ns	2
CLKIN/PCI_CLK duty cycle	t_{KHK}/t_{CLKIN}	40	—	60	%	3
CLKIN/PCI_CLK jitter	—	—	—	± 150	ps	4, 5

Notes:
1. **Caution:** The system, core and security block must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for CLKIN/PCI_CLK are measured at 0.4 V and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter-short term and long term-and is guaranteed by design.
5. The CLKIN/PCI_CLK driver's closed loop jitter bandwidth should be < 500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track CLKIN drivers with the specified jitter.
6. Spread spectrum is allowed up to 1% down-spread on CLKIN/PCI_CLK up to 60 KHz.

5.2 RESET AC Electrical Characteristics

This table provides the reset initialization AC timing specifications of the device.

Table 11. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Note
Required assertion time of $\overline{\text{HRESET}}$ to activate reset flow	32	—	$t_{PCI\_SYNC\_IN}$	1
Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to CLKIN when the device is in PCI host mode	32	—	t_{CLKIN}	2
Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to PCI_CLK when the device is in PCI agent mode	32	—	$t_{PCI\_SYNC\_IN}$	1
$\overline{\text{HRESET}}$ assertion (output)	512	—	$t_{PCI\_SYNC\_IN}$	1
$\overline{\text{HRESET}}$ negation to negation (output)	16	—	$t_{PCI\_SYNC\_IN}$	1
Input setup time for POR config signals (CFG_RESET_SOURCE[0:3], CFG_CLKIN_DIV, and CFG_LBMUX) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI host mode	4	—	t_{CLKIN}	2
Input setup time for POR config signals (CFG_RESET_SOURCE[0:3], CFG_CLKIN_DIV, and CFG_LBMUX) with respect to negation of $\overline{\text{PORESET}}$ when the device is in PCI agent mode	4	—	$t_{PCI\_SYNC\_IN}$	1
Input hold time for POR config signals with respect to negation of $\overline{\text{HRESET}}$	0	—	ns	—
Time for the device to turn off POR config signals with respect to the assertion of $\overline{\text{HRESET}}$	—	4	ns	3
Time for the device to start driving functional output signals multiplexed with the POR configuration signals with respect to the negation of HRESET	1	—	$t_{PCI\_SYNC\_IN}$	1, 3

Notes:

1. $t_{PCI\_SYNC\_IN}$ is the clock period of the input clock applied to PCI_SYNC_IN. When the device is In PCI host mode the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. See the *MPC8379E Integrated Host Processor Reference Manual* for more details.
2. t_{CLKIN} is the clock period of the input clock applied to CLKIN. It is only valid when the device is in PCI host mode. See the *MPC8379E Integrated Host Processor Reference Manual* for more details.
3. POR config signals consists of CFG_RESET_SOURCE[0:3], CFG_LBMUX, and CFG_CLKIN_DIV.

Table 12 provides the PLL lock times.

Table 12. PLL Lock Times

Parameter	Min	Max	Unit	Note
PLL lock times	—	100	μs	—

Note:

- The device guarantees the PLL lock if the clock settings are within spec range. The core clock also depends on the core PLL ratio. See Section 23, “Clocking,” for more information.

6 DDR1 and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the chip. Note that DDR1 SDRAM is GV_{DD}(typ) = 2.5 V and DDR2 SDRAM is GV_{DD}(typ) = 1.8 V.

6.1 DDR1 and DDR2 SDRAM DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR2 SDRAM component(s) of the device when GV_{DD}(typ) = 1.8 V.

Table 13. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Parameter	Symbol	Min	Max	Unit	Note
I/O supply voltage	GV_{DD}	1.71	1.89	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2, 5
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF} + 0.140	GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.140	V	—
Output leakage current	I_{OZ}	–50	50	μA	4
Output high current (V_{OUT} = 1.40 V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.3 V)	I_{OL}	13.4	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.
5. See AN3665, “MPC837xE Design Checklist,” for proper DDR termination.

Table 14 provides the DDR2 capacitance when GV_{DD}(typ) = 1.8 V.

Table 14. DDR2 SDRAM Capacitance for GV_{DD}(typ) = 1.8 V

Parameter	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the recommended operating conditions for the DDR SDRAM component(s) when GV_{DD}(typ) = 2.5 V.

Table 15. DDR SDRAM DC Electrical Characteristics for GV_{DD} (typ) = 2.5 V

Parameter	Symbol	Min	Max	Unit	Note
I/O supply voltage	GV_{DD}	2.375	2.625	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2, 5
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF} + 0.18	GV_{DD} + 0.3	V	—

This figure shows the DDR1 and DDR2 SDRAM output timing diagram.

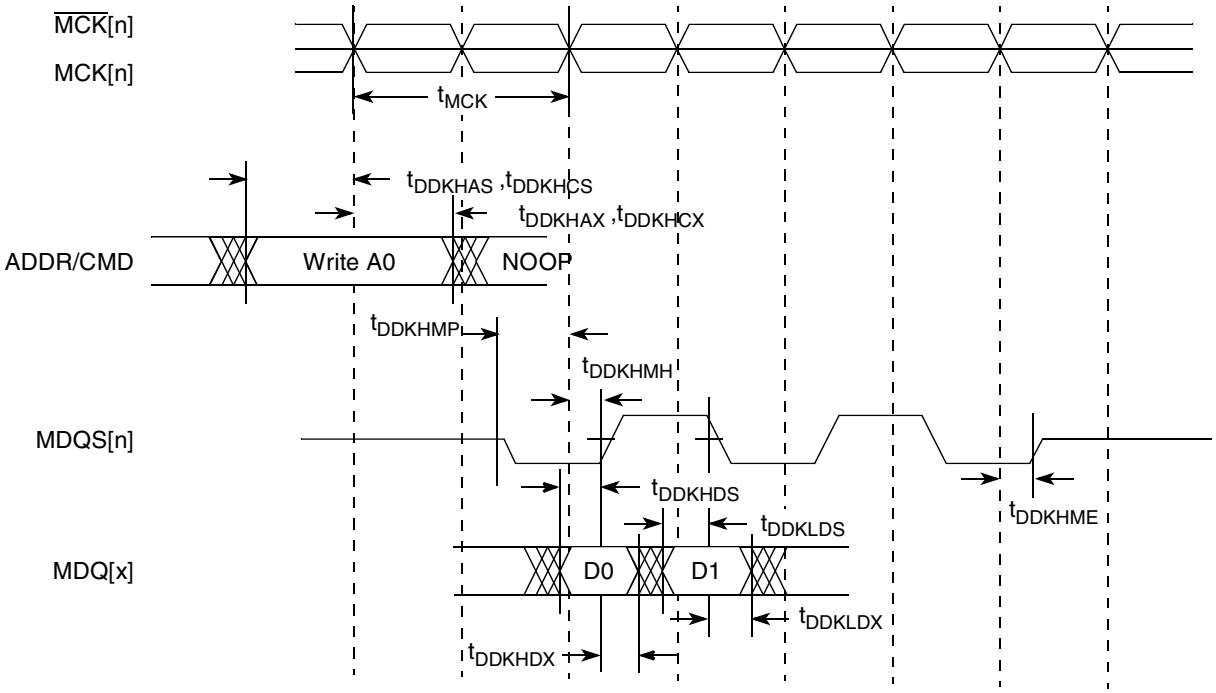

Figure 5. DDR1 and DDR2 SDRAM Output Timing Diagram

This figure provides AC test load for the DDR bus.

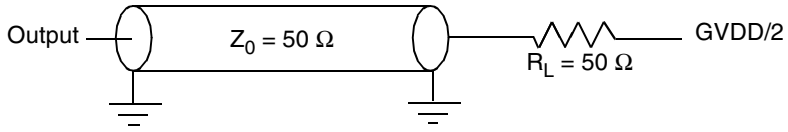

Figure 6. DDR AC Test Load

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the chip.

7.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface of the device.

Table 22. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage OV_{DD}	V_{IL}	–0.3	0.8	V
High-level output voltage, I_{OH} = –100 μA	V_{OH}	OV_{DD} – 0.2	—	V

This figure shows the MII receive AC timing diagram.

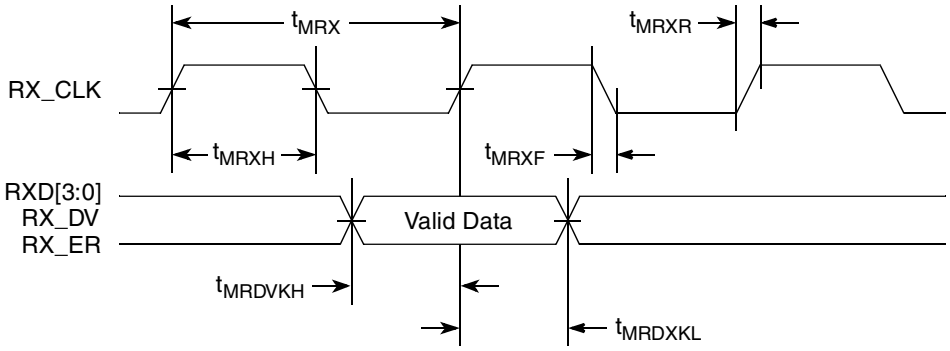

Figure 9. MII Receive AC Timing Diagram

8.2.2 RGMII and RTBI AC Timing Specifications

This table presents the RGMII and RTBI AC timing specifications.

Table 28. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

Parameter	Symbol[1]	Min	Typical	Max	Unit	Note
Data to clock output skew (at transmitter)	t_{SKRGT}	–600	0	600	ps	—
Data to clock input skew (at receiver)	t_{SKRGT}	1.0	—	2.8	ns	2
Clock period	t_{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 1000Base-T	t_{RGTH}/t_{RGT}	45	50	55	%	4
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40	50	60	%	3, 4
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns	—
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns	—
EC_GTX_CLK125 reference clock period	t_{G12}	—	8.0	—	ns	5
EC_GTX_CLK125 reference clock duty cycle measured at $0.5 \times LV_{DD1}$	t_{G125H}/t_{G125}	47	—	53	%	—

Notes:

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between
5. This symbol represents the external EC_GTX_CLK125 and does not follow the original signal naming convention.

This figure shows the MII management AC timing diagram.

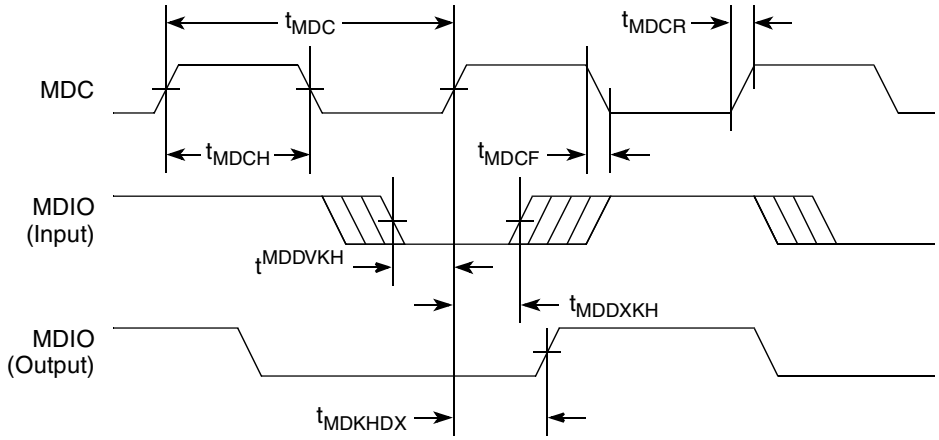

Figure 16. MII Management Interface Timing Diagram

9 USB

This section provides the AC and DC electrical characteristics for the USB dual-role controllers.

9.1 USB DC Electrical Characteristics

This table provides the DC electrical characteristics for the ULPI interface at recommended OV_{DD} = 3.3 V ± 165 mV.

Table 34. USB DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Note
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V	1
Low-level input voltage	V_{IL}	–0.3	0.8	V	1
Input current	I_{IN}	—	±30	μA	2
High-level output voltage, I_{OH} = –100 μA	V_{OH}	OV_{DD} – 0.2	—	V	—
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V	—

Notes:
1. The minimum V_{IL} and maximum V_{IH} values are based on the respective minimum and maximum OV_{IN} values found in Table 3.
2. The symbol OV_{IN} represents the input voltage of the supply and is referenced in Table 3.

Table 39. Local Bus General Timing Parameters—PLL Enable Mode (continued)

Parameter	Symbol[1]	Min	Max	Unit	Note
Local bus clock to output high impedance for LAD/LDP	t_{LBKHOZ}	—	3.8	ns	3, 8
Output hold from local bus clock for LAD/LDP	t_{LBKHOX}	1	—	ns	3

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to rising edge of LSYNC_IN at $LBV_{DD}/2$ and the $0.4 \times LBV_{DD}$ of the signal in question.
3. All signals are measured from $LBV_{DD}/2$ of the rising/falling edge of LSYNC_IN to $0.5 \times LBV_{DD}$ of the signal in question.
4. Input timings are measured at the pin.
5. $t_{LBOTOT1}$ should be used when LBCR[AHD] is set and the load on LALE output pin is at least 10pF less than the load on LAD output pins.
6. $t_{LBOTOT2}$ should be used when LBCR[AHD] is not set and the load on LALE output pin is at least 10pF less than the load on LAD output pins.
7. $t_{LBOTOT3}$ should be used when LBCR[AHD] is not set and the load on LALE output pin equals to the load on LAD output pins.
8. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

This figure provides the eSDHC clock input timing diagram.

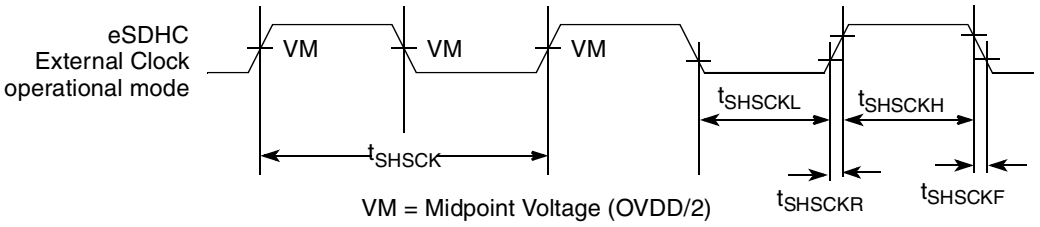

Figure 29. eSDHC Clock Input Timing Diagram

11.3.1 High-Speed Output Path (Write)

This figure provides the data and command output timing diagram.

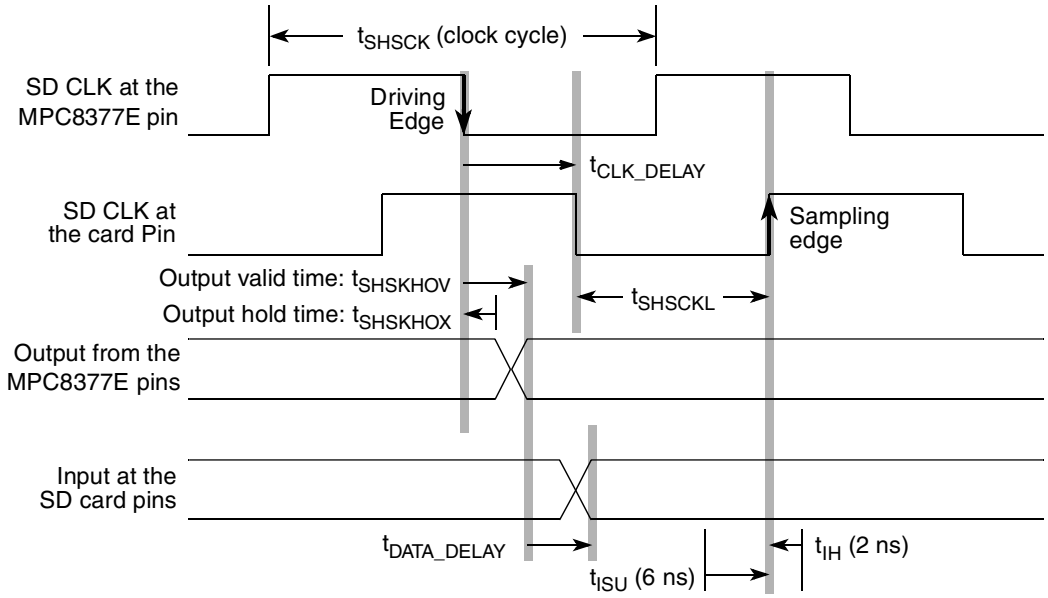

Figure 30. High Speed Output Path

11.3.1.1 High-Speed Write Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

Zero clock delay:

$$t_{SHSKHOV} + t_{DATA\_DELAY} + t_{ISU} < t_{SHSCKL} \quad \textit{Eqn. 10}$$

With clock delay:

$$t_{SHSKHOV} + t_{DATA\_DELAY} + t_{ISU} < t_{SHSCKL} + t_{CLK\_DELAY} \quad \textit{Eqn. 11}$$

$$t_{DATA\_DELAY} - t_{CLK\_DELAY} < t_{SHSCKL} - t_{ISU} - t_{SHSKHOV} \quad \textit{Eqn. 12}$$

This figure provides the AC test load for PCI.

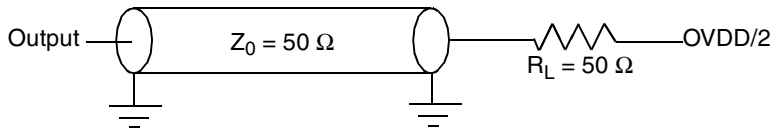

Figure 39. PCI AC Test Load

This figure shows the PCI input AC timing conditions.

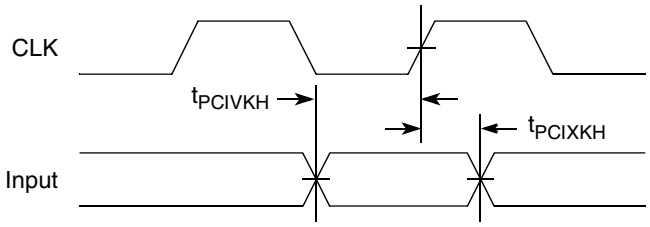

Figure 40. PCI Input AC Timing Measurement Conditions

This figure shows the PCI output AC timing conditions.

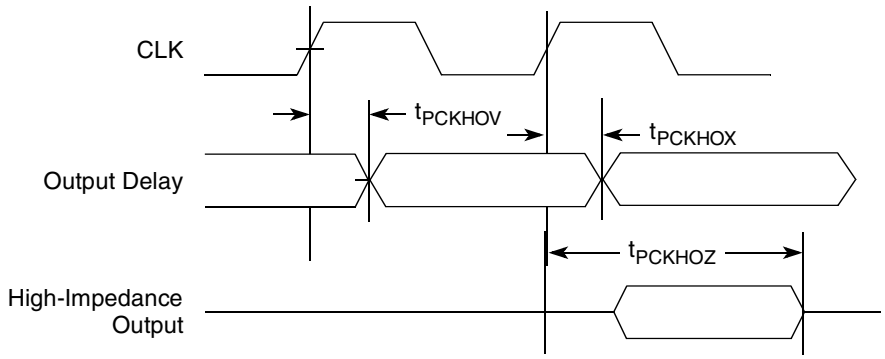

Figure 41. PCI Output AC Timing Measurement Condition

15 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus.

15.1 DC Requirements for PCI Express SD_REF_CLK and SD_REF_CLK

For more information see Section 21, “High-Speed Serial Interfaces (HSSI).”

15.2 AC Requirements for PCI Express SerDes Clocks

This table lists the PCI Express SerDes clock AC requirements.

Table 51. SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ AC Requirements

Parameter	Symbol	Min	Typical	Max	Unit	Note
REFCLK cycle time	t_{REF}	—	10	—	ns	—
REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles.	t_{REFCJ}	—	—	100	ps	—
REFCLK phase jitter peak-to-peak. Deviation in edge location with respect to mean edge location.	t_{REFPJ}	–50	—	+50	ps	—
SD_REF_CLK/_B cycle to cycle clock jitter (period jitter)	t_{CKCJ}	—	—	100	ps	—
SD_REF_CLK/_B phase jitter peak-to-peak. Deviation in edge location with respect to mean edge location.	t_{CKPJ}	–50	—	+50	ps	2, 3

Notes:
1. All options provide serial interface bit rate of 1.5 and 3.0 Gbps.
2. In a frequency band from 150 kHz to 15 MHz, at BER of 10^{-12}.
3. Total peak-to-peak Deterministic Jitter "J_D" should be less than or equal to 50 ps.

15.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

15.4 Physical Layer Specifications

Following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the transport and data link layer, use the *PCI Express Base Specification*, Rev. 1.0a.

NOTE

The voltage levels of the transmitter and the receiver depend on the SerDes control registers which should be programmed at the recommended values for PCI Express protocol (that is, L1_nV$_{DD}$ = 1.0 V).

The eye diagram must be valid for any 250 consecutive UIs.

A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI.

NOTE

It is recommended that the recovered Tx UI be calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (that is, least squares and median deviation fits).

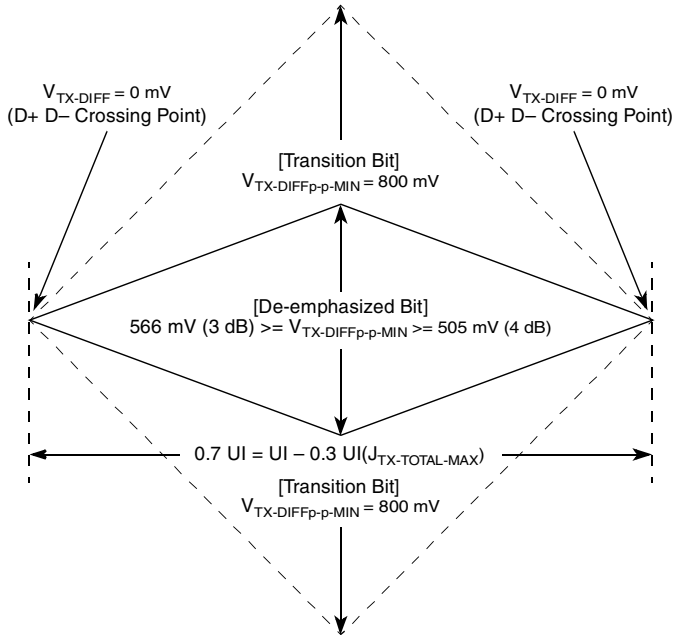

Figure 42. Minimum Transmitter Timing and Voltage Output Compliance Specifications

15.4.3 Differential Receiver (Rx) Input Specifications

This table defines the specifications for the differential input at all receivers. The parameters are specified at the component pins.

Table 53. Differential Receiver (Rx) Input Specifications

Parameter	Comments	Symbol	Min	Typical	Max	Units	Note
Unit interval	Each U_{PERX} is 400 ps ± 300 ppm. U_{PERX} does not account for Spread Spectrum Clock dictated variations.	UI	399.88	400	400.12	ps	1
Differential peak-to-peak output voltage	$V_{PEDPPRX} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$	$V_{RX-DIFFp-p}$	0.175	—	1.200	V	2

17 Timers

This section describes the DC and AC electrical specifications for the timers of the chip.

17.1 Timers DC Electrical Characteristics

This table provides the DC electrical characteristics for the device timers pins, including TIN, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$, and RTC_CLK.

Table 63. Timers DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Output high voltage	I_{OH} = –6.0 mA	V_{OH}	2.4	—	V
Output low voltage	I_{OL} = 6.0 mA	V_{OL}	—	0.5	V
Output low voltage	I_{OL} = 3.2 mA	V_{OL}	—	0.4	V
Input high voltage	—	V_{IH}	2.0	OV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.8	V
Input current	0 V ≤ V_{IN} ≤ OV_{DD}	I_{IN}	—	± 30	μA

17.2 Timers AC Timing Specifications

This table provides the timers input and output AC timing specifications.

Table 64. Timers Input AC Timing Specifications[1]

Parameter	Symbol [2]	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs should be synchronized before use by any external synchronous logic. Timers inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation

This figure provides the AC test load for the timers.

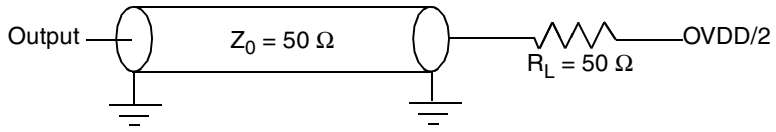

Figure 46. Timers AC Test Load

18 GPIO

This section describes the DC and AC electrical specifications for the GPIO of the chip.

18.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for the device GPIO.

Table 65. GPIO DC Electrical Characteristics

This specification applies when operating at 3.3 V ± 165 mV supply.

Parameter	Condition	Symbol	Min	Max	Unit
Output high voltage	I_{OH} = –6.0 mA	V_{OH}	2.4	—	V
Output low voltage	I_{OL} = 6.0 mA	V_{OL}	—	0.5	V
Output low voltage	I_{OL} = 3.2 mA	V_{OL}	—	0.4	V
Input high voltage	—	V_{IH}	2.0	OV_{DD} + 0.3	V
Input low voltage	—	V_{IL}	–0.3	0.8	V
Input current	0 V ≤ V_{IN} ≤ OV_{DD}	I_{IN}	—	± 30	μA

18.2 GPIO AC Timing Specifications

This table provides the GPIO input and output AC timing specifications.

Table 66. GPIO Input AC Timing Specifications

Parameter	Symbol	Min	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of SYS_CLKIN. Timings are measured at the pin.
2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

This figure provides the AC test load for the GPIO.

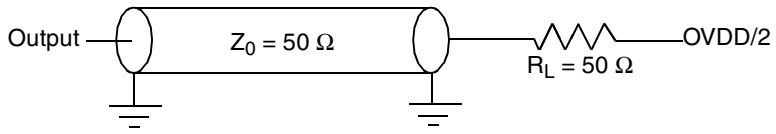

Figure 47. GPIO AC Test Load

19 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins of the chip.

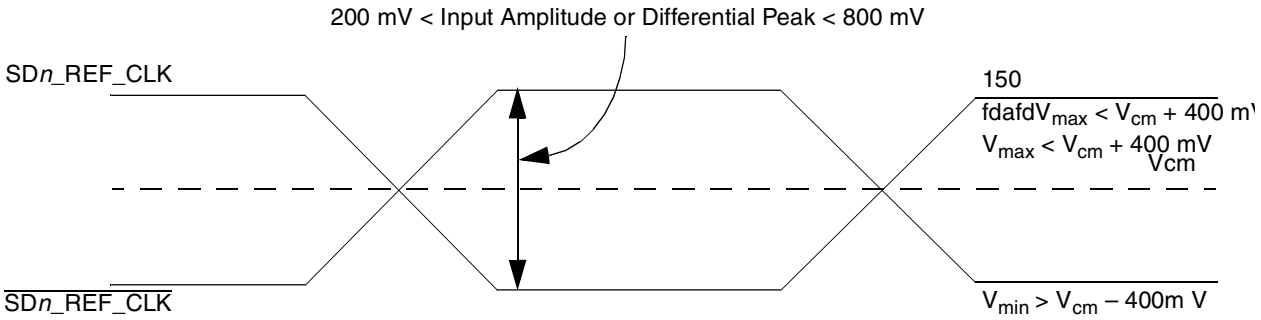

Figure 54. Differential Reference Clock Input DC Requirements (External AC-Coupled)

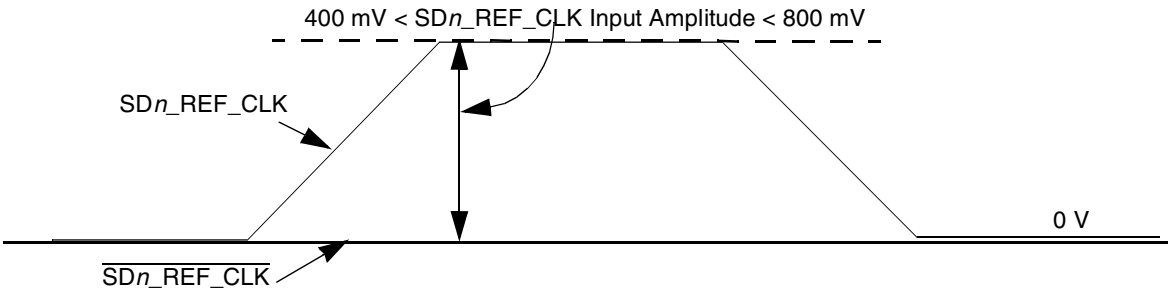

Figure 55. Single-Ended Reference Clock Input DC Requirements

21.2.3 Interfacing With Other Differential Signaling Levels

The following list provides information about interfacing with other differential signaling levels.

- With on-chip termination to SGND_SRDS*n* (xcorevss), the differential reference clocks inputs are HCSL (high-speed current steering logic) compatible DC-coupled.
- Many other low voltage differential type outputs like LVDS (low voltage differential signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 mV to 400 mV) for DC-coupled connection.
- LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

occurs in the 1–15 MHz range. The source impedance of the clock driver should be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

This table describes some AC parameters for PCI Express .

Table 71. SerDes Reference Clock Common AC Parameters

At recommended operating conditions with XV_{DD_SRDS} or XV_{DD_SRDS} = 1.0 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Note
Rising Edge Rate	Rise Edge Rate	1.0	4.0	V/ns	2, 3
Falling Edge Rate	Fall Edge Rate	1.0	4.0	V/ns	2, 3
Differential Input High Voltage	V_{IH}	200	—	mV	2
Differential Input Low Voltage	V_{IL}	—	–200	mV	2
Rising edge rate (SD*n*_REF_CLK) to falling edge rate ($\overline{\text{SD}n\text{\_REF\_CLK}}$) matching	Rise-Fall Matching	—	20	%	1, 4

Notes:

1. Measurement taken from single ended waveform.
2. Measurement taken from differential waveform.
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SD*n*_REF_CLK minus $\overline{\text{SD}n\text{\_REF\_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 60.
4. Matching applies to rising edge rate for SD*n*_REF_CLK and falling edge rate for $\overline{\text{SD}n\text{\_REF\_CLK}}$. It is measured using a 200 mV window centered on the median cross point where SDn_REF_CLK rising meets $\overline{\text{SD}n\text{\_REF\_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of SD*n*_REF_CLK should be compared to the Fall Edge Rate of $\overline{\text{SD}n\text{\_REF\_CLK}}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 61.

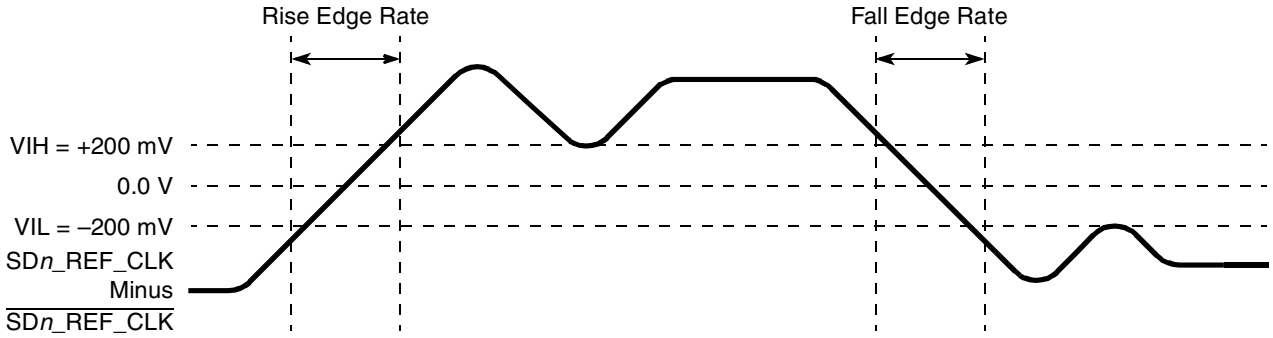

Figure 60. Differential Measurement Points for Rise and Fall Time

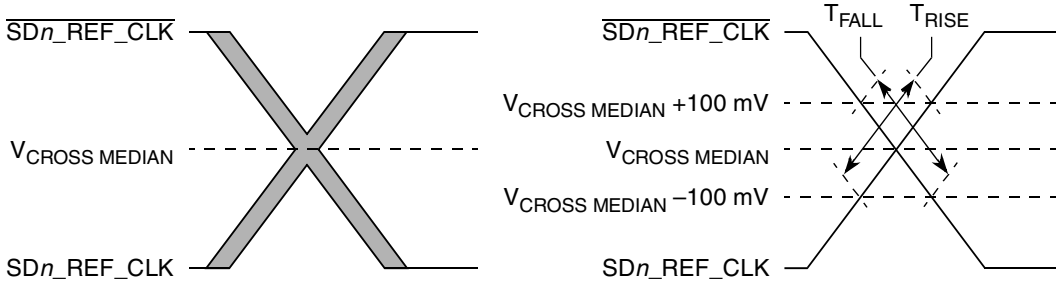

Figure 61. Single-Ended Measurement Points for Rise and Fall Time Matching

Table 72. TePBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
LA25/LAD30	D29	I/O	LBVDD	—
LA26/LAD31	E20	I/O	LBVDD	—
LA27	H26	O	LBVDD	—
LA28	C29	O	LBVDD	—
LA29	E28	O	LBVDD	—
LA30	B26	O	LBVDD	—
LA31	J25	O	LBVDD	—
LA10/LALE	H29	O	LBVDD	—
LBCTL	A22	O	LBVDD	—
LCLK0	B22	O	LBVDD	—
LCLK1	C23	O	LBVDD	—
LCLK2	B23	O	LBVDD	—
LCS_B0	D25	O	LBVDD	—
LCS_B1	F19	O	LBVDD	—
LCS_B2	C27	O	LBVDD	—
LCS_B3	D24	O	LBVDD	—
LCS_B4/LDP0	C24	I/O	LBVDD	—
LCS_B5/LDP1	B29	I/O	LBVDD	—
LA7/LCS_B6/LDP2	E29	I/O	LBVDD	—
LA8/LCS_B7/LDP3	F29	I/O	LBVDD	—
LFCLE/LGPL0	D21	O	LBVDD	—
LFALE/LGPL1	A26	O	LBVDD	—
LFRE_B/LGPL2/LOE_B	F22	O	LBVDD	—
LFWP_B/LGPL3	C21	O	LBVDD	—
LGPL4/LFRB_B/LGTA_B/ LUPWAIT/LPBSE	J29	I/O	LBVDD	16
LA9/LGPL5	G29	O	LBVDD	—
LSYNC_IN	A21	I	LBVDD	—
LSYNC_OUT	D23	O	LBVDD	—
LWE_B0/LFWE0/LBS_B0	E22	O	LBVDD	—
LWE_B1/LFWE1/LBS_B1	B25	O	LBVDD	—
LWE_B2/LFWE2/LBS_B2	E27	O	LBVDD	—
LWE_B3/LFWE3/LBS_B3	F28	O	LBVDD	—

Table 87. Document Revision History (continued)

Revision	Date	Substantive Change(s)
6	07/2011	In Section 2.2, "Power Sequencing," updated power down sequencing information.
5	07/2011	• In Table 2, "Absolute Maximum Ratings[1]," removed footnote 5 from LB_{IN} to OV_{IN}. Also, corrected footnote 5. • In Table 3, "Recommended Operating Conditions," added footnote 2 to AV_{DD}. • In Figure 2, "Overshoot/Undershoot Voltage for $GV_{DD}/LV_{DD}/OV_{DD}/LBV_{DD}$," added LBV_{DD}. • In Table 13, "DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V," updated I_{OZ} min/max to –50/50. • In Figure 11, "RGMII and RTBI AC Timing and Multiplexing Diagrams," added distinction between t_{SKRGT_RX} and t_{SKRGT_TX} signals. • In Table 33, "MII Management AC Timing Specifications," updated MDC frequency—removed Min and Max values, added Typical value. Also, updated footnote 2 and removed footnote 3. • In Table 48, "PCI DC Electrical Characteristics," updated V_{IH} min value to 2.0. • In Table 72, "TePBGA II Pinout Listing," added Note to LGPL4/LFRB_B/LGTA_B/LUPWAIT/LPBSE (to be consistent with AN3665, "MPC837xE Design Checklist." • In Table 74, "Operating Frequencies for TePBGA II," added Minimum Operating Frequency for eTSEC, and corrected DDR2 Minimum and Maximum Operating Frequency values.
4	11/2010	• In Table 25, "RGMII and RTBI DC Electrical Characteristics," updated V_{IH} min value to 1.7. • In Table 40, "Local Bus General Timing Parameters—PLL Bypass Mode," added row for t_{LBKHLR}. • In Section 10.2, "Local Bus AC Electrical Specifications," and in Section 23, "Clocking," updated LCCR to LCRR. • In Table 72, "TePBGA II Pinout Listing," added SD_WP to pin C9. Also clarified TEST_SEL0 and TEST_SEL1 pins—no change in functionality.
3	03/2010	• Added Section 4.3, "eTSEC Gigabit Reference Clock Timing." • In Table 34, "USB DC Electrical Characteristics," and Table 35, "USB General Timing Parameters (ULPI Mode Only)," added table footnotes . • In Table 39, "Local Bus General Timing Parameters—PLL Enable Mode," and Table 40, "Local Bus General Timing Parameters—PLL Bypass Mode," corrected footnotes for $t_{LBOTOT1}$, $t_{LBOTOT2}$, $t_{LBOTOT3}$. • In Figure 22, "Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2 (PLL Enable Mode)," and Figure 24, "Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4 (PLL Enable Mode)," shifted "Input Signals: LAD[0:31]/LDP[0:3]" from the falling edge to the rising edge of LSYNC_IN. • In Figure 63, "Mechanical Dimensions and Bottom Surface Nomenclature of the TEPBGA II," added heat spreader. • In Section 25.6, "Pull-Up Resistor Requirements," removed "Ethernet Management MDIO pin" from list of open drain type pins. • In Table 72, "TePBGA II Pinout Listing," updated the Pin Type column for AVDD_C, AVDD_L, and AVDD_P pins. • in Table 72, "TePBGA II Pinout Listing," added Note 16 to eTSEC pins. • In Table 77, "CSB Frequency Options for Host Mode," and Table 78, "CSB Frequency Options for Agent Mode," updated *csb_clk* frequencies available. • In Table 84, "Part Numbering Nomenclature," removed footnote to "e300 core Frequency."