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NXP USA Inc. - MPC8377ECVRALG Datasheet



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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300c4s
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	667MHz
Co-Processors/DSP	Security; SEC 3.0
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 125°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	689-BBGA Exposed Pad
Supplier Device Package	689-TEPBGA II (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8377ecvralg

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Characteristic		Symbol	Max Value	Unit	Note
Input voltage	DDR DRAM signals	MV _{IN}	–0.3 to (GV _{DD} + 0.3)	V	2, 4
	DDR DRAM reference	MV _{REF}	–0.3 to (GV _{DD} + 0.3)	V	2, 4
Three-speed Ethernet signals		LV _{IN}	–0.3 to (LV _{DD} + 0.3)	V	
	PCI, DUART, CLKIN, system control and power management, I ² C, and JTAG signals	OV _{IN}	–0.3 to (OV _{DD} + 0.3)	V	3, 4, 5
	Local Bus	LB _{IN}	–0.3 to (LBV _{DD} + 0.3)	V	_
Storage temperature range		T _{STG}	–55 to 150	°C	_

Table 2. Absolute Maximum Ratings¹ (continued)

Notes:

- 1. Functional and tested operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
- 2. Caution: MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- 3. Caution: OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- 4. (M,O)V_{IN} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
- 5. Overshoot/undershoot by OV_{IN} on the PCI interface does not comply to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 2.
- 6. L[1,2]_nV_{DD} includes SDAV_{DD_0}, XCOREV_{DD}, and XPADV_{DD} power inputs.

2.1.2 Power Supply Voltage Specification

This table provides recommended operating conditions for the device. Note that the values in this table are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Characteristic	Symbol	Recommended Value	Unit	Note	
Core supply voltage	up to 667 MHz	V _{DD}	1.0 ± 50 mV	V	1
	800 MHz		1.05 ± 50 mV	V	1
PLL supply voltage (e300 core, eLBC and	up to 667 MHz	AV _{DD}	1.0 ± 50 mV	V	1, 2
system)	800 MHz		1.05 ± 50 mV	۷	1, 2
DDR1 and DDR2 DRAM I/O voltage	GV _{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	1	
Three-speed Ethernet I/O, MII management volta	LV _{DD} [1,2]	3.3 V ± 165 mV 2.5 V ± 125 mV	V	_	
PCI, local bus, DUART, system control and power JTAG I/O voltage	OV _{DD}	3.3 V ± 165 mV	V	1	
Local Bus	LBV _{DD}	1.8 V ± 90 mV 2.5 V ± 125 mV 3.3 V ± 165 mV	V		

Table 3. Recommended Operating Conditions

5.2 **RESET AC Electrical Characteristics**

This table provides the reset initialization AC timing specifications of the device.

Parameter/Condition	Min	Max	Unit	Note
Required assertion time of HRESET to activate reset flow	32	—	t _{PCI_SYNC_IN}	1
Required assertion time of $\overline{\text{PORESET}}$ with stable clock applied to CLKIN when the device is in PCI host mode	32	_	t _{CLKIN}	2
Required assertion time of PORESET with stable clock applied to PCI_CLK when the device is in PCI agent mode	32	—	t _{PCI_SYNC_IN}	1
HRESET assertion (output)	512	_	t _{PCI_SYNC_IN}	1
HRESET negation to negation (output)	16	—	t _{PCI_SYNC_IN}	1
Input setup time for POR config signals (CFG_RESET_SOURCE[0:3], CFG_CLKIN_DIV, and CFG_LBMUX) with respect to negation of PORESET when the device is in PCI host mode	4	—	^t CLKIN	2
Input setup time for POR config signals (CFG_RESET_SOURCE[0:3], CFG_CLKIN_DIV, and CFG_LBMUX) with respect to negation of PORESET when the device is in PCI agent mode	4	—	^t PCI_SYNC_IN	1
Input hold time for POR config signals with respect to negation of HRESET	0	—	ns	_
Time for the device to turn off POR config signals with respect to the assertion of \overrightarrow{HRESET}	_	4	ns	3
Time for the device to start driving functional output signals multiplexed with the POR configuration signals with respect to the negation of HRESET	1	_	t _{PCI_SYNC_IN}	1, 3

Table 11. RESET Initialization Timing Specifications

Notes:

1. t_{PCI_SYNC_IN} is the clock period of the input clock applied to PCI_SYNC_IN. When the device is In PCI host mode the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. See the *MPC8379E Integrated Host Processor Reference Manual* for more details.

2. t_{CLKIN} is the clock period of the input clock applied to CLKIN. It is only valid when the device is in PCI host mode. See the *MPC8379E Integrated Host Processor Reference Manual* for more details.

3. POR config signals consists of CFG_RESET_SOURCE[0:3], CFG_LBMUX, and CFG_CLKIN_DIV.

Table 12 provides the PLL lock times.

Table 12. PLL Lock Times

Parameter	Min	Мах	Unit	Note
PLL lock times		100	μs	_

Note:

• The device guarantees the PLL lock if the clock settings are within spec range. The core clock also depends on the core PLL ratio. See Section 23, "Clocking," for more information.

6 DDR1 and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the chip. Note that DDR1 SDRAM is $GV_{DD}(typ) = 2.5 \text{ V}$ and DDR2 SDRAM is $GV_{DD}(typ) = 1.8 \text{ V}$.

6.1 DDR1 and DDR2 SDRAM DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR2 SDRAM component(s) of the device when $GV_{DD}(typ) = 1.8 \text{ V}.$

Parameter	Symbol	Min	Мах	Unit	Note
I/O supply voltage	GV _{DD}	1.71	1.89	V	1
I/O reference voltage	MV _{REF}	$0.49 imes GV_{DD}$	$0.51 imes GV_{DD}$	V	2, 5
I/O termination voltage	V _{TT}	MV _{REF} – 0.04	MV _{REF} + 0.04	V	3
Input high voltage	V _{IH}	MV _{REF} + 0.140	GV _{DD} + 0.3	V	_
Input low voltage	V _{IL}	-0.3	MV _{REF} – 0.140	V	_
Output leakage current	I _{OZ}	-50	50	μA	4
Output high current (V _{OUT} = 1.40 V)	I _{ОН}	-13.4	—	mA	_
Output low current (V _{OUT} = 0.3 V)	I _{OL}	13.4	_	mA	

Table 13. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.

2. MV_{REF} is expected to be equal to $0.5 \times GV_{DD}$, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.

3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.

4. Output leakage is measured with all outputs disabled, $0 V \le V_{OUT} \le GV_{DD}$.

5. See AN3665, "MPC837xE Design Checklist," for proper DDR termination.

Table 14 provides the DDR2 capacitance when $GV_{DD}(typ) = 1.8$ V.

Table 14. DDR2 SDRAM Capacitance for GV_{DD}(typ) = 1.8 V

Parameter	Symbol	Min	Мах	Unit	Note
Input/output capacitance: DQ, DQS, DQS	C _{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, \overline{DQS}	C _{DIO}	—	0.5	pF	1

Note:

1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, V_{OUT} = $GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the recommended operating conditions for the DDR SDRAM component(s) when $GV_{DD}(typ) = 2.5 \text{ V}.$

Table 15. DDR SDRAM DC Electrical Characteristics for GV_{DD} (typ) = 2.5 V

Parameter	Symbol	Min	Мах	Unit	Note
I/O supply voltage	GV _{DD}	2.375	2.625	V	1
I/O reference voltage	MV _{REF}	$0.49 imes GV_{DD}$	$0.51 imes GV_{DD}$	V	2, 5
I/O termination voltage	V _{TT}	MV _{REF} – 0.04	MV _{REF} + 0.04	V	3
Input high voltage	V _{IH}	MV _{REF} + 0.18	GV _{DD} + 0.3	V	

Parameter	Symbol	Min	Мах	Unit
Low-level output voltage, $I_{OL} = 100 \ \mu A$	V _{OL}	_	0.2	V
Input current, (0 $V \leq V_{IN} \leq OV_{DD}$)	I _{IN}	—	±30	μΑ

Table 22. DUART DC Electrical Characteristics (continued)

Note: The symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 2.

7.2 DUART AC Electrical Specifications

this table provides the AC timing parameters for the DUART interface of the device.

Table 23. DUART AC Timing Specifications

Parameter	Value	Unit	Note
Minimum baud rate	256	baud	—
Maximum baud rate	> 1,000,000	baud	1
Oversample rate	16	_	2

Notes:

1. Actual attainable baud rate will be limited by the latency of interrupt processing.

2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

8 Ethernet: Enhanced Three-Speed Ethernet (eTSEC)

This section provides the AC and DC electrical characteristics for the enhanced three-speed Ethernet controller.

8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—MII/RGMII/RTBI/RMII DC Electrical Characteristics

The electrical characteristics specified here apply to media independent interface (MII), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), reduced media independent interface (RMII) signals, management data input/output (MDIO) and management data clock (MDC).

The MII and RMII interfaces are defined for 3.3 V, while the RGMII and RTBI interfaces can be operated at 2.5 V. The RGMII and RTBI interfaces follow the *Reduced Gigabit Media-Independent Interface* (*RGMII*) Specification Version 1.3. The RMII interface follows the *RMII Consortium RMII Specification Version 1.2*.

Parameter	Conditions		Symbol	Min	Мах	Unit
Supply voltage (3.3 V)	-	LV _{DD1}	3.135	3.465	V	
Output high voltage	I _{OH} = -1.0 mA	LV _{DD1} = Min	V _{OH}	2.10	LV _{DD1} + 0.3	V
Output low voltage	I _{OL} = 1.0 mA LV _{DD1} = Min		V _{OL}	GND	0.50	V
Input high voltage	-	V _{IH}	2.00	—	V	
Input low voltage	-	_	V _{IL}	—	0.80	V
Input high current	LV _{DD1} = Max	V _{IN} ¹ = 2.1 V	I _{IH}	—	30	μA
Input low current	LV _{DD1} = Max	V _{IN} = 0.5 V	Ι _{ΙL}	-600	—	μA

Table 32. MII Management DC Electrical Characteristics When Powered at 3.3 V

8.3.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

Table 33. MII Management AC Timing Specifications

Parameter	Symbol ¹	Min	Typical	Мах	Unit	Note
MDC frequency	f _{MDC}	—	2.5	—	MHz	2
MDC period	t _{MDC}	80	_	400	ns	
MDC clock pulse width high	t _{MDCH}	32	_	_	ns	
MDC to MDIO valid	t _{MDKHDV}	$2 \times (t_{plb_clk} \times 8)$	—	—	ns	4
MDC to MDIO delay	t _{MDKHDX}	10	—	$2 \times (t_{\text{plb}clk} \times 8)$	ns	2, 4
MDIO to MDC setup time	t _{MDDVKH}	5	—	—	ns	
MDIO to MDC hold time	t _{MDDXKH}	0	—	—	ns	_
MDC rise time (20%-80%)	t _{MDCR}	—	—	10	ns	3
MDC fall time (80%–20%)	t _{MDCF}	_	—	10	ns	3

Notes:

 The symbols used for timing specifications herein follow the pattern of t_{(first two letters of functional block)(signal)(state)} (reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2. This parameter is dependent on the system clock speed.

3. Guaranteed by design.

4. t_{plb_clk} is the platform (CSB) clock divided according to the SCCR[TSEC1CM].

Table 38. Local Bus DC Electrical Characteristics (LBV_{DD} = 1.8 V)

At recommended operating conditions with $LBV_{DD} = 1.8$ V.

Parameter	Cond	itions	Symbol	Min	Мах	Unit
Supply voltage 1.8 V	-	_	LBV _{DD}	1.71	1.89	V
Output high voltage	I _{OH} = -1.0 mA	LBV _{DD} = Min	V _{OH}	LBV _{DD} - 0.45	—	V
Output low voltage	I _{OL} = 1.0 mA	LBV _{DD} = Min	V _{OL}	—	0.45	V
Input high voltage	_	LBV _{DD} = Min	V _{IH}	$0.65 imes LBV_{DD}$	LBV _{DD} + 0.3	V
Input low voltage	_	LBV _{DD} = Min	V _{IL}	-0.3	$0.35 imes LBV_{DD}$	V
Input high current	$V_{IN}^{1} = LBV_{DD}$		I _{IH}	—	10	μA
Input low current	V _{IN} ¹ = GND		١ _{IL}	-10	—	μA

10.2 Local Bus AC Electrical Specifications

This table describes the general timing parameters of the local bus interface of the device when in PLL enable mode.

Parameter	Symbol ¹	Min	Max	Unit	Note
Local bus cycle time	t _{LBK}	7.5	15	ns	2
Input setup to local bus clock (except LUPWAIT/LGTA)	t _{LBIVKH}	1.5	—	ns	3, 4
Input hold from local bus clock	t _{LBIXKH}	1.0	—	ns	3, 4
LUPWAIT/LGTA input setup to local bus clock	t _{LBIVKH1}	1.5	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	t _{LBOTOT1}	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	t _{LBOTOT2}	3	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	t _{LBOTOT3}	2.5	—	ns	7
Local bus clock to LALE rise	t _{LBKHLR}	—	4.5	ns	—
Local bus clock to output valid (except LALE)	t _{LBKHOV}	—	4.5	ns	3

Table 39. Local Bus General Timing Parameters—PLL Enable Mode

This figure provides the eSDHC clock input timing diagram.



Figure 29. eSDHC Clock Input Timing Diagram

11.3.1 High-Speed Output Path (Write)

This figure provides the data and command output timing diagram.



Figure 30. High Speed Output Path

11.3.1.1 High-Speed Write Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

Zero clock delay:

$$t_{SHSKHOV} + t_{DATA_{DELAY}} + t_{ISU} < t_{SHSCKL}$$
 Eqn. 10

With clock delay:

This means that data delay should be equal or less than the clock delay in the ideal case where $t_{SHSCLKL} = 10$ ns:

```
t_{DATA\_DELAY} - t_{CLK\_DELAY} < 10 - 6 - 4t_{DATA\_DELAY} - t_{CLK\_DELAY} < 0
```

11.3.1.2 High-Speed Write Meeting Hold (Minimum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

```
t_{CLK\_DELAY} < t_{SHSCKL} + t_{SHSKHOX} + t_{DATA\_DELAY} - t_{IH} Eqn. 13
```

$$t_{CLK_DELAY} - t_{DATA_DELAY} < t_{SHSCKL} + t_{SHSKHOX} - t_{IH}$$
 Eqn. 14

This means that clock can be delayed versus data up to 8 ns (external delay line) in ideal case of $t_{SHSCLKL} = 10$ ns:

```
t_{CLK\_DELAY} - t_{DATA\_DELAY} < 10 + 0 - 2
t_{CLK\_DELAY} - t_{DATA\_DELAY} < 8
```

11.3.2 High-Speed Input Path (Read)

This figure provides the data and command input timing diagram.



Figure 31. High-Speed Input Path

For the input path, the device eSDHC expects to sample the data 1.5 internal clock cycles after it was driven by the SD card. Since in this mode the SD card drives the data at the rising edge of the clock, a sufficient delay to the clock and the data must exist to ensure it will not be sampled at the wrong internal

	-					
Parameter	Symbol	Min	Typical	Мах	Units	Note
Total jitter $f_{C3dB} = f_{BAUD}/1667$	U _{SATA_TXTJfB/1667}	_	—	0.55	UI _{p-p}	1
Deterministic jitter $f_{C3dB} = f_{BAUD}/10$	U _{SATA_TXDJfB/10}	_	_	0.17	UI _{p-p}	1
Deterministic jitter $f_{C3dB} = f_{BAUD}/500$	U _{SATA_TXDJfB/500}	_	—	0.19	UI _{p-p}	1
Deterministic jitter $f_{C3dB} = f_{BAUD}/1667$	U _{SATA_TXDJfB/1667}	—	—	0.35	UI _{p-p}	1

Table 58. Gen 2i/3G Transmitter AC Specifications (continued)

Note:

1. Measured at Tx output pins peak to peak phase variation, random data pattern.

16.3 Differential Receiver (Rx) Input Characteristics

This section discusses the Gen1i/1.5G and Gen2i/3G differential receiver input AC characteristics.

16.3.1 Gen1i/1.5G Receiver Specifications

This table provides the Gen1i or 1.5 Gbits/s differential receiver input DC characteristics for the SATA interface.

Table 59. Gen1i/1.5G Receiver Input DC Specifications

Parameter	Symbol	Min	Typical	Мах	Units	Note
Differential input voltage	V _{SATA_RXDIFF}	240	500	600	mV _{p-p}	1
Differential Rx input impedance	Z _{SATA_RXSEIM}	85	100	115	Ω	

Note:

1. Voltage relative to common of either signal comprising a differential pair.

This table provides the Gen1i or 1.5 Gbits/s differential receiver input AC characteristics for the SATA interface.

Table 60. Gen 1i/1.5G Receiver AC Specifications

Parameter	Symbol	Min	Typical	Мах	Units	Note
Unit interval	Τ _{UI}	666.4333	666.667	670.2333	ps	_
Total jitter, data-data 5 UI	U _{SATA_TXTJ5UI}	_	—	0.43	UI _{p-p}	1
Total jitter, data-data 250 UI	U _{SATA_TXTJ250UI}	_	_	0.60	UI _{p-p}	1
Deterministic jitter, data-data 5 UI	U _{SATA_TXDJ5UI}	_	_	0.25	UI _{p-p}	1

19.1 IPIC DC Electrical Characteristics

This table provides the DC electrical characteristics for the external interrupt pins of the chip.

Parameter	Condition	Symbol	Min	Мах	Unit
Input high voltage	—	V _{IH}	2.0	OV _{DD} + 0.3	V
Input low voltage	—	V _{IL}	-0.3	0.8	V
Input current	—	I _{IN}	—	±30	μA
Output low voltage	I _{OL} = 6.0 mA	V _{OL}	—	0.5	V
Output low voltage	I _{OL} = 3.2 mA	V _{OL}	—	0.4	V

Table 67. IPIC DC Electrical Characteristics

Note:

1. This table applies for pins IRQ[0:7], IRQ_OUT, MCP_OUT.

2. IRQ_OUT and MCP_OUT are open drain pins, thus V_{OH} is not relevant for those pins.

19.2 IPIC AC Timing Specifications

This table provides the IPIC input and output AC timing specifications.

Table 68. IPIC Input AC Timing Specifications

Parameter	Symbol	Min	Unit
IPIC inputs—minimum pulse width	t _{PIWID}	20	ns

Note:

- 1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
- 2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.

20 SPI

This section describes the DC and AC electrical specifications for the SPI of the chip.

20.1 SPI DC Electrical Characteristics

This table provides the DC electrical characteristics for the device SPI.

Table 69. SPI DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Мах	Unit
Input high voltage	—	V _{IH}	2.0	OV _{DD} + 0.3	V
Input low voltage	—	V _{IL}	-0.3	0.8	V
Input current	—	I _{IN}		± 30	μA
Output high voltage	I _{OH} = -8.0 mA	V _{OH}	2.4	_	V

Parameter	Condition	Symbol	Min	Мах	Unit	
Output low voltage	I _{OL} = 8.0 mA	V _{OL}	—	0.5	V	
Output low voltage	I _{OL} = 3.2 mA	V _{OL}	—	0.4	V	

Table 69. SPI DC Electrical Characteristics (continued)

20.2 SPI AC Timing Specifications

This table provides the SPI input and output AC timing specifications.

Table	70.	SPI	AC	Timina	Specifications
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Parameter	Symbol ¹	Min	Мах	Unit
SPI outputs—Master mode (internal clock) delay	t _{NIKHOV}	0.5	6	ns
SPI outputs—Slave mode (external clock) delay	t _{NEKHOV}	2	8	ns
SPI inputs—Master mode (internal clock) input setup time	t _{NIIVKH}	4	—	ns
SPI inputs—Master mode (internal clock) input hold time	t _{NIIXKH}	0	—	ns
SPI inputs—Slave mode (external clock) input setup time	t _{NEIVKH}	4	—	ns
SPI inputs—Slave mode (external clock) input hold time	t _{NEIXKH}	2	—	ns

Notes:

 The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state) (reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{NIKHOV} symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).
</sub>

2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin. The maximum SPICLK input frequency is 66.666 MHz.

This figure provides the AC test load for the SPI.



Figure 48. SPI AC Test Load

These figures represent the AC timing from Table 70. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.







Figure 55. Single-Ended Reference Clock Input DC Requirements

21.2.3 Interfacing With Other Differential Signaling Levels

The following list provides information about interfacing with other differential signaling levels.

- With on-chip termination to SGND_SRDS*n* (xcorevss), the differential reference clocks inputs are HCSL (high-speed current steering logic) compatible DC-coupled.
- Many other low voltage differential type outputs like LVDS (low voltage differential signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 mV to 400 mV) for DC-coupled connection.
- LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

21.3 SerDes Transmitter and Receiver Reference Circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.



Figure 62. SerDes Transmitter and Receiver Reference Circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below in this document based on the application usage:

- Section 8, "Ethernet: Enhanced Three-Speed Ethernet (eTSEC)"
- Section 15, "PCI Express"
- Section 16, "Serial ATA (SATA)"

Note that an external AC coupling capacitor is required for the above three serial transmission protocols with the capacitor value defined in specification of each protocol section.

22 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions.

22.1 Package Parameters for the MPC8377E TePBGA II

The package parameters are provided in the following list. The package type is $31 \text{ mm} \times 31 \text{ mm}$, 689 plastic ball grid array (TePBGA II).

Package outline	$31 \text{ mm} \times 31 \text{ mm}$
Interconnects	689
Pitch	1.00 mm
Module height (typical)	2.0 mm to 2.46 mm (maximum)
Solder Balls	3.5% Ag, 96.5% Sn
Ball diameter (typical)	0.60 mm
Pitch Module height (typical) Solder Balls Ball diameter (typical)	1.00 mm 2.0 mm to 2.46 mm (maximum) 3.5% Ag, 96.5% Sn 0.60 mm

Table 72	. TePBGA	II Pinout	Listing	(continued)
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Signal	Package Pin Number	Pin Type	Power Supply	Note	
GPIO1[10]/GTM1_TGATE4_B/ GTM2_TGATE3_B/DACK3_B	J27	I/O	OVDD		
GPIO1[11]/GTM1_TOUT4_B/ GTM2_TOUT3_B/DDONE3_B	P24	I/O	OVDD	_	
	USB/GPIO2 Interface				
USBDR_CLK/GPIO2[23]	AJ11	I/O	OVDD	_	
USBDR_DIR_DPPULLUP/ GPIO2[9]	AG12	I/O	OVDD	_	
USBDR_NXT/GPIO2[8]	AJ10	I/O	OVDD	_	
USBDR_PCTL0/GPIO2[11]/ SD_DAT2	AF10	I/O	OVDD	—	
USBDR_PCTL1/GPIO2[22]/ SD_DAT3	AE9	I/O	OVDD	_	
USBDR_PWRFAULT/ GPIO2[10]/SD_DAT1	AG13	I/O	OVDD	_	
USBDR_STP_SUSPEND	AH12	0	OVDD	12	
USBDR_D0_ENABLEN/ GPIO2[0]	AG10	I/O	OVDD	_	
USBDR_D1_SER_TXD/ GPIO2[1]	AF13	I/O	OVDD	_	
USBDR_D2_VMO_SE0/ GPIO2[2]	AG11	I/O	OVDD	_	
USBDR_D3_SPEED/GPIO2[3]	AH11	I/O	OVDD	_	
USBDR_D4_DP/GPIO2[4]	AG9	I/O	OVDD		
USBDR_D5_DM/GPIO2[5]	AF9	I/O	OVDD		
USBDR_D6_SER_RCV/ GPIO2[6]	AH13	I/O	OVDD		
USBDR_D7_DRVVBUS/ GPIO2[7]	AH10	I/O	OVDD	_	
I ² C Interface					
IIC1_SCL	C12	I/O	OVDD	2	
IIC1_SDA	B12	I/O	OVDD	2	
IIC2_SCL	A10	I/O	OVDD	2	
IIC2_SDA	A12	I/O	OVDD	2	
	JTAG Interface				
ТСК	B13	I	OVDD	_	

	5	<i>\ \</i>
Unit	Default Frequency	Options
PCI Express1, 2	csb_clk/3	Off, c <i>sb_clk, csb_clk/2, csb_clk/3</i>
SATA1, 2	csb_clk/3	Off, <i>csb_clk</i>

Table 73. Configurable Clock Units (continued)

¹ This only applies to I^2C1 (I^2C2 clock is not configurable).

This table provides the operating frequencies for the TePBGA II package under recommended operating conditions (see Table 3).

Parameter ¹	Minimum Operating Frequency (MHz)	Maximum Operating Frequency (MHz)
e300 core frequency (<i>core_clk</i>)	333	800
Coherent system bus frequency (<i>csb_clk</i>)	133	400
DDR2 memory bus frequency (MCK) ¹	250	400
DDR1 memory bus frequency (MCK) ²	167	333
Local bus frequency (LCLKn) ¹	_	133
Local bus controller frequency (<i>lbc_clk</i>)	—	400
PCI input frequency (CLKIN or PCI_CLK)	25	66
eTSEC frequency	133	400
Security encryption controller frequency	—	200
USB controller frequency	—	200
eSDHC controller frequency	—	200
PCI Express controller frequency	-	400
SATA controller frequency	-	200

Table 74. Operating Frequencies for TePBGA II

Notes:

 The CLKIN frequency, RCWLR[SPMF], and RCWLR[COREPLL] settings must be chosen such that the resulting *csb_clk*, MCK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies. The value of SCCR[xCM] must be programmed such that the maximum internal operating frequency of the Security core, USB modules, SATA, and eSDHC will not exceed their respective value listed in this table.

2. The DDR data rate is $2 \times$ the DDR memory bus frequency.

3. The local bus frequency is ½, ¼, or 1/8 of the *lbiu_clk* frequency (depending on LCRR[CLKDIV]) which is in turn 1× or 2× the *csb_clk* frequency (depending on RCWLR[LBCM]).

23.1 System PLL Configuration

The system PLL is controlled by the RCWLR[SPMF] parameter. The system PLL VCO frequency depends on RCWLR[DDRCM] and RCWLR[LBCM]. Table 75 shows the multiplication factor encodings for the system PLL.

NOTE

If RCWLR[DDRCM] and RCWLR[LBCM] are both cleared, the system PLL VCO frequency = (CSB frequency) × (System PLL VCO Divider).

If either RCWLR[DDRCM] or RCWLR[LBCM] are set, the system PLL VCO frequency = $2 \times (CSB$ frequency) $\times (System PLL VCO Divider)$.

The VCO divider needs to be set properly so that the System PLL VCO frequency is in the range of 400–800 MHz.

RCWLR[SPMF]	System PLL Multiplication Factor
0000	Reserved
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110	× 6
0111–1111	\times 7 to \times 15

Table 75. System PLL Multiplication Factors

As described in Section 23, "Clocking," The LBIUCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (CLKIN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). Table 77 and Table 78 show the expected frequency values for the CSB frequency for select *csb_clk* to CLKIN/PCI_SYNC_IN ratios.

The RCWLR[SVCOD] denotes the system PLL VCO internal frequency as shown in Table 76.

Table 76. System PLL VCO Divider

RCWLR[SVCOD]	VCO Division Factor
00	4
01	8
10	2
11	1

			Input Clock Frequency (MHz) ²			
CFG_CLKIN_DIV at reset ¹	SPMF	<i>csb_clk</i> : Input Clock Ratio ¹	25	33.33	66.67	
			csb	_ <i>clk</i> Frequency (I	MHz)	
Low	0111	7:1	175	233		
Low	1000	8 : 1	200	267		
Low	1001	9 : 1	225	300		
Low	1010	10 : 1	250	333		
Low	1011	11 : 1	275	367		
Low	1100	12 : 1	300	400		
Low	1101	13 : 1	325			
Low	1110	14 : 1	350			
Low	1111	15 : 1	375			

Table 78. CSB Frequency Options for Agent Mode (continued)

Notes:

1. CFG_CLKIN_DIV doubles csb_clk if set high.

2. CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

23.2 Core PLL Configuration

RCWLR[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). Table 79 shows the encodings for RCWLR[COREPLL]. COREPLL values that are not listed in Table 79 should be considered as reserved.

NOTE

Core VCO frequency = core frequency \times VCO divider VCO divider has to be set properly so that the core VCO frequency is in the range of 800–1600 MHz.

RCWLR[COREPLL]			aara alki ash alk Patio	VCO Divider ¹	
0–1	2–5	6			
nn	0000	0	PLL bypassed (PLL off, <i>csb_clk</i> clocks core directly)	PLL bypassed (PLL off, <i>csb_clk</i> clocks core directly)	
11	nnnn	n	n/a	n/a	
00	0001	0	1:1	2	
01	0001	0	1:1	4	
10	0001	0	1:1	8	
00	0001	1	1.5:1	2	

Table 79. e300 Core PLL Configuration

The thermal performance of a device cannot be adequately predicted from the junction to ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_A + (R_{\theta JB} \times P_D)$$
 where:

 T_A = ambient temperature for the package (°C) $R_{\theta JB}$ = junction to board thermal resistance (°C/W) per JESD51-8 P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

24.2.3 Experimental Determination of Junction Temperature

NOTE

The heat sink cannot be mounted on the package.

To determine the junction temperature of the device in the application after prototypes are available, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature and a measure of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

 T_J = junction temperature (°C)

 T_T = thermocouple temperature on top of package (°C)

 Ψ_{JT} = junction to ambient thermal resistance (°C/W)

 P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per the JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

24.2.4 Heat Sinks and Junction-to-Case Thermal Resistance

For the power values the device is expected to operate at, it is anticipated that a heat sink will be required. A preliminary estimate of heat sink performance can be obtained from the following first-cut approach.

Tyco Electronics Chip Coolers[™] www.chipcoolers.com

Wakefield Engineering www.wakefield.com

Interface material vendors include the following:

Chomerics, Inc. www.chomerics.com

Dow-Corning Corporation Dow-Corning Electronic Materials www.dowcorning.com

Shin-Etsu MicroSi, Inc. www.microsi.com

The Bergquist Company www.bergquistcompany.com

24.3 Heat Sink Attachment

The device requires the use of heat sinks. When heat sinks are attached, an interface material is required, preferably thermal grease and a spring clip. The spring clip should connect to the printed circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces that can lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. The recommended maximum compressive force on the top of the package is 10 lb force (4.5 kg force). Any adhesive attachment should attach to painted or plastic surfaces, and its performance should be verified under the application requirements.

24.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When a heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimize the size of the clearance to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction to case thermal resistance.

 $T_J = T_C + (R_{\theta JC} \times P_D)$ where:

 T_J = junction temperature (°C) T_C = case temperature of the package (°C)

Table 87	. Document	Revision	History	(continued)
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Revision	Date	Substantive Change(s)
2	10/2009	 In Table 3, "Recommended Operating Conditions," added "Operating temperature range" values. In Table 5, "Power Dissipation ¹," corrected maximal application for 800/400 MHz to 4.3 W. In Table 5, "Power Dissipation ¹," added a column for "Typical Application at T_j = 65°C (W)". In Table 5, "Power Dissipation ¹," added a column for "Sleep Power at T_j = 65°C (W)". In Table 11, removed overbar from CFG_CLKIN_DIV. In Table 11, "Current Draw Characteristics for MV_{REF}," updated I_{MVREF} maximum value for both DDR1 and DDR2 to 600 and 400 µA, respectively. Also, updated Note 1 and added Note 2. In Table 20, "DDR1 and DDR2 SDRAM Input AC Timing Specifications," column headings renamed to "Min" and "Max". Footnote 2 updated to state "T is the MCK clock period". In Table 20, "DDR1 and DDR2 SDRAM Input AC Timing Specifications," and Table 21, "DDR1 and DDR2 SDRAM Output AC Timing Specifications," and Table 21, "DDR1 and DDR2 SDRAM Output AC Timing Specifications," and Table 21, "DDR1 and DDR2 SDRAM Output AC Timing Specifications," and Table 20, "DDR1 and DDR2 SDRAM Input AC Timing Specifications," and Table 20, "DDR1 and DDR2 SDRAM Input AC Timing Specifications," and Table 21, "DDR1 and DDR2 SDRAM Output AC Timing Specifications," updated t_{RMTDX}I to 2.0 ns. In Table 60, Gen 1i/1.5G Transmitter AC Specifications," and Table 62, Gen 2i/3G Transmitter AC Specifications," corrected titles from "Transmitter" to "Receiver". In Table 72, "TePBGA II Pinout Listing," removed pin THERM0; it is now Reserved. Also added 1.05 V to VDD pin. In Table 74, "Operating Frequencies for TePBGA II," corrected "DDR2 memory bus frequency (MCK)" range to 125–200. In Table 79, "e300 Core PLL Configuration," added 3.5:1 and 4:1 core_clk: csb_clk ratio options. In Table 80, "Example Clock Frequency Combinations," updated column heading to "DDR data rate" . In Section 20.2, "SPI AC Timing Specifications," correct
1	02/2009	 In Table 3, "Recommended Operating Conditions," added two new rows for 800 MHz, and created two rows for SerDes. In addition, changed 666 to 667 MHz. In Table 5, "Power Dissipation ¹," added Notes 4 and 5. In addition, changed 666 to 667 MHz. In Table 13, "DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V," Table 21, "DDR1 and DDR2 SDRAM Output AC Timing Specifications," and Table 72, "TePBGA II Pinout Listing," added footnote to references to MVREF, MDQ, and MDQS, referencing AN3665, <i>MPC837xE Design Checklist</i>. In Table 21, updated t_{DDKHCX} minimum value for 333 MHz to 2.40. In Table 72, "TePBGA II Pinout Listing," added footnote to USBDR_STP_SUSPEND and modified footnote 10 and added footnote 14. In Table 74, "Operating Frequencies for TePBGA II," changed 667 to 800 MHz for <i>core_clk</i>. In Table 80, "Example Clock Frequency Combinations," added 800 MHz cells for e300 core. Updated part numbering information in AF column in Table 84, "Part Numbering Nomenclature." In addition, modified extended temperature information in notes 1 and 4. In Table 85, "Available Parts (Core/DDR Data Rate)," added new row for 800/400 MHz.
0	12/2008	Initial public release.